CD4035BMS

CMOS 4 -Stage Parallel In/Parallel Out Shift Register

December 1992

Features

- **J - K̄ Serial Inputs and True/Complement Outputs**
- **High Voltage Type (20V Rating)**
- **4-Stage Clocked Shift Operation**
- **Synchronous Parallel Entry on All 4 Stages**
- **JK̄ Inputs on First Stage**
- **Asynchronous True/Complement Control on All Outputs**
- **Static Flip-Flop Operation; Master-Slave Configuration**
- **Buffered Inputs and Outputs**
- **High Speed Operation 12MHz (Typ) at VDD = 10V**
- **100% Tested for Quiescent Current at 20V**
- **Standardized, Symmetrical Output Characteristics**
- **5V, 10V and 15V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard Number 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Counters, Registers**
  - **Arithmetic-Unit Registers**
  - **Shift Left/Shift Right Registers**
  - **Serial-to-Parallel/Parallel-to-Serial Conversions**
- **Sequence Generation**
- **Control Circuits**
- **Code Conversion**

Description

CD4035BMS is a four stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via JK̄ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

JK̄ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With JK̄ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common, RESET is also provided.

The CD4035BMS series type is supplied in these 16 lead outline packages

Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4035BMS
TOP VIEW

Pin		Pin	
Q1/Q̄1	1	16	VDD
TRUE/COMP.	2	15	Q2/Q̄2
K̄	3	14	Q3/Q̄3
J	4	13	Q4/Q̄4
RESET	5	12	PI-4
CLOCK	6	11	PI-3
P/S	7	10	PI-2
VSS	8	9	PI-1

Functional Diagram

PARALLEL IN

9 1 10 2 11 3 12 4

SER IN { J 4, K̄ 3 }
CLK 6
P/S 7
T/C 2
RESET 5

4-STAGE REGISTER

VDD = 16
VSS = 8

1 15 14 13
Q1/Q̄1 Q2/Q̄2 Q3/Q̄3 Q4/Q̄4

T/C OUT
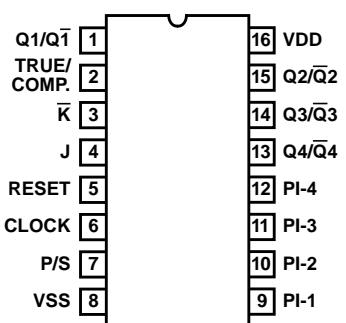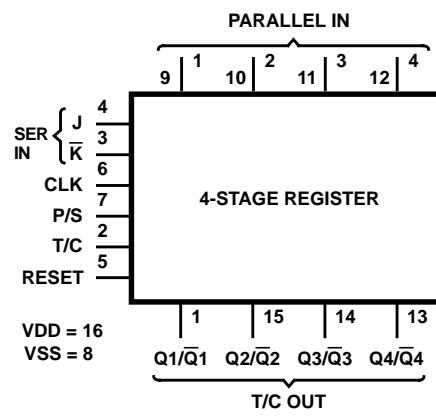
FIRST STAGE TRUTH TABLE

	tn-1 (INPUT)				tn (OUTPUT)
CL	J	K̄	R	Qn-1	Qn
⟋	0	X	0	0	0
⟋	1	X	0	0	1
⟋	X	0	0	1	0
⟋	1	0	0	Qn-1	Qn-1 Toggle Mode
⟋	X	1	0	1	1
⟍	X	X	0	Qn-1	Qn-1
X	X	X	1	X	0

File Number **3308**

Specifications CD4035BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
   (Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . .-0.5V to VDD +0.5V
DC Input Current, Any One Input . . . .±10mA
Operating Temperature Range. . . . . -55°C to +125°C
   Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . +265°C
   At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
   10s Maximum

Reliability Information

Thermal Resistance . . . . θ_{ja} θ_{jc}
   Ceramic DIP and FRIT Package . . . . . 80°C/W   20°C/W
   Flatpack Package . . . . 70°C/W   20°C/W
Maximum Package Power Dissipation (PD) at +125°C
   For TA = -55°C to +100°C (Package Type D, F, K) 500mW
   For TA = +100°C to +125°C (Package Type D, F, K) . . . . .Derate
             Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
   For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
        2. Go/No Go test with limits applied to inputs.
        3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Reset to Q	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	460	ns
			10, 11	+125°C, -55°C	-	621	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay Reset tO Q	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8	-	MHz
Maximum Clock Rise and Fall Time (Note 4)	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	15	µs
		VDD = 15V	1, 2, 3	+25°C	-	15	µs
Minimum Data Setup Time J/$\overline{K}$ Lines	TS	VDD = 5V	1, 2, 3	+25°C	-	220	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Data Setup Time Parallel-In Lines	TS	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.

2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

4. If more than one unit is cascaded, tRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	∆VTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	∆VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

3. See Table 2 for +25°C limit.

4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	$\pm$ 1.0μA
Output Current (Sink)	IOL5	$\pm$ 20% x Pre-Test Reading
Output Current (Source)	IOH5A	$\pm$ 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE:

1. 5% parametric, 3% functional; cumulative for static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST PRE-IRRAD	TEST POST-IRRAD	READ AND RECORD PRE-IRRAD	READ AND RECORD POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V $\pm$ -0.5V	OSCILLATOR 50kHz	OSCILLATOR 25kHz
Static Burn-In 1 Note 1	1, 13 - 15	2 - 12	16			
Static Burn-In 2 Note 1	1, 13 - 15	8	2 - 7, 9 - 12, 16			
Dynamic Burn-In Note 1	1, 3, 4	2, 5, 7 - 12	16	13 - 15	6	-
Irradiation Note 2	1, 13 - 15	8	2 - 7, 9 - 12, 16			

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V

2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram
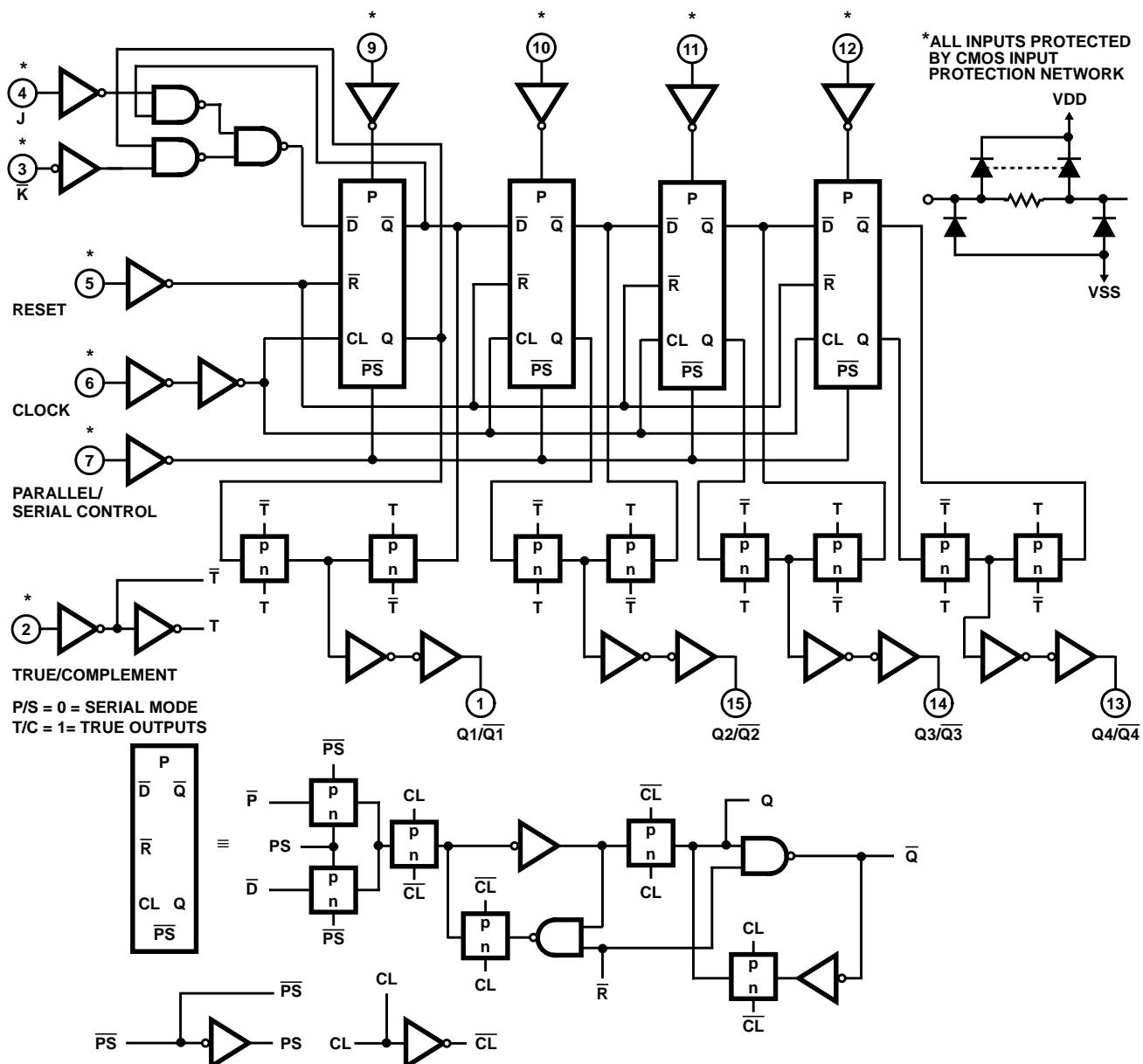
FIGURE 1. TYPICAL STAGE DETAIL LOGIC

Typical Performance Characteristics

AMBIENT TEMPERATURE (T$_A$) = +25°C

GATE-TO-SOURCE VOLTAGE (VGS) = 15V

10V

5V

Y-axis: OUTPUT LOW (SINK) CURRENT (IOL) (mA)
X-axis: DRAIN-TO-SOURCE VOLTAGE (VDS) (V)
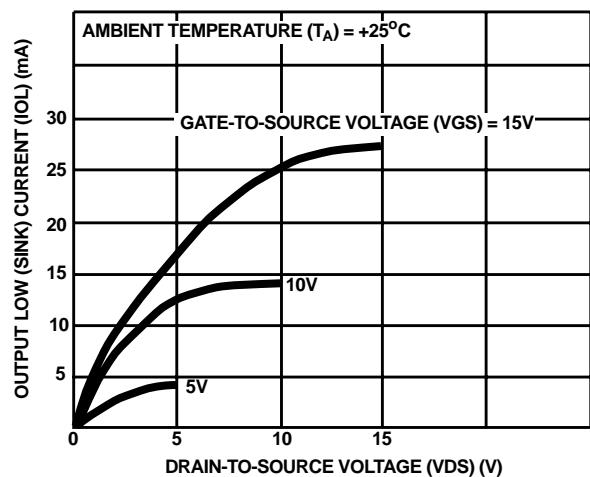
FIGURE 1 . TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

AMBIENT TEMPERATURE (T$_A$) = +25°C

GATE-TO-SOURCE VOLTAGE (VGS) = 15V

10V

5V

Y-axis: OUTPUT LOW (SINK) CURRENT (IOL) (mA)
X-axis: DRAIN-TO-SOURCE VOLTAGE (VDS) (V)
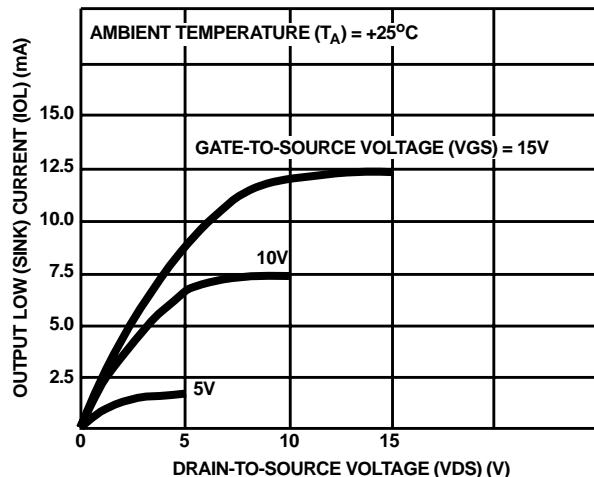
FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE (VDS) (V)

AMBIENT TEMPERATURE (T$_A$) = +25°C

GATE-TO-SOURCE VOLTAGE (VGS) = -5V

-10V

-15V

Y-axis: OUTPUT HIGH (SOURCE) CURRENT (IOH) (mA)
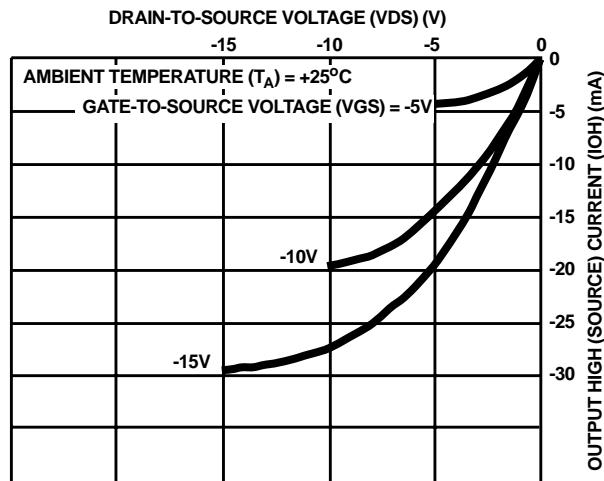
FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE (VDS) (V)

AMBIENT TEMPERATURE (T$_A$) = +25°C

GATE-TO-SOURCE VOLTAGE (VGS) = -5V

-10V

-15V

Y-axis: OUTPUT HIGH (SOURCE) CURRENT (IOH) (mA)
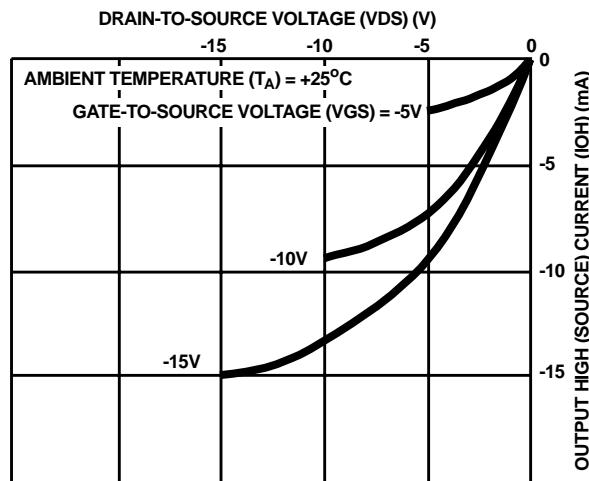
FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

AMBIENT TEMPERATURE (T$_A$) = +25°C

SUPPLY VOLTAGE (VDD) = 5V

10V

15V

Y-axis: TRANSITION TIME (tTHL, tTLH) (ns)
X-axis: LOAD CAPACITANCE (CL) (pF)
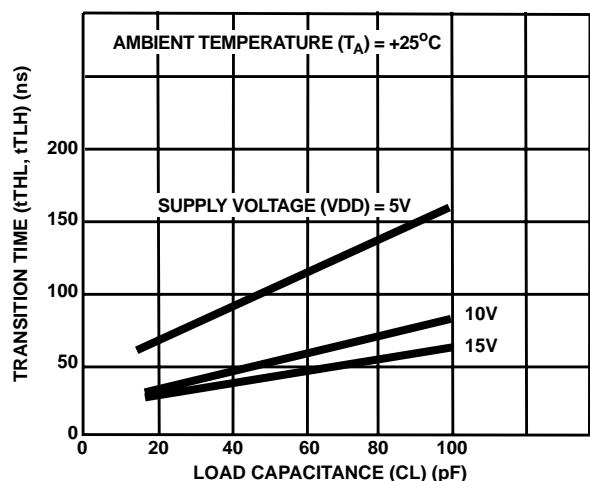
FIGURE 5. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

AMBIENT TEMPERATURE (T$_A$) = +25°C

CLOCKED OPERATION

SUPPLY VOLTAGE (VDD) = 5V

10V

15V

Y-axis: PROPAGATION DELAY TIME (tPHL, tPLH) (ns)
X-axis: LOAD CAPACITANCE (CL) (pF)
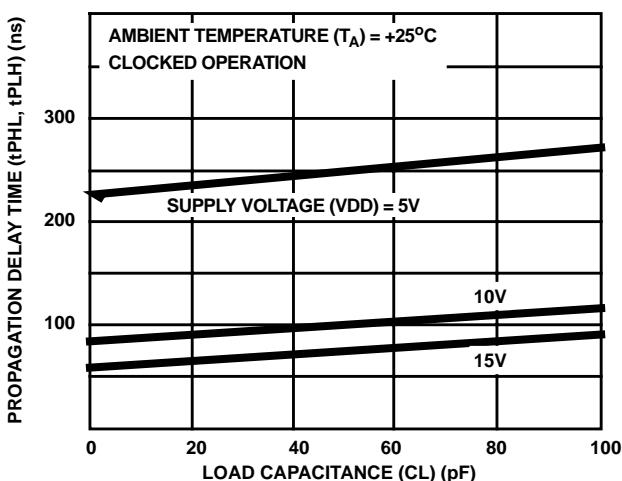
FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (Q OUTPUT)

Typical Performance Characteristics (Continued)
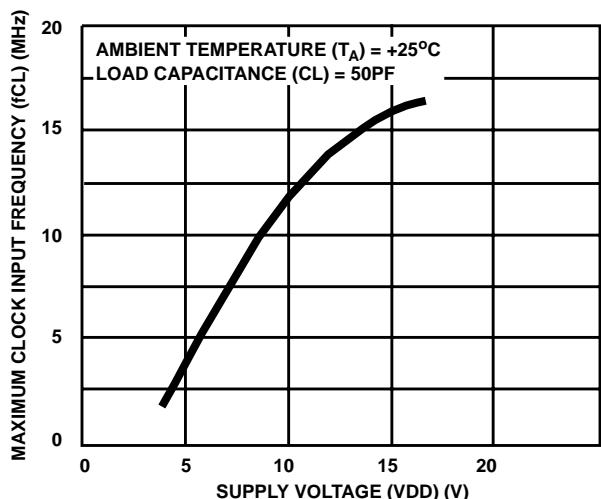
FIGURE 7. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE
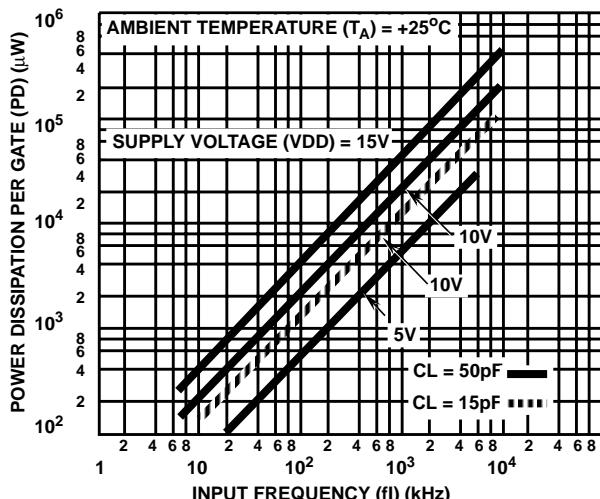
FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY
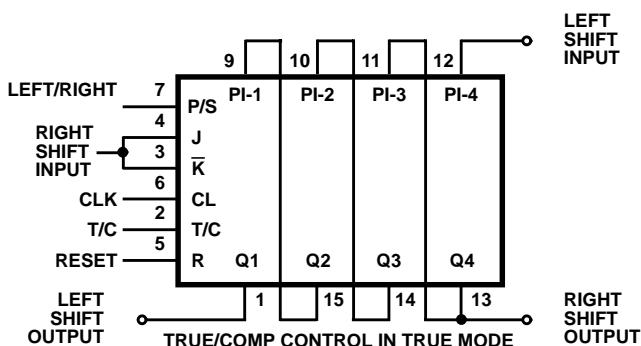
FIGURE 9. SHIFT LEFT/SHIFT RIGHT REGISTER
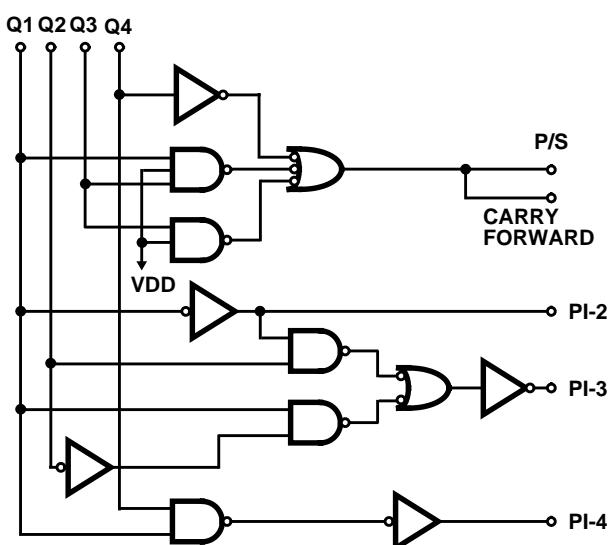
Using Couleur's Technique (BIDEC)*, a binary number (most significant bit, MSB) first is shifted and processed, such that the BCD equivalent is obtained when the last binary bit is clocked into the register. The CD4035BMS, with the correct conversion logic, can also be used as a BCD-to-binary converter.

*NOTE: The basic rule is: If a 4 or less is in a decade, shift with the next clock pulse; if a 5 or greater is in a decade, add 3 and then shift at the next clock pulse. For more information refer to "IRE TRANSACTIONS ON ELECTRONIC COMPUTERS", Dec. 1958, pages 313-316.

FIGURE 10. BIDEC LOGIC
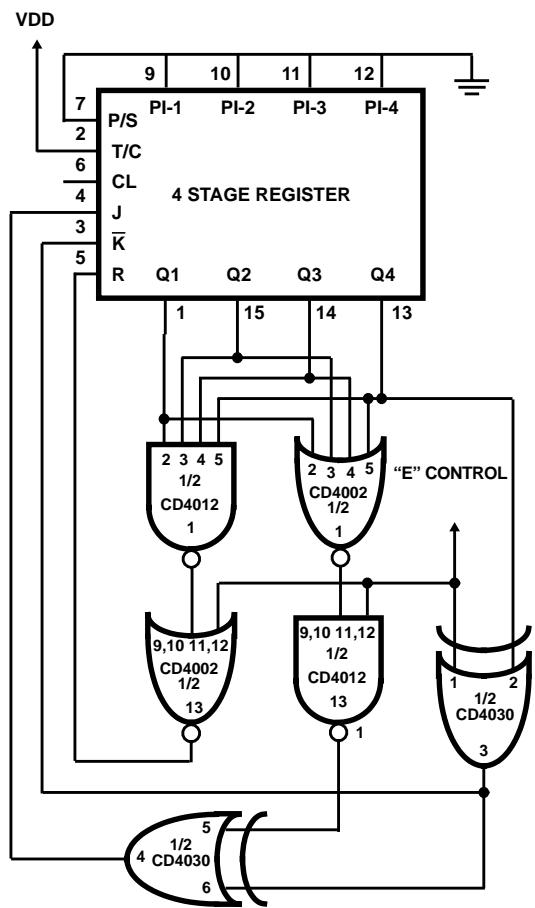
FIGURE 11(a). DOUBLE SEQUENCE GENERATOR

Control = E = 0					1				
	Q1 A	Q2 B	Q3 C	Q4 D		Q1 A	Q2 B	Q3 C	Q4 D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	1	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	0	0
8	0	0	0	1	7	1	1	1	0

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E).

FIGURE 11(b). STATE SEQUENCES
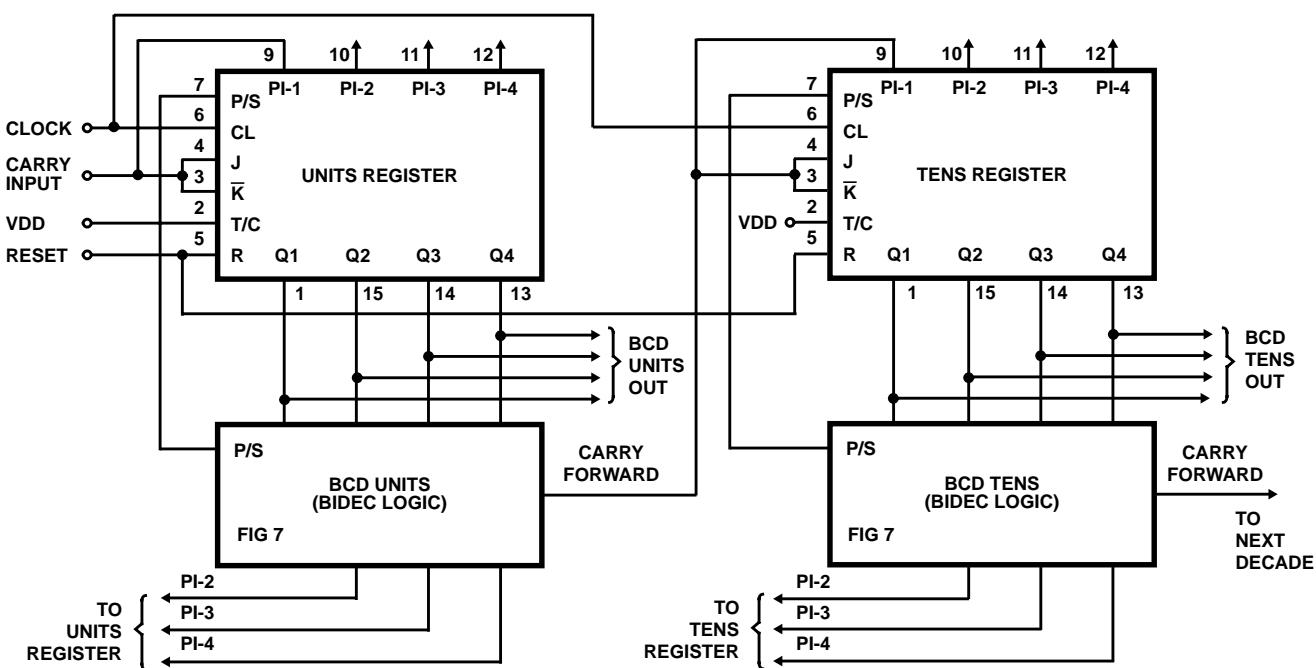
FIGURE 12. BINARY-TO-BCD CONVERTER

CD4035BMS

Chip Dimensions and Pad Layout
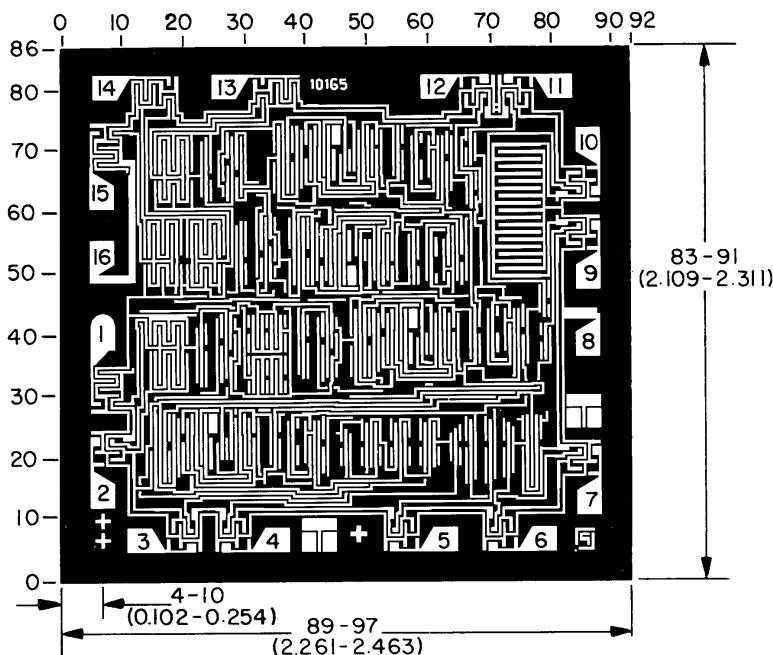
Dimensions in parantheses are in millimeters and
are derived from the basic inch dimensions as indicated.
Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

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