National Semiconductor

PRELIMINARY

CD4094BM/CD4094BC 8-Bit Shift Register/Latch with TRI-STATE® Outputs

General Description

The CD4094BM/CD4094BC consists of an 8-bit shift register and a TRI-STATE® 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_S) can be used to cascade several devices. Data on the Q_S output is transferred to a second output, Q'_S, on the following negative clock edge.

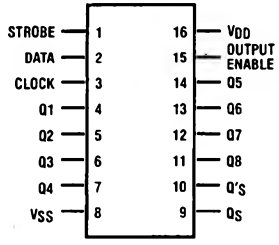
The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is high, data propagates through the latch to TRI-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken high.

TRI-STATE is a registered trademark of National Semiconductor Corp.

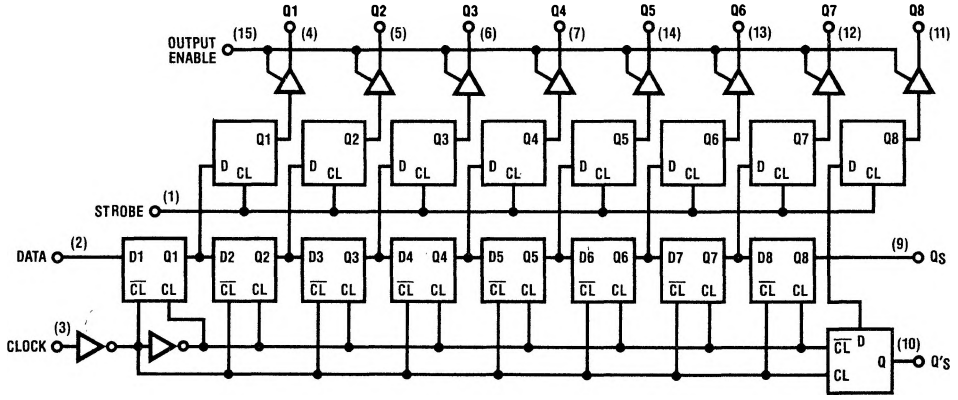
Features

■ Wide supply voltage range	3.0V to 18V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ TRI-STATE outputs	

Connection Diagram



Block or Logic Diagram



Absolute Maximum Ratings
(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions
(Note 2)

V_{DD} DC Supply Voltage	+3.0 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4094BM	−55°C to +125°C
CD4094BC	−40°C to +85°C

DC Electrical Characteristics CD4094BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		5.0			5.0		150	μA
	V_{DD} = 10 V		10			10		300	μA
	V_{DD} = 15 V		20			20		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
	V_{DD} = 10 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
	V_{DD} = 15 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O \rvert \leq 1\,\mu A$	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V, $\lvert I_O \rvert \leq 1\,\mu A$	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V, $\lvert I_O \rvert \leq 1\,\mu A$	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	0.88		−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	2.55		−0.9		mA
	V_{DD} = 15 V, V_O = 113.5 V	−4.2		−3.4	8.8		−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1			−0.1		−1.0	μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.1			0.1		1.0	μA

DC Electrical Characteristics CD4094BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD} Quiescent Device Current	V_{DD} = 5.0 V		20			20		150	μA
	V_{DD} = 10 V		40			40		300	μA
	V_{DD} = 15 V		80			80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
	V_{DD} = 10 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
	V_{DD} = 15 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O \rvert \leq 1\,\mu A$	4.95		4.95	5.0		4.95		V
	V_{DD} = 10 V, $\lvert I_O \rvert \leq 1\,\mu A$	9.95		9.95	10.0		9.95		V
	V_{DD} = 15 V, $\lvert I_O \rvert \leq 1\,\mu A$	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5.0 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.25		0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics (cont'd) CD4094BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{OH} High Level Output Current	$V_{DD}=5.0V$, $V_O=4.6V$	−0.52		−0.44	0.88		−0.36		mA
	$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	2.55		−0.9		mA
	$V_{DD}=15V$, $V_O=113.5V$	−3.6		−3.0	8.8		−2.4		mA
I_{IN} Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3			−0.3		−1.0	μA
	$V_{DD}=15V$, $V_{IN}=15V$		0.3			0.3		1.0	μA

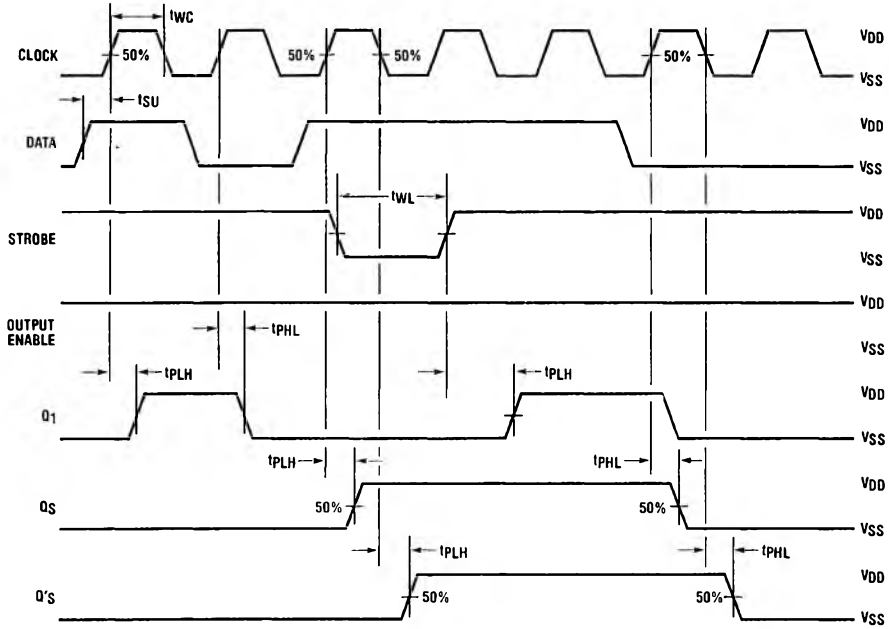
AC Electrical Characteristics $T_A=25°C$, $C_L=50pF$

		Conditions	Min.	Typ.	Max.	Units
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q_S	$V_{DD}=5.0V$		300		ns
		$V_{DD}=10V$		125		ns
		$V_{DD}=15V$		95		ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q'_S	$V_{DD}=5.0V$		230		ns
		$V_{DD}=10V$		110		ns
		$V_{DD}=15V$		75		ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Parallel Out	$V_{DD}=5.0V$		420		ns
		$V_{DD}=10V$		195		ns
		$V_{DD}=15V$		135		ns
t_{PHL}, t_{PLH}	Propagation Delay Strobe to Parallel Out	$V_{DD}=5.0V$		290		ns
		$V_{DD}=10V$		145		ns
		$V_{DD}=15V$		100		ns
t_{PHZ}	Propagation Delay High Level to High Impedance	$V_{DD}=5.0V$		140		ns
		$V_{DD}=10V$		75		ns
		$V_{DD}=15V$		55		ns
t_{PLZ}	Propagation Delay Low Level to High Impedance	$V_{DD}=5.0V$		225		ns
		$V_{DD}=10V$		95		ns
		$V_{DD}=15V$		70		ns
t_{PZH}	Propagation Delay High Impedance to High Level	$V_{DD}=5.0V$		225		ns
		$V_{DD}=10V$		95		ns
		$V_{DD}=15V$		70		ns
t_{PZL}	Propagation Delay High Impedance to Low Level	$V_{DD}=5.0V$		140		ns
		$V_{DD}=10V$		75		ns
		$V_{DD}=15V$		55		ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5.0V$		100		ns
		$V_{DD}=10V$		50		ns
		$V_{DD}=15V$		40		ns
t_{SU}	Set-up Time Data to Clock	$V_{DD}=5.0V$		60		ns
		$V_{DD}=10V$		30		ns
		$V_{DD}=15V$		20		ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{DD}=5.0V$	15			μs
		$V_{DD}=10V$	5.0			μs
		$V_{DD}=15V$	5.0			μs
t_{PC}	Minimum Clock Pulse Width	$V_{DD}=5.0V$		100		ns
		$V_{DD}=10V$		50		ns
		$V_{DD}=15V$		40		ns
t_{PS}	Minimum Strobe Pulse Width	$V_{DD}=5.0V$		100		ns
		$V_{DD}=10V$		40		ns
		$V_{DD}=15V$		35		ns
f_{MAX}	Maximum Clock Frequency	$V_{DD}=5.0V$		2.5		MHz
		$V_{DD}=10V$		5.0		MHz
		$V_{DD}=15V$		6.0		MHz
C_{IN}	Input Capacitance	Any Input		5.0		pF

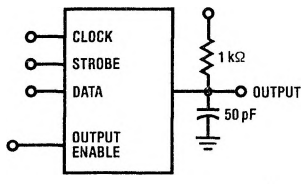
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

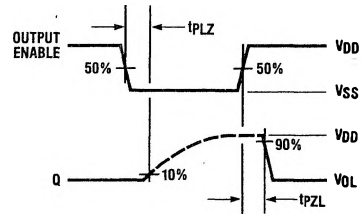
Timing Diagram

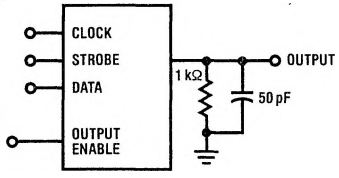


Test Circuits and Timing Diagrams for TRI-STATE®

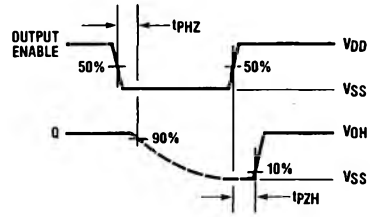


t_{PZL}, t_{PLZ}





t_{PZH}, t_{PHZ}



Logic Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S*	Q'S
↑	0	X	X	Hi-Z	Hi-Z	Q7	No Chg.
↓	0	X	X	Hi-Z	Hi-Z	No Chg.	Q7
↑	1	0	X	No Chg.	No Chg.	Q7	No Chg.
↑	1	1	0	0	$Q_N - 1$	Q7	No Chg.
↑	1	1	1	1	$Q_N - 1$	Q7	No Chg.
↓	1	1	1	No Chg.	No Chg.	No Chg.	Q7

X = Don't Care

*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.