

October 1987 Revised January 1999

### CD4512BC 8-Channel Buffered Data Selector

#### **General Description**

The CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a 3-STATE output. A high level at the Inhibit input forces a low level at the output. A high level at the  $\overline{\text{Output}}$  Enable  $\overline{\text{OE}}$ ) input forces the output into the 3-STATE condition. Low levels at both the Inhibit and  $\overline{\text{OE}}$ ) inputs allow normal operation.

#### **Features**

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V<sub>DD</sub> (typ.)
- 3-STATE output
- Low quiescent power dissipation: 0.25  $\mu$ W/package (typ.) @ V<sub>CC</sub> = 5.0V
- Plug-in replacement for Motorola MC14512

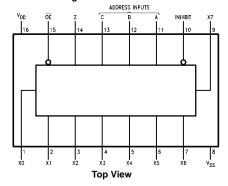
#### **Ordering Code:**

Order Number	Package Number	Package Description
CD4512BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4512BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

#### **Connection Diagram**

#### Pin Assignments for SOIC and DIP



#### **Truth Table**

Address Inputs			Control I	Output	
С	В	Α	Inhibit	OE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	Х3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
2	1	1	1	0	0
2	2	2	2	1	Hi-Z

2 = Don't care Hi-Z = 3-STATE condition Xn = Data at input n

#### **Absolute Maximum Ratings**(Note 1)

(Note 2)

Storage Temperature Range ( $T_S$ )  $-65^{\circ}C$  to  $+150^{\circ}C$ 

Power Dissipation (P<sub>D</sub>)

 Dual-In-Line
 700 mW

 Small Outline
 500 mW

Lead Temperature, (T<sub>L</sub>)

(Soldering, 10 seconds) 260°C

## Recommended Operating Conditions (Note 2)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The Recommended Operating Conditions and Electrical Characteristics table provide conditions for actual device operation.

Note 2:  $V_{SS} = 0V$  unless otherwise specified.

#### DC Electrical Characteristics (Note 2)

Parameter	Conditions	-40°C		+25°C		+85°C		Units	
i arameter	Mil		Max	Min	Тур	Max	Min	Max	Oilles
Quiescent Device	$V_{DD} = 5V$ , $V_{IN} = V_{DD}$ or $V_{SS}$		20		0.005	20		150	μΑ
Current	$V_{DD} = 10V$ , $V_{IN} = V_{DD}$ or $V_{SS}$		40		0.010	40		300	μΑ
	$V_{DD} = 15V$ , $V_{IN} = V_{DD}$ or $V_{SS}$		80		0.015	80		600	μΑ
LOW Level	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
Output Voltage	$V_{DD} = 10V$ $ I_{OL}  < 1 \mu A$		0.05		0	0.05		0.05	V
	V <sub>DD</sub> = 15V		0.05		0	0.05		0.05	V
HIGH Level	$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
Output Voltage	$V_{DD} = 10V$ $ I_{OH}  < 1 \mu A$	9.95		9.95	10.0		9.95		V
	V <sub>DD</sub> = 15V	14.95		14.95	15.0		14.95		V
LOW Level	$V_{DD} = 5V, V_{O} = 0.5V$		1.5		2.25	1.5		1.5	V
Input Voltage	$V_{DD} = 10V, V_{O} = 1.0V$		3.0		4.50	3.0		3.0	V
	$V_{DD} = 15V, V_{O} = 1.5V$		4.0		6.75	4.0		4.0	V
HIGH Level	$V_{DD} = 5V, V_{O} = 4.5V$	3.5		3.5	2.75		3.5		V
Input Voltage	$V_{DD} = 10V, V_{O} = 9.0V$	7.0		7.0	5.50		7.0		V
	$V_{DD} = 15V, V_{O} = 13.5V$	11.0		11.0	8.25		11.0		V
LOW Level Output	$V_{DD} = 5V, V_{O} = 0.4V$	0.52		0.44	0.78		0.36		mA
Current	$V_{DD} = 10V, V_{O} = 0.5V$	1.3		1.1	2.0		0.9		mA
(Note 3)	$V_{DD} = 15V, V_{O} = 1.5V$	3.6		3.4	7.8		2.4		mA
HIGH Level Output	$V_{DD} = 5V, V_{O} = 4.6V$	-0.2		-0.16			-0.12		mA
Current	$V_{DD} = 10V, V_{O} = 9.5$	-0.5		-0.4			-0.3		mA
(Note 3)	$V_{DD} = 15V, V_{O} = 13.5V$	-1.4		-1.2			-1.0		mA
Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		$-10^{-5}$	-0.3		-1.0	μΑ
	$V_{DD} = 15V, V_{IN} = 15V$		0.3		10 <sup>-5</sup>	0.3		1.0	μΑ
3-STATE	$V_{DD} = 15V, V_{O} = 0V$		±1.0		±10 <sup>-5</sup>	±1.0		±7.5	μΑ
Output Current	$V_{DD} = 15V, V_{O} = 15V$								
	Current  LOW Level Output Voltage  HIGH Level Output Voltage  LOW Level Input Voltage  HIGH Level Input Voltage  LOW Level Output Current (Note 3)  HIGH Level Output Current (Note 3)  Input Current (Note 3)	$ \begin{array}{c} \text{Current} & \text{V}_{\text{DD}} = 10\text{V}, \text{V}_{\text{IN}} = \text{V}_{\text{DD}} \text{ or } \text{V}_{\text{SS}} \\ \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{IN}} = \text{V}_{\text{DD}} \text{ or } \text{V}_{\text{SS}} \\ \text{CoUtput Voltage} & \text{V}_{\text{DD}} = 15\text{V} \\ \text{Output Voltage} & \text{V}_{\text{DD}} = 10\text{V} &  I_{\text{OL}}  < 1 \ \mu\text{A} \\ \text{V}_{\text{DD}} = 15\text{V} \\ \text{Output Voltage} & \text{V}_{\text{DD}} = 10\text{V} &  I_{\text{OH}}  < 1 \ \mu\text{A} \\ \text{V}_{\text{DD}} = 15\text{V} \\ \text{Output Voltage} & \text{V}_{\text{DD}} = 10\text{V} &  I_{\text{OH}}  < 1 \ \mu\text{A} \\ \text{V}_{\text{DD}} = 15\text{V} \\ \text{Input Voltage} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 0.5\text{V} \\ \text{Input Voltage} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 1.5\text{V} \\ \text{Input Voltage} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 4.5\text{V} \\ \text{Input Voltage} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 4.5\text{V} \\ \text{Input Voltage} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 3.5\text{V} \\ \text{LOW Level Output} & \text{V}_{\text{DD}} = 5\text{V}, \text{V}_{\text{O}} = 0.4\text{V} \\ \text{Current} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 0.5\text{V} \\ \text{(Note 3)} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 1.5\text{V} \\ \text{HIGH Level Output} & \text{V}_{\text{DD}} = 5\text{V}, \text{V}_{\text{O}} = 4.6\text{V} \\ \text{Current} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 9.5 \\ \text{(Note 3)} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 13.5\text{V} \\ \text{Input Current} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 13.5\text{V} \\ \text{Input Current} & \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{N}} = 0\text{V} \\ \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{N}} = 15\text{V}, \text{V}_{\text{N}} = 15\text{V} \\ \text{J}_{\text{DD}} = 15\text{V}, \text{V}_{\text{N}} = 15\text{V}, \text{V}_{\text{N}} = 0\text{V} \\ \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{O}} = 0.5\text{V} \\ \text{V}_{\text{DD}} = 15\text{V}, \text{V}_{\text{N}} = 15\text{V}, \text{V}_{\text{N}} = 15\text{V} \\ \text{J}_{\text{DD}} = 15\text{V}, \text{V}_{\text{N}} = 0\text{V} \\ \text{V}_{\text{DD}} $	Quiescent Device         V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> Current         V <sub>DD</sub> = 10V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> V <sub>DD</sub> = 15V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> LOW Level         V <sub>DD</sub> = 5V           Output Voltage         V <sub>DD</sub> = 10V   I <sub>OL</sub>   < 1 μA	Quiescent Device         V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> 20           Current         V <sub>DD</sub> = 10V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> 40           V <sub>DD</sub> = 15V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> 80           LOW Level         V <sub>DD</sub> = 5V         0.05           Output Voltage         V <sub>DD</sub> = 10V   I <sub>OL</sub>   < 1 μA	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Quiescent Device         V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> 20         0.005         20           Current         V <sub>DD</sub> = 10V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> 40         0.010         40           LOW Level         V <sub>DD</sub> = 15V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> 80         0.015         80           LOW Level         V <sub>DD</sub> = 5V         0.05         0         0.05           Output Voltage         V <sub>DD</sub> = 15V         4.95         0.05         0         0.05           HIGH Level         V <sub>DD</sub> = 5V         4.95         4.95         5.0         4.95           Output Voltage         V <sub>DD</sub> = 10V   I <sub>I OH</sub>   < 1 μA	Quiescent Device $V_{DD} = 5V, V_{IN} = V_{DD} \text{ or } V_{SS}$ 20         0.005         20         150           Current $V_{DD} = 10V, V_{IN} = V_{DD} \text{ or } V_{SS}$ 40         0.010         40         300           LOW Level $V_{DD} = 15V, V_{IN} = V_{DD} \text{ or } V_{SS}$ 80         0.015         80         600           LOW Level $V_{DD} = 5V$ 0.05         0         0.05         0         0.05         0.05           Output Voltage $V_{DD} = 15V$ 4.95         0.05         0         0.05<

Note 3:  $\rm I_{OH}$  and  $\rm I_{OL}$  are tested one output at a time.

# AC Electrical Characteristics (Note 4) $T_A = 25^{\circ}C, \, t_r = t_f = 20 \text{ ns, } C_L = 50 \text{ pF}$

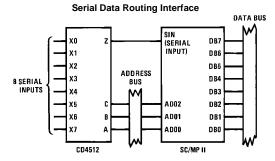
Symbol	Parameter	Conditions	(	CD4512BM			CD4512BC		
Syllibol			Min	Тур	Max	Min	Тур	Max	Units
t <sub>PHL</sub>	Propagation Delay	$V_{DD} = 5V$		225	500		225	750	ns
	HIGH-to-LOW Level	$V_{DD} = 10V$		75	175		75	200	ns
		$V_{DD} = 15V$		57	130		57	150	ns
t <sub>PLH</sub>	Propagation Delay	$V_{DD} = 5V$		225	500		225	750	ns
	LOW-to-HIGH Level	$V_{DD} = 10V$		75	175		75	200	ns
		$V_{DD} = 15V$		57	130		57	150	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Transition Time	$V_{DD} = 5V$		70	200		70	200	ns
		$V_{DD} = 10V$		35	100		35	100	ns
		$V_{DD} = 15V$		25	80		25	80	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Propagation Delay into	$V_{DD} = 5V$		50	125		50	125	ns
	3-STATE from Logic Level	$V_{DD} = 10V$		25	75		25	75	ns
		$V_{DD} = 15V$		19	60		19	60	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Propagation Delay to Logic	$V_{DD} = 5V$		50	125		50	125	ns
	Level from 3-STATE	$V_{DD} = 10V$		25	75		25	75	ns
		$V_{DD} = 15V$		19	60		19	60	ns
C <sub>IN</sub>	Input Capacitance	(Note 5)		7.5	15		7.5	15	pF
C <sub>OUT</sub>	3-STATE Output	(Note 5)		7.5	15		7.5	15	pF
	Capacitance								
C <sub>PD</sub>	Power Dissipation Capacity	(Note 6)		150			150		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

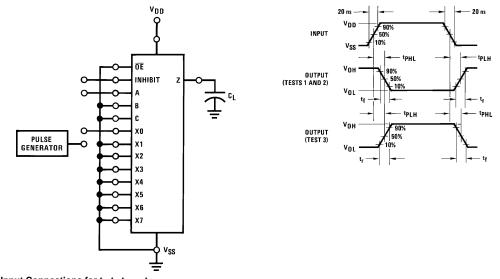
Note 5: Capacitance guaranteed by periodic testing.

Note 6: C<sub>PD</sub> determines the no load AC power of any CMOS device. For complete explanation, see Family Characteristics Application Note, AN-90.

#### **Typical Application**



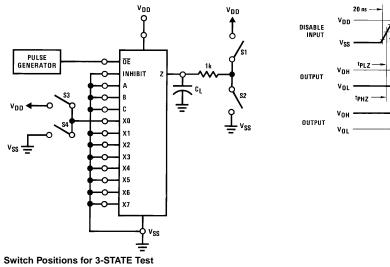
#### **AC Test Circuit and Switching Time Waveforms**



Input Connections for  $t_{\rm r},\,t_{\rm f},\,t_{\rm PLH},\,t_{\rm PHL}$ 

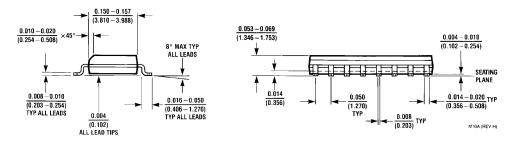
Test	Inhibit	Α	X0
1	PG	GND	$V_{DD}$
2	GND	PG	$V_{DD}$
3	GND	GND	PG

### **3-STATE AC Test Circuit and Switching Time Waveforms**



Test	S1	S2	S3	S4
t <sub>PHZ</sub>	Open	Closed	Closed	Open
$t_{PLZ}$	Closed	Open	Open	Closed
$t_{PZL}$	Closed	Open	Open	Closed
t <sub>PZH</sub>	Open	Closed	Closed	Open

## 



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Wide Package Number M16A

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) $\frac{0.740 - 0.780}{(18.80 - 19.81)}$ (2.286) 16 15 14 13 12 11 10 9 16 15 INDEX AREA $\frac{0.250 \pm 0.010}{(6.350 \pm 0.254)}$ PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 8 1 2 L OPTION 01 OPTION 02 0.065 (1.651) $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ $\frac{0.060}{(1.524)}$ TYP 4° TYP OPTIONAL 0.300 = 0.320 (7.620 = 8.128) ¥ $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 95° ± 5° $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 90°±4° TYP $\frac{0.020}{(0.508)}$ 0.280 0.125 - 0.150 (3.175 - 3.810) (7.112) $0.030 \pm 0.015$ (0.762 ± 0.381) MIN $\frac{0.014 - 0.023}{(0.356 - 0.584)}$ 0.100 ± 0.010 (0.325 +0.040 -0.015 $(2.540 \pm 0.254)$ 0.050 ± 0.010 N16E (REV F) (8.255 **+**1.016 **-**0.381 (1.270 ± 0.254)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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