intersil

CD4518BMS, CD4520BMS

December 1992

CMOS Dual Up Counters

Features

- **High Voltage Types (20V Rating)**
- **CD4518BMS Dual BCD Up Counter**
- **CD4520BMS Dual Binary Up Counter**
- **Medium Speed Operation**
  - **6MHz Typical Clock Frequency at 10V**
- **Positive or Negative Edge Triggering**
- **Synchronous Internal Carry Propagation**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Noise Margin (Over Full Package/Temperature Range)**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Standardized Symmetrical Output Characteristics**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Multistage Synchronous Counting**
- **Multistage Ripple Counting**
- **Frequency Dividers**

Description

CD4518BMS Dual BCD Up Counter and CD4520BMS Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

The CD4518BMS and CD4520BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	H4S
Frit Seal DIP	H1F
Ceramic Flatpack	*H6P †H6W
*CD4518B Only	†CD4520B Only

Pinout

CD4518BMS, CD4520BMS
TOP VIEW

Pin			Pin
CLOCK A	1	16	VDD
ENABLE A	2	15	RESET B
Q1A	3	14	Q4B
Q2A	4	13	Q3B
Q3A	5	12	Q2B
Q4A	6	11	Q1B
RESET A	7	10	ENABLE B
VSS	8	9	CLOCK B

Functional Diagram

VSS = 8
VDD = 16

File Number **3342**
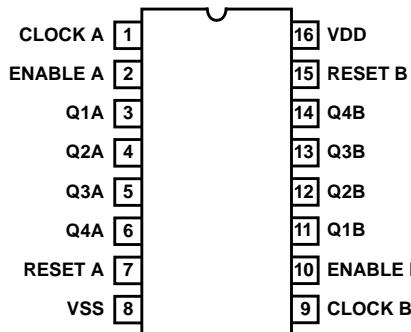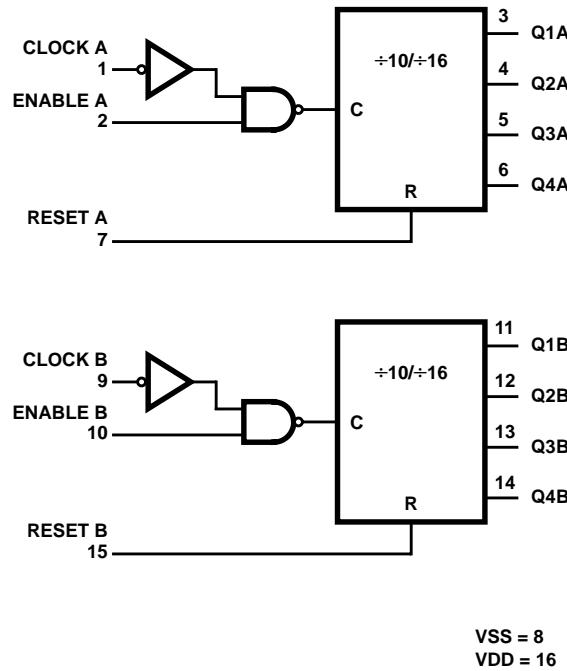
Specifications CD4518BMS, CD4520BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
  (Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . .-0.5V to VDD +0.5V
DC Input Current, Any One Input . . . .±10mA
Operating Temperature Range. . . . . -55°C to +125°C
  Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . +265°C
  At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
  10s Maximum

Reliability Information

Thermal Resistance . . . . θ_{ja} θ_{jc}
  Ceramic DIP and FRIT Package . . . . . 80°C/W   20°C/W
  Flatpack Package . . . . 70°C/W   20°C/W
Maximum Package Power Dissipation (PD) at +125°C
  For T_A = -55°C to +100°C (Package Type D, F, K) 500mW
  For T_A = +100°C to +125°C (Package Type D, F, K). . . . . .Derate
               Linearity at 12mW/^{o}C to 200mW
Device Dissipation per Output Transistor 100mW
  For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
       2. Go/No Go test with limits applied to inputs.
       3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	560	ns
			10, 11	+125°C, -55°C	-	756	ns
Propagation Delay Reset to Ouput	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	650	ns
			10, 11	+125°C, -55°C	-	878	ns
Transition Time (Note 2)	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	1.5	-	MHz
			10, 11	+125°C, -55°C	1.11	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Reset to Output	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	225	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	3	-	MHz
		VDD = 15V	1, 2, 3	+25°C	4	-	MHz
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 4	+25°C	-	5	µs
		VDD = 15V	1, 2, 3, 4	+25°C	-	5	µs
Minimum Enable Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.

2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	∆VTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	∆VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.   3. See Table 2 for +25°C limit.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.   4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3-6, 11-14	1, 2, 7-10, 15	16			
Static Burn-In 2 Note 1	3-6, 11-14	8	1, 2, 7, 9, 10, 15, 16			
Dynamic Burn-In Note 1	-	7, 8, 15	2, 10, 16	3-6, 11-14	1, 9	
Irradiation Note 2	3-6, 11-14	8	1, 2, 7, 9, 10, 15, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V

2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams
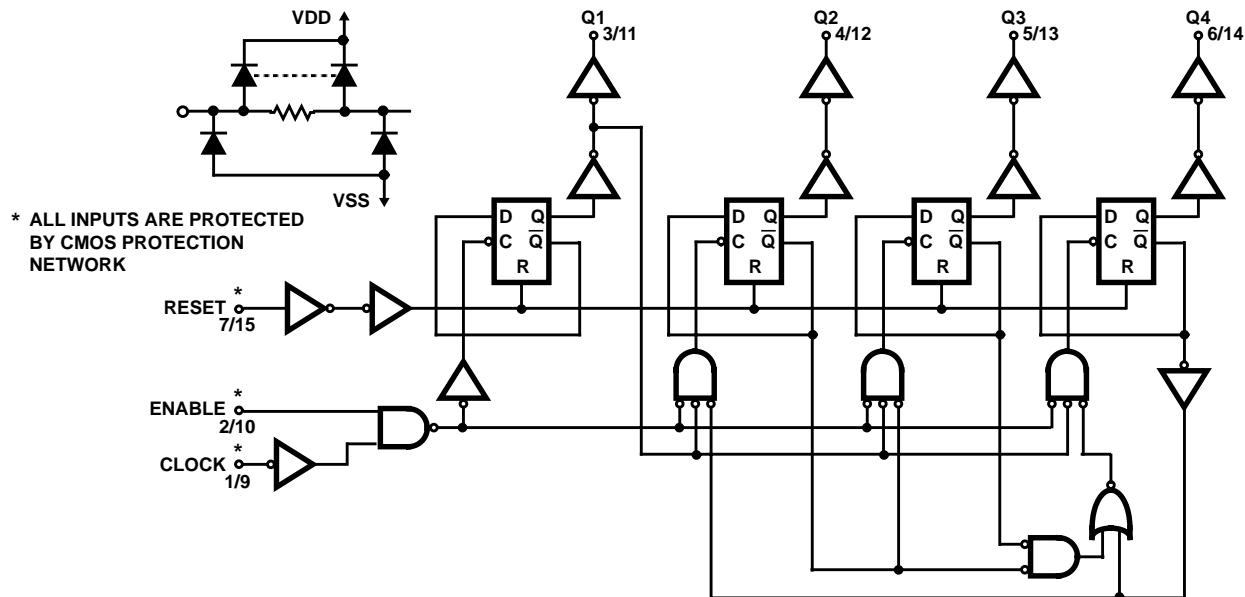
FIGURE 1. DECADE COUNTER (CD4518BMS) LOGIC DIAGRAM FOR ONE OF TWO IDENTICAL COUNTERS
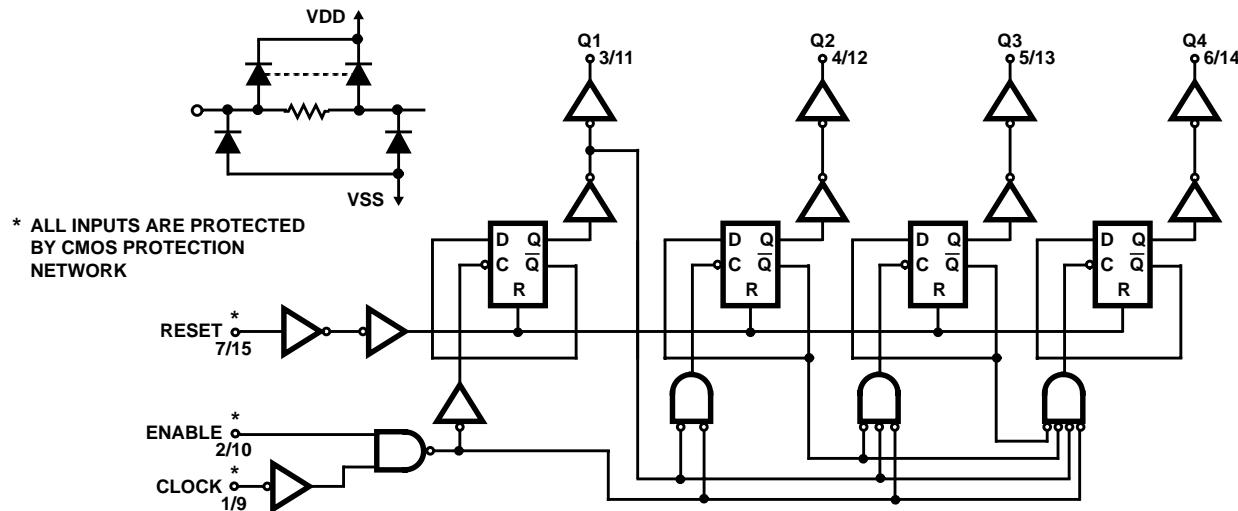
FIGURE 2. BINARY COUNTER (CD4520BMS) LOGIC DIAGRAM FOR ONE OF TWO IDENTICAL COUNTERS

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
___/‾	1	0	Increment Counter
0	‾___	0	Increment Counter
‾___	X	0	No Change
X	___/‾	0	No Change
___/‾	0	0	No Change
1	‾___	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care   1 ≡ High State   0 ≡ Low State

Typical Performance Curves
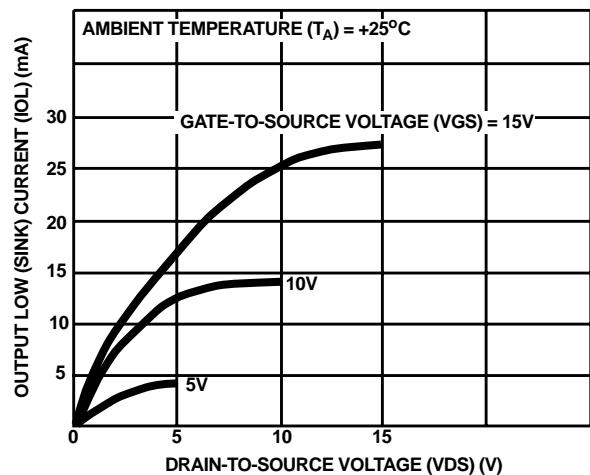
FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT
CHARACTERISTICS
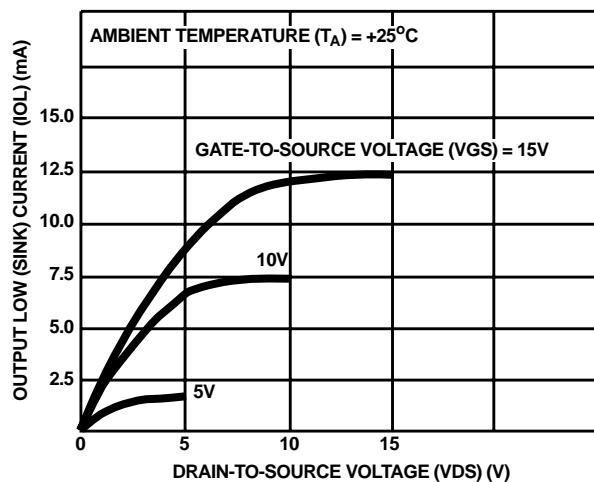
FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT
CHARACTERISTICS
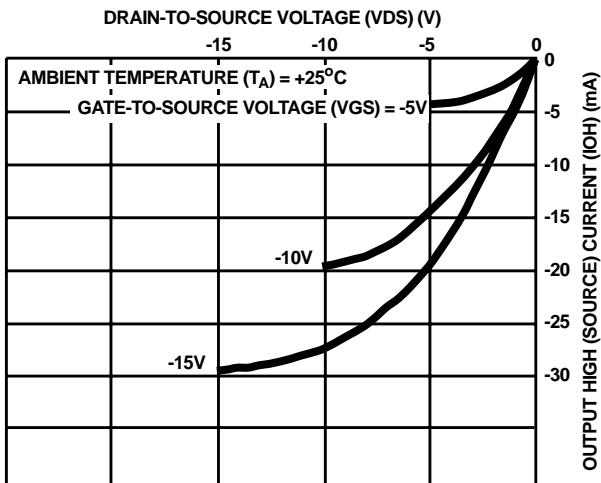
FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT
CHARACTERISTICS
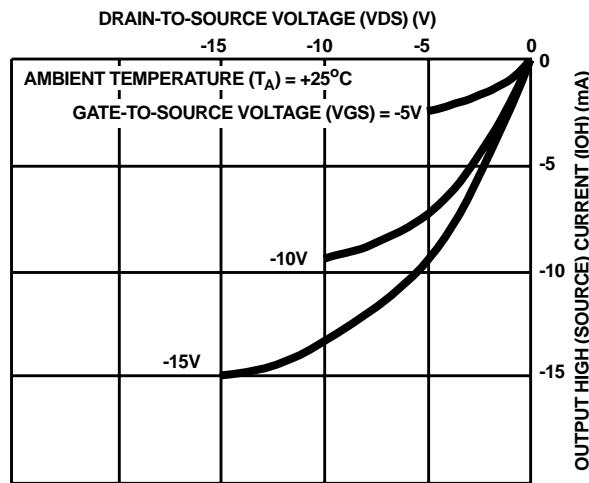
FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT
CHARACTERISTICS
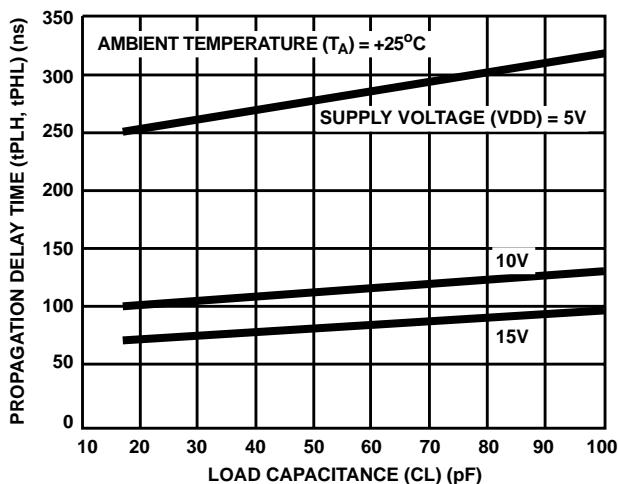
FIGURE 7. TYPICAL PROPAGATION DELAY vs LOAD CAPAC-
ITANCE, CLOCK OR ENABLE TO OUTPUT
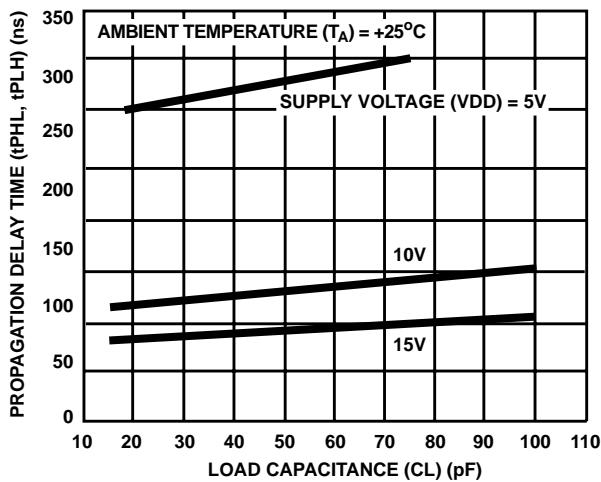
FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD
CAPACITANCE, RESET TO OUTPUT

Typical Performance Curves
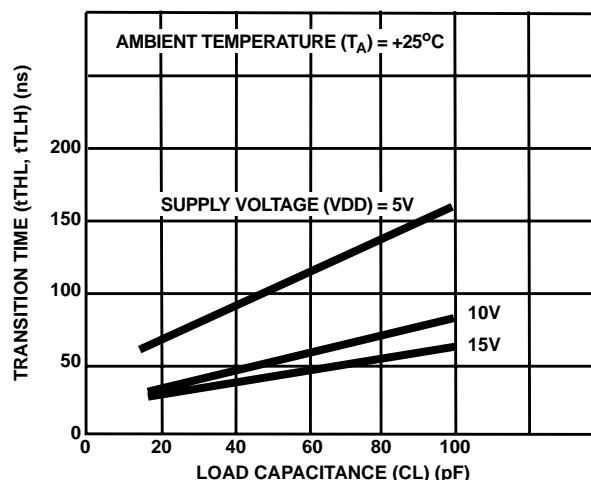
FIGURE 9. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE
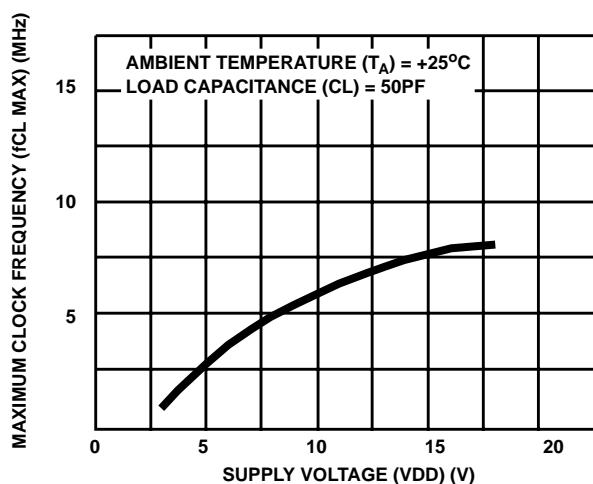
FIGURE 10. TYPICAL MAXIMUM CLOCK FREQUENCY vs SUPPLY VOLTAGE
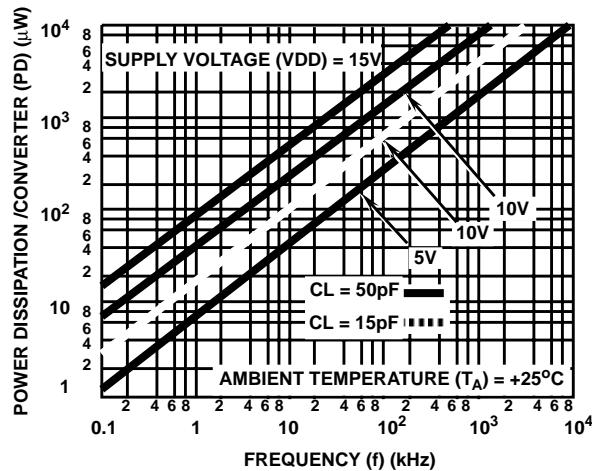
FIGURE 11. TYPICAL POWER DISSIPATION CHARACTERISTICS

Timing Diagrams
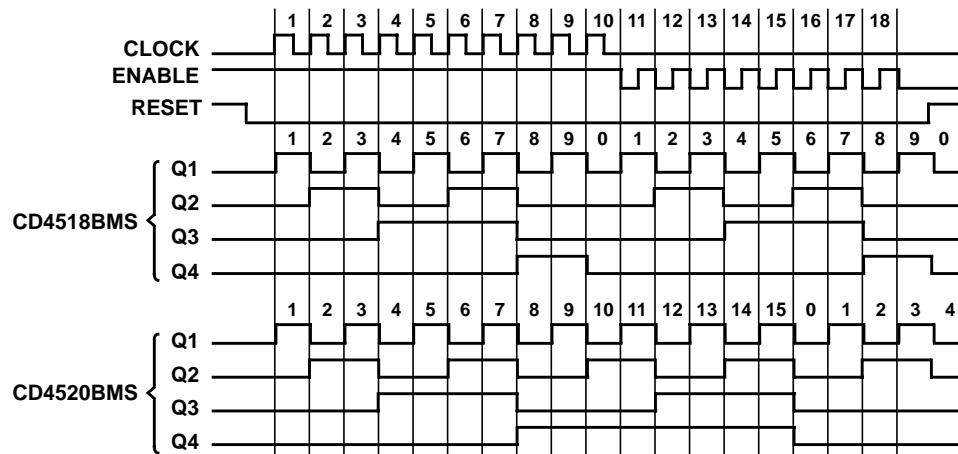
FIGURE 12. TIMING DIAGRAMS FOR CD4518BMS AND CD4520BMS
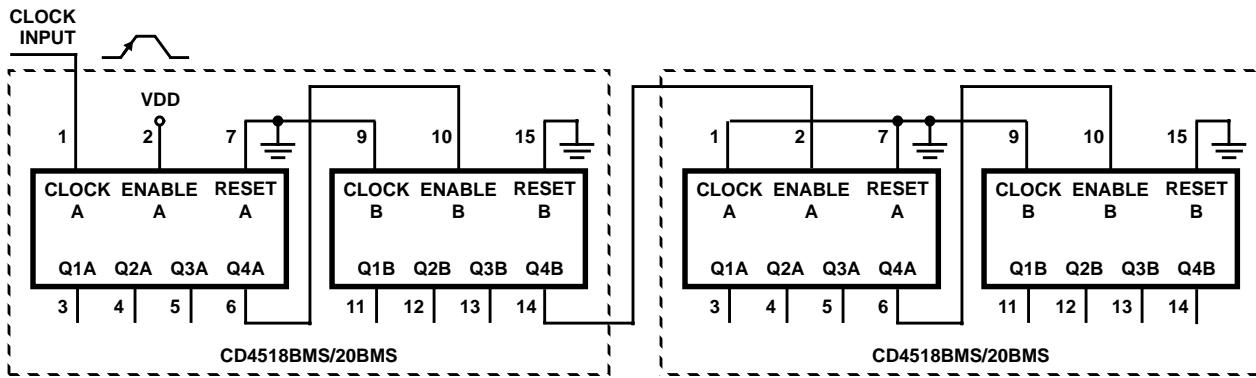
FIGURE 13. RIPPLE CASCADING OF FOUR COUNTERS WITH POSITIVE EDGE TRIGGERING
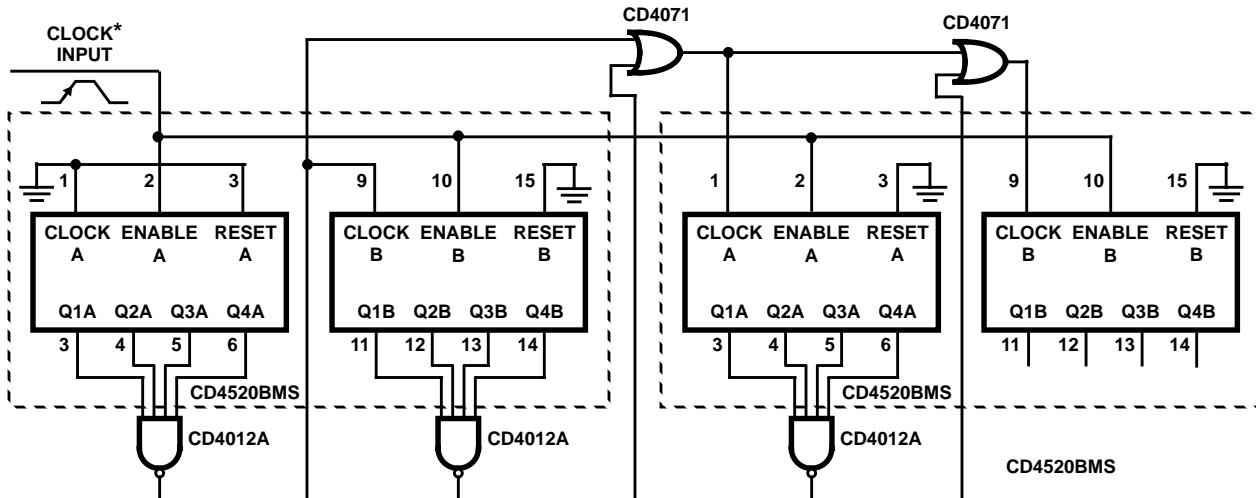
* For synchronous cascading, the clock transition time should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the output driver stage for the estimated capacitive load.

FIGURE 14. SYNCHRONOUS CASCADING OF FOUR BINARY COUNTERS WITH NEGATIVE EDGE TRIGGERING

Chip Dimensions and Pad Layouts
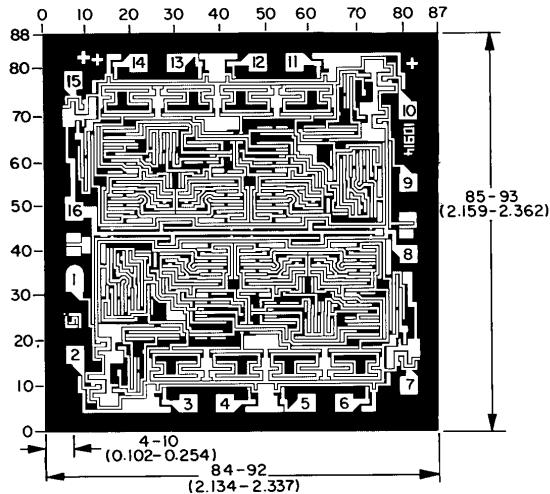
CD4518BMS
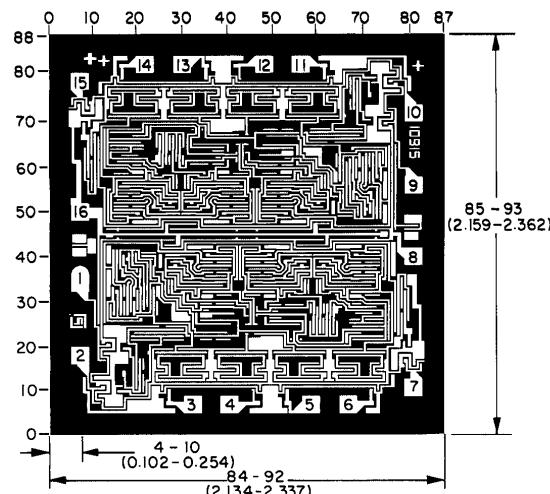
CD4520BMS

Dimensions in parenthesis are in millimeters and are
derived from the basic inch dimensions as indicated.
Grid graduations are in mils (10-3 inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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