National Semiconductor

CD4543BM/CD4543BC BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals

General Description

The CD4543BM/CD4543BC is a monolithic CMOS BCD-to-7-segment latch/decoder/driver for use with liquid crystal and other types of displays. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-7-segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI) and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display, and the outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features

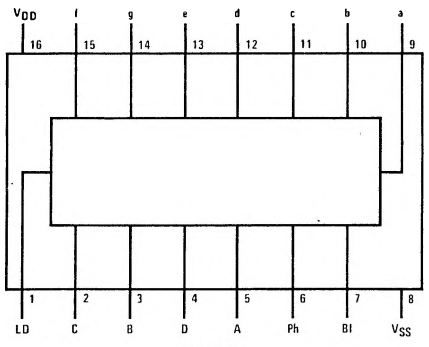
- Wide supply voltage range — 3.0 V to 18 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Low power dissipation — 50 nA/package (typ.) at V_{DD} = 5.0 V
- Latch storage
- Blanking input
- Blank for all illegal inputs
- Direct-drive LCD, LED and VF displays
- Pin-for-pin replacement for CD4056B (with pin 7 tied to V_{SS})
- Pin-for-pin replacement for Motorola MC14543B

Applications

- Instrument (e.g., counter, DVM, etc.) display driver
- Computer/calculator display driver
- Cockpit display driver
- Various clock, watch, and timer users

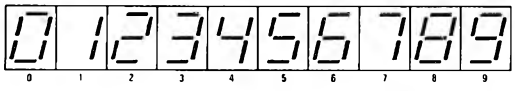
Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW

Display Format



INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as Above

X = Don't care
† = Above combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 V_{DC} to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4543BM	−55°C to +125°C
CD4543BC	−40°C to +85°C

DC Electrical Characteristics CD4543BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4			2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4543BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0			2.4		mA

DC Electrical Characteristics CD4543BC (Note 2) (Continued)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, V_{SS} = 0, unless otherwise specified.

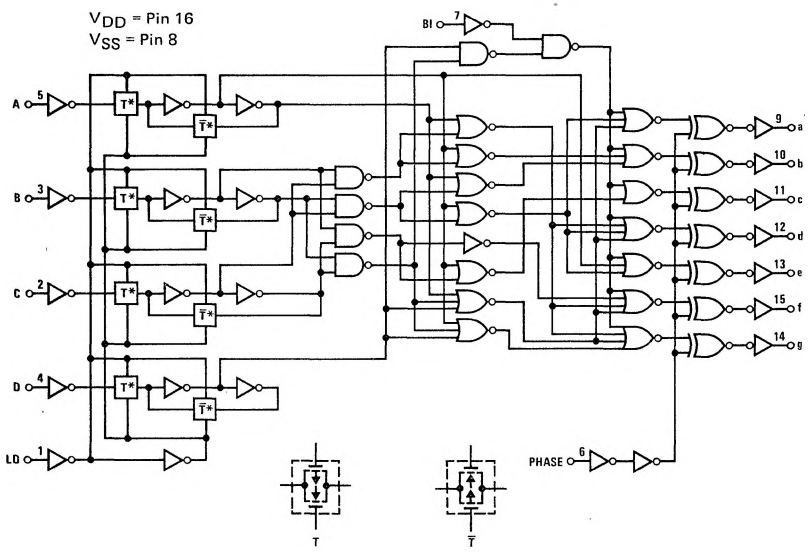
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Output Rise Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_f	Output Fall Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}	Turn-ON Propagation Delay Time	V_{DD} = 5V		450	1100	ns
		V_{DD} = 10V		170	440	ns
		V_{DD} = 15V		110	330	ns
t_{PHL}	Turn-OFF Propagation Delay Time	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		180	440	ns
		V_{DD} = 15V		120	330	ns
t_{SET-UP}	Set-Up Time	V_{DD} = 5V		−5	80	ns
		V_{DD} = 10V		−2	30	ns
		V_{DD} = 15V		0	20	ns
t_{HOLD}	Hold Time	V_{DD} = 5V		30	120	ns
		V_{DD} = 10V		20	45	ns
		V_{DD} = 15V		15	30	ns
PW_{LD}	Latch Disable Pulse Width	V_{DD} = 5V		50	250	ns
		V_{DD} = 10V		30	100	ns
		V_{DD} = 15V		20	80	ns
C_{IN}	Input Capacitance	Per Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	See C_{PD} Measurement Waveforms, (Note 3)		300		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load AC power consumption of a CMOS device. For a complete explanation, see "MM54C/74C Family Characteristics" application note AN-90.

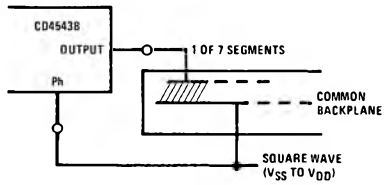
Logic Diagram



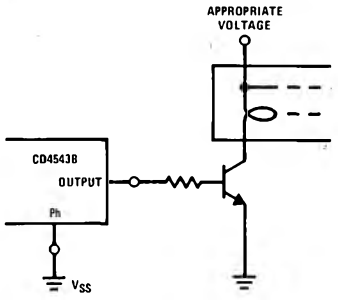
*Transmission gates

Typical Applications

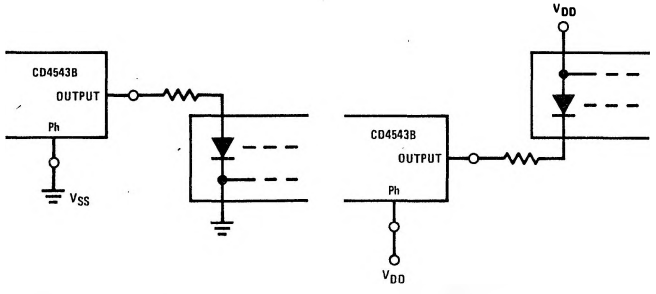
Liquid Crystal (LC) Readout



Incandescent Readout



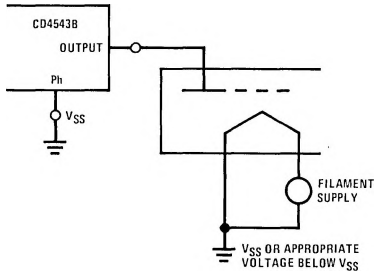
Light Emitting Diode (LED) Readout



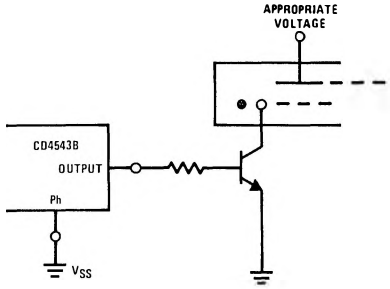
Note. Bipolar transistors may be added for gain (for $V_{DD} \leq 10V$ or $I_{OUT} \geq 10$ mA)

Typical Applications (Continued)

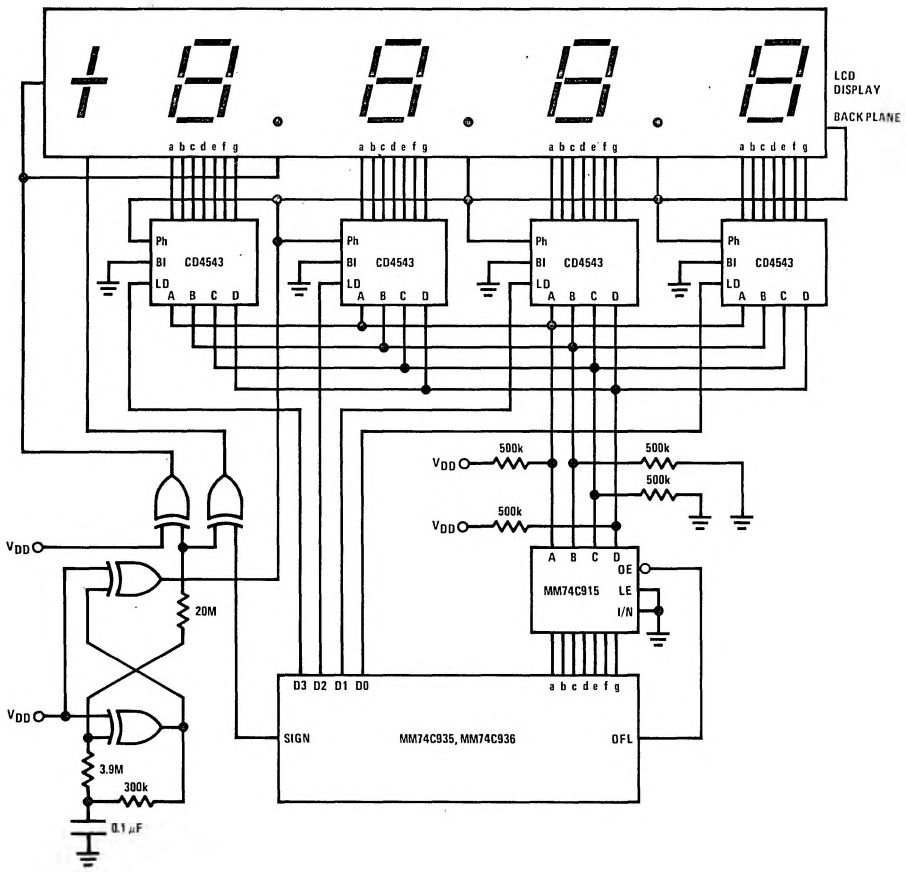
Fluorescent Readout



Gas Discharge Readout



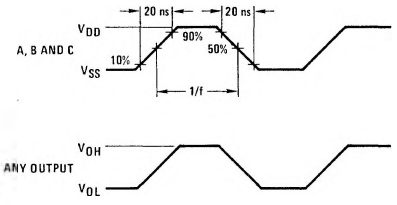
3 1/2-Digit DVM with LCD Display



Display 9.999 when overflowed. All digits can also be blanked at overflow by tying OFL to BI on the CD4543's

Switching Time Waveforms

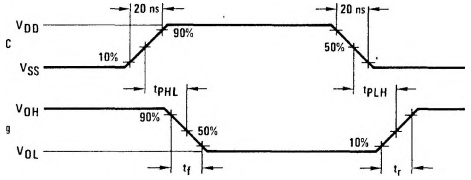
C_{PD} Measurement Waveforms



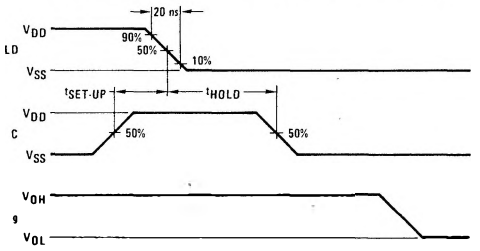
Inputs BI and Ph low, and inputs D and LD high. f in respect to a system clock.
All outputs connected to respective C_L loads.

Dynamic Signal Waveforms

(a) Inputs D, Ph and BI low, and inputs A, B and LD high



(b) Inputs D, Ph and BI low, and inputs A and B high



(c) Data DCBA strobe into latches