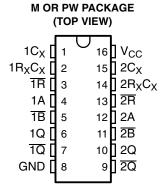
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- Qualified for Automotive Applications
- Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of R_X, C_X
- Triggering From the Leading or Trailing Edge
- Q and Q Buffered Outputs Available
- Separate Resets
- Wide Range of Output Pulse Widths
- Schmitt-Trigger Input on A and B Inputs
- Retrigger Time Is Independent of C_X
- Fanout (Over Temperature Range)
 - Standard Outputs ... 10 LSTTL Loads
 - Bus Driver Outputs ... 15 LSTTL Loads

description/ordering information

The CD74HC4538 is a dual retriggerable/resettable precision monostable multivibrator for fixed-voltage timing applications. An external resistor (R_X) and

- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- V_{CC} Voltage = 2 V to 6 V
- High Noise Immunity N_{IL} or N_{IH} = 30% of V_{CC}, V_{CC} = 5 V



external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and \overline{Q} terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of R_X and C_X .

Leading-edge triggering (A) and trailing-edge triggering (\overline{B}) inputs are provided for triggering from either edge of the input pulse. An unused A input should be tied to GND and an unused \overline{B} input should be tied to V_{CC} . On power up, the IC is reset. Unused resets and sections must be terminated. In normal operation, the circuit retriggers on the application of each new trigger pulse. To operate in the nontriggerable mode, \overline{Q} is connected to \overline{B} when leading-edge triggering (A) is used, or Q is connected to A when trailing-edge triggering (\overline{B}) is used. The period (τ) can be calculated from τ = (0.7) R_X , C_X ; R_{MIN} is 5 $k\Omega$. C_{MIN} is 0 pF.

ORDERING INFORMATION[†]

T _A	PACK	(AGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
40°C to 105°C	SOIC - M	Tape and reel	CD74HC4538QM96Q1	HC4538M
-40°C to 125°C	TSSOP - PW	Tape and reel	CD74HC4538QPWRQ1	HC4538M

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

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FUNCTION TABLE

	INPUTS	OUTPUTS				
R	Α	В	Q	Q		
L	Х	Х	L	Н		
Х	Н	Χ	L	Н		
Х	Χ	L	L	Н		
Н	L	\downarrow	Л	Т		
Н	\uparrow	Н	Л	Т		

NOTE: H = High voltage level

L = Low voltage level

↑ = Transition from low to high level

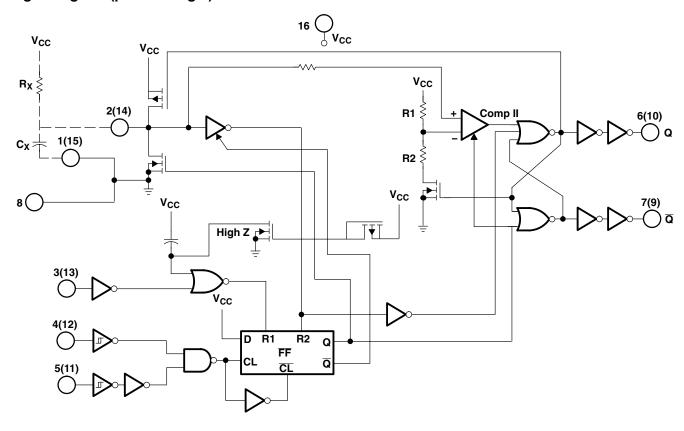
 \downarrow = Transition from high to low level

 \Box = one high-level pulse

☐ = one low-level pulse

X = Irrelevant

logic diagram (positive logic)





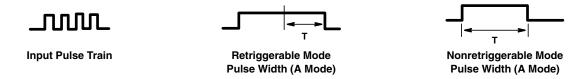
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FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	•	TO NUMBER	_	TO NUMBER	INPUT PI TERMINAL	ULSE TO . NUMBER	OTHER CONNECTIONS		
	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂	
Leading-edge trigger/retriggerable	3, 5	11, 13			4	12			
Leading-edge trigger/nonretriggerable	3	13			4	12	5–7	11–9	
Trailing-edge trigger/retriggerable	3	13	4	12	5	11			
Trailing-edge trigger/nonretriggerable	3	13			5	11	4–6	12–10	

NOTES: 1. A retriggerable one-shot multivibrator has an output pulse width that is extended one full time period (T) after application of the last trigger pulse.

2. A nontriggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$)	±20 mA
Output clamp current, I_{OK} ($V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$)	±20 mA
Switch current per output pin, I_O ($V_O > -0.5 \text{ V}$ or $V_O < V_{CC} + 0.5 \text{ V}$)	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ _{JA} (see Note 2): M package	73°C/W
PW package	108°C/W
Maximum junction temperature, T _J	150°C
Lead temperature (during soldering):	
At distance 1/16 \pm 1/32 inch (1,59 \pm 0,79 mm) from case for 10 s max	300°C
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are referenced to GND, unless otherwise specified.
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

				MIN	MAX	UNIT	
V_{CC}	Supply voltage			2	6	V	
			V _{CC} = 2 V	1.5			
V_{IH}	High-level input voltage		V _{CC} = 4.5 V	3.15		V	
			V _{CC} = 6 V	4.2			
			V _{CC} = 2 V		0.5		
V_{IL}	Low-level input voltage		$V_{CC} = 4.5 \text{ V}$		1.35	V	
			V _{CC} = 6 V		1.8		
VI	Input voltage	0	V_{CC}	V			
Vo	Output voltage			0	V_{CC}	V	
			V _{CC} = 2 V	0	0 1000		
		Reset input	V _{CC} = 4.5 V	0	500		
١.	Land Land West Color and Cally Pro-		V _{CC} = 6 V	0	400		
t _t	Input transition (rise and fall) time		V _{CC} = 2 V	0	Unlimited	ns	
		Trigger inputs A or B	V _{CC} = 4.5 V	0	Unlimited		
		V _{CC} = 6 V	0	Unlimited			
R _X	External timing resistor (see Note 4)			5		kΩ	
C _X	External timing capacitor (see Note 4)			0		F	
T _A	Operating free-air temperature	·	·	-40	125	°C	

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4. The maximum allowable values of R_X and C_X are a function of leakage of capacitor C_X , leakage of the CD74HC4538, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 30 mA. Susceptibility to externally induced noise signals may occur for $R_X > 1$ M Ω .



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I _O (mA)	v _{cc}	T _A = 2	25°C	T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT	
					MIN	MAX	MIN	MAX	MIN	MAX		
				2 V	1.9		1.9		1.9			
		CMOS loads	-0.02	4.5 V	4.4		4.4		4.4			
V _{OH}	$V_i = V_{iH}$ or V_{iL}			6 V	5.9		5.9		5.9		V	
		TTI locale	-4	4.5 V	3.98		3.84		3.7			
		TTL loads	-5.2	6 V	5.48		5.34		5.2			
	$V_{I} = V_{IH}$ or V_{IL}		2 V		0.1		0.1		0.1			
		CMOS loads	0.02	4.5 V		0.1		0.1		0.1		
V _{OL}		or V _{IL}		6 V		0.1		0.1		0.1	V	
		TTI leads	4	4.5 V		0.26		0.33	0.33	0.4		
		TTL loads	5.2	6 V		0.26		0.33		0.4		
	V VOND	A, B, R		6 V		±0.1		±1		±1	•	
I _I	$V_I = V_{CC}$ or GND	R _X C _X (see Note 5)		6 V		±0.05		±0.5		±0.5	μ A	
		Quiescent	0	6 V		8		80		160	μΑ	
Icc	$V_I = V_{CC}$ or GND	Active, Q = high, Pins 2 and 14 at V _{CC} /4	0	6 V		0.6		0.8		1	mA	
C _{IN}	C _L = 50 pF					10		10		10	pF	

NOTE 5: When testing I_{IL} , the Q output must be high. If Q is low (device not triggered), the pullup P device is ON and the low-resistance path from V_{DD} to the test pin causes a current far exceeding the specification.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	PARAMETER		T,	_A = 25°C	;	T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
		2 V	80			100		120		
t _w	Input pulse width	4.5 V	16			20		24		ns
		6 V	14			17		20		
		2 V	5			5		5		
t _{su}	Reset setup time	4.5 V	5			5		5		ns
		6 V	5			5		5		
t _{rr}	Retrigger time (see Figure 4)	5 V		175						ns
	Output pulse-width match, same package			±1						%

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	LOAD	v _{cc}	T,	_A = 25°C	;	T _A = -		T _A = -		UNIT	
	(INPUT)	(OUTPUT)	CAPACITANCE		MIN	MIN TYP MAX			MAX	MIN	MAX		
				2 V			250		315		375		
	4 5	0 0	C _L = 50 pF	4.5 V			50		63		75		
	A, \overline{B}	Q or Q		6 V			43		54		64		
			C _L = 15 pF	5 V		21							
t _{pd}				2 V			250		315		375	ns	
	R	0 0	C _L = 50 pF	4.5 V			50		63		75		
	H QorQ	Q or Q	y or Q	6 V			43		54		64		
			C _L = 15 pF	5 V		21							
				2 V			75		95		110		
t _t			C _L = 50 pF	4.5 V			15		19		22	ns	
				6 V			13		16		19	1	
τ†			C 50 pF	3 V	0.64		0.78	0.612	0.812	0.605	0.819	mo	
τι			C _L = 50 pF	5 V	0.63		0.77	0.602	0.798	0.595	0.805	ms	

 $^{^{\}dagger}$ Output pulse width with R_X = 10 $k\Omega$ and C_X = 0.1 μF

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, input t_r , $t_f = 6 \text{ ns}$, $C_L = 15 \text{ pF}$

	PARAMETER	TYP	UNIT
Ср	Power dissipation capacitance (see Note 6)	136	pF

NOTE 6: C_{pd} is used to determine the dynamic power consumption, per one shot.

 $P_D = (C_{pd} + C_X) V_{CC}^2 f_I \Sigma (C_L V_{CC}^2 f_O)$

f_I = input frequency

f_O = output frequency

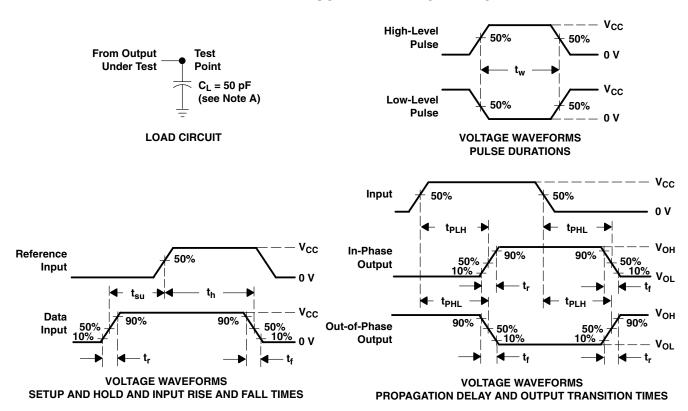
C_L = output load capacitance

C_X = external capacitance

 V_{CC} = supply voltage, assuming $f_I \ll I/\tau$

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

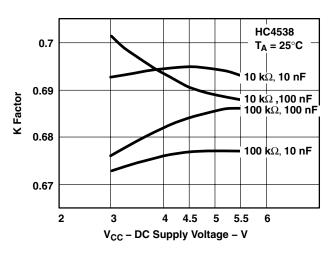


Figure 2. K Factor vs DC Supply Voltage

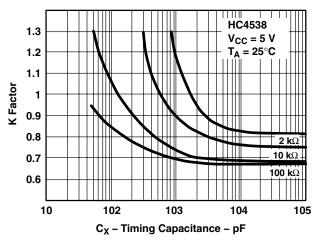


Figure 3. K Factor vs C_X

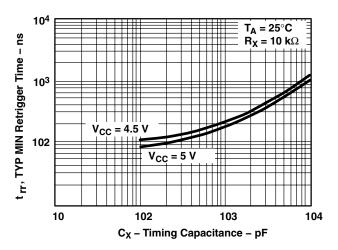


Figure 4. Minimum Retrigger Time vs Timing Capacitance



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TYPICAL APPLICATION DATA

power-down mode

During a rapid power-down condition (as would occur with a power-supply short circuit with a poorly filtered power supply), the energy stored in C_X could discharge into pin 2 or pin 14. To avoid possible device damage in this mode when C_X is $\geq 0.5 \, \mu F$, a protection diode with a 1-A rating or higher (1N5395 or equivalent) and a separate ground return for C_X should be provided (see Figure 5).

An alternate protection method is shown in Figure 6, where a $51-\Omega$ current-limiting resistor is inserted in series with C_X . Note that a small pulse-duration decrease occurs, however, and R_X must be increased appropriately to obtain the originally desired pulse duration.

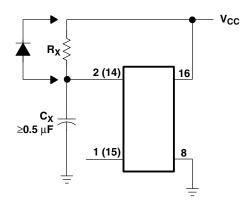


Figure 5. Rapid-Power-Down Protection Circuit

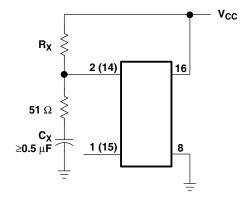


Figure 6. Alternative Rapid-Power-Down Protection Circuit

6-Jan-2013

PACKAGING INFORMATION

Orderable Device		Package Type		Pins	Package Qty	Eco Plan	Lead/Ball Finish		Samples
	(1)		Drawing			(2)		(3)	(Requires Login)
CD74HC4538QM96G4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538QM96Q1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
CD74HC4538QPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4538QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD74HC4538-Q1:





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Military: CD54HC4538

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

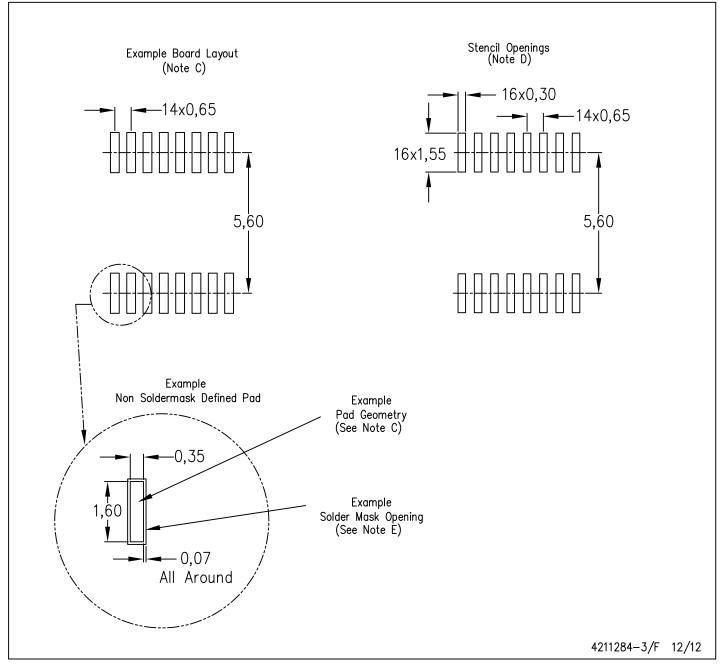


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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