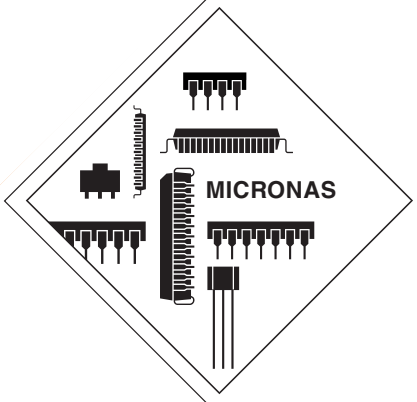

ADVANCE INFORMATION

CDC3272G-B V1.0 Automotive Controller Specification

ARM POWERED®

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MICRONAS

Contents

1. Introduction

The device is a microcontroller for use in automotive applications. The on-chip CPU is an ARM® processor ARM7TDMI™ with 32-bit data and address bus, which supports Thumb™ format instructions.

The chip contains timer/counters, interrupt controller, multi channel AD converter, stepper motor and LCD driver, CAN interfaces and PWM outputs and a crystal clock multiplying PLL.

This document provides ROM hardware specific information. General information on operating the IC can be found in the document “CDC32xxG-B V3.0 Hardware Manual and CDC3205G-B Data Sheet”. Details on the Patch module and the Special Function ROM are found in the document “CDC32xxG-C V2.0 Hardware Manual and CDC3205G-C Data Sheet”.

1.1. Features

Table 1–1: CDC32xxG Family Feature List

				This Device:
Item	**CDC3205G-A EMU**	**CDC3205G-B EMU**	**CDC3207G-B MCM-Flash**	**CDC3272G-B Mask ROM**
Core				
CPU	32-Bit ARM7TDMI™			
CPU operation modes	DEEP SLOW, SLOW, FAST and PLL			
CPU clock multiplication	PLL delivering up to 24MHz	PLL delivering up to 50MHz		
EMI Reduction Mode	-	selectable in PLL mode		
Quartz oscillator	4 to 5MHz			
RAM, 32 Bit wide	16KByte	32KByte	32KByte	12KByte
ROM	ROMless, ext. up to 4M x 32/8M x 16, int. 8-KByte Boot ROM	ROMless, ext. up to 4M x 32/ 8M x 16, int. 8-KByte Boot ROM	512-KByte Flash (256K x 16) top boot conf., int. 8-KByte Boot ROM	384KByte (96K x 32/ 192K x 16), + 8-KByte Special Function ROM (SFR)
Digital Watchdog	✔			
Central Clock Divider	✔			
Interrupt Controller expanding IRQ	40 inputs,16 priority levels			
Port Interrupts including Slope Selection	6 inputs			
Patch Module	-			10 ROM locations
Boot System	allows in-system downloading of external code to Flash memory via JTAG			-

Table 1–1: CDC32xxG Family Feature List

	This Device:			
Item	**CDC3205G-A EMU**	**CDC3205G-B EMU**	**CDC3207G-B MCM-Flash**	**CDC3272G-B Mask ROM**
Analog				
Reset/Alarm	Combined Input for Regulator Input Supervision			
Clock and Supply Supervision	✔			
10-Bit ADC, charge balance type	16 channels (6 selectable as digital input)	16 channels (each selectable as digital input)		
ADC Reference	VREF Pin	VREF Pin, P1.0 Pin, P1.1 Pin or VREFINT Internal Bandgap selectable		
Comparators	P06COMP with 1/2 AVDD reference	P06COMP with 1/2 AVDD reference, WAITCOMP with Internal Bandgap reference		
LCD	Internal processing of all analog voltages for the LCD driver			
Communication				
DMA	1 DMA Channel for servicing a port or an SPI	3 DMA Channels, one each for servicing the Graphics Bus interface, SPI0 and SPI1		
UART	2: UART0 and UART1			
Synchronous Serial Peripheral Interfaces	2: SPI0 and SPI1			
Full CAN modules V2.0B	3: CAN0, CAN1 and CAN2 with 256bytes of object RAM each (LCAN0009)	3: CAN0, CAN1 and CAN2 with 512bytes of object RAM each (LCAN0009)		2: CAN0 and CAN1 with 512bytes of object RAM each (LCAN0009)
DIGITbus	1 master module			
I^2C	2 master modules: I2C0 and I2C1			
Input & Output				
Universal Ports selectable as 4:1 mux LCD Segment/Backplane lines or Digital I/O Ports	up to 54 I/O or 50 LCD segment lines (=200 segments)	up to 52 I/O or 48 LCD segment lines (=192 segments), individually configurable as I/O or LCD		
Universal Port Slew Rate	Mask selectable	SW selectable		
Stepper Motor Control Modules with high current ports	7 Modules, 32 dI/dt controlled ports			
PWM Modules, each configurable as two 8-bit PWMs or one 16-bit PWM	6 Modules: PWM0/1, PWM2/3, PWM4/5, PWM6/7, PWM8/9 and PWM10/11			
Phase-Frequency Modulator	-	1: PFM0		
Audio Module with auto-decay	✔			
SW selectable Clock outputs	2			

Table 1–1: CDC32xxG Family Feature List

	This Device:			
Item	**CDC3205G-A EMU**	**CDC3205G-B EMU**	**CDC3207G-B MCM-Flash**	**CDC3272G-B Mask ROM**
Timers & Counters				
16-bit free running counters with Capture/Compare modules	CCC0 with 4 CAPCOM CCC1 with 2 CAPCOM			
16-bit timers	1: T0			
8-bit timers	4: T1, T2, T3 and T4			
Miscellaneous				
Scalable layout in CAN, RAM and ROM	-		✔	
Various randomly selectable HW options	Set by copy from user program storage during system start-up			
JTAG test interface	✔		allows Flash programming	✔
On Chip Debug Aids	Embedded Trace Module, JTAG		JTAG	
Core Bond-Out	✔		-	
Supply Voltage	4.5 to 5.5V	3.5 to 5.5V (limited I/O performance below 4.5V)		
Case Temperature Range	-40 to +105C			
Package				
Type	Ceramic 257PGA		Plastic 128QFP 0.5mm pitch	
Bonded Pins	256		128	126

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1.2. Abbreviations

ADC	Analog-to-Digital Converter
AM	Audio Module
CAN	Controller Area Network Module
CAPCOM	Capture/Compare Module
CCC	Capture/Compare Counter
CPU	Central Processing Unit
DMA	Direct Memory Access Module
ERM	EMI Reduction Mode
ETM	Embedded Trace Module
ICU	Interrupt Controller
I2C	I^2C Interface Module
LCD	Liquid Crystal Display Module
P06COMP	P0.6 Alarm Comparator
PINT	Port Interrupt Module
PWM	Pulse Width Modulator Module
SM	Stepper Motor Control Module
SPI	Serial Synchronous Peripheral Interface
T	Timer
UART	Universal Asynchronous Receiver Transmitter
WAITCOMP	Wait Comparator

1.3. Block Diagram

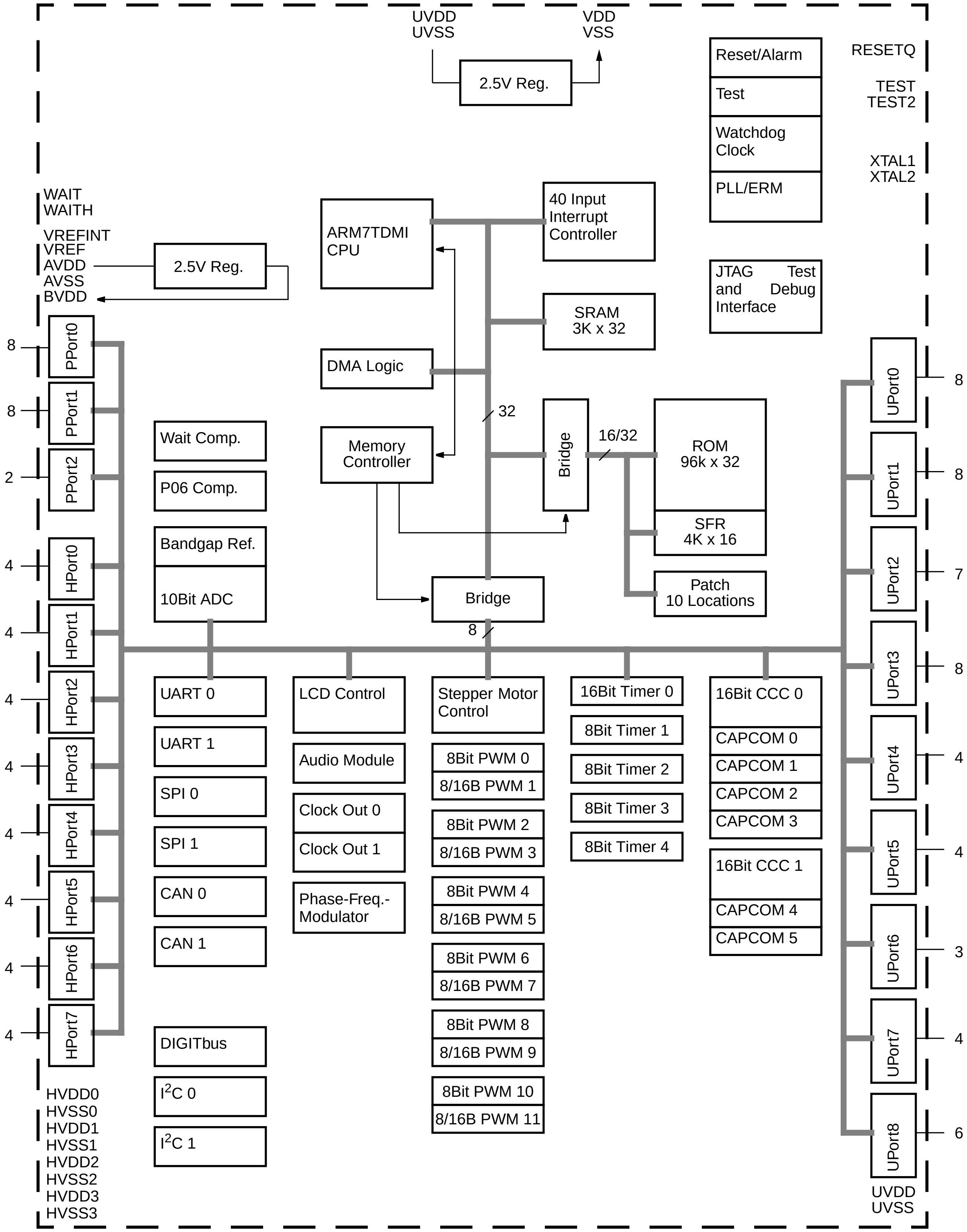


Fig. 1–1: CDC3272G-B block diagram

2. Packages and Pins

2.1. Package Outline Dimensions

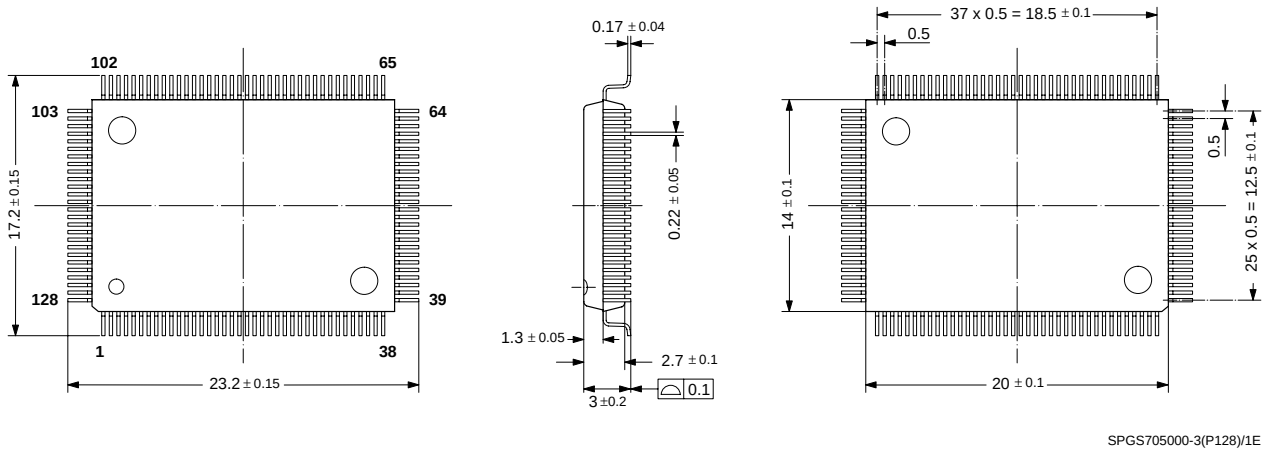
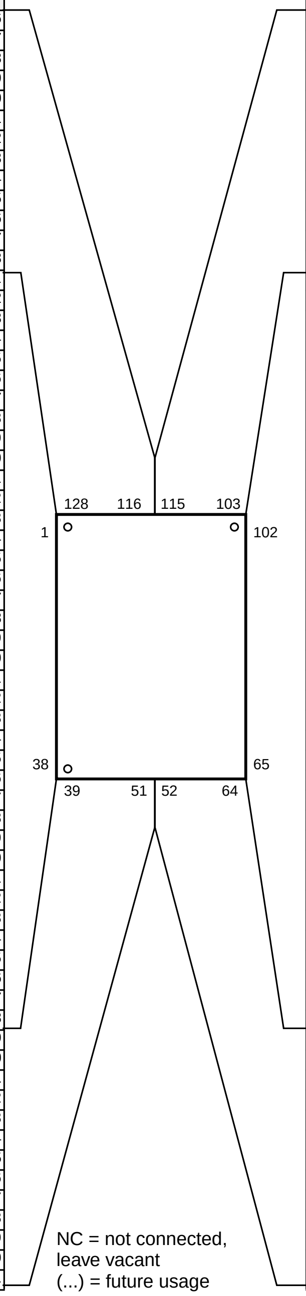


Fig. 2–1: PQFP128 Plastic Quad Flat Pack 128-Pin (Weight approx. 1.61g. Dimensions in mm)

2.2. Pin Assignment

LCD Mode	Port Special Out	Port Special In	Basic Function	Note	Pin No.
SEG3.1	CC1-OUT	CC1-IN / TMS	U3.1		116
SEG3.0	CC2-OUT	CC2-IN / TDI	U3.0		117
			TEST2		118
			UVDD		119
			UVSS		120
SEG2.6	DIGIT-OUT	DIGIT-IN	U2.6		121
SEG2.5	CC1-OUT	UART0-RX	U2.5		122
SEG2.4	UART0-TX	CC1-IN	U2.4		123
SEG2.3	CC2-OUT	UART1-RX	U2.3		124
SEG2.2	UART1-TX	CC2-IN	U2.2		125
SEG7.7	CO0		U7.7/GD7	1,2	126
SEG7.6	CO1		U7.6/GD6	1,2	127
SEG7.5	LCK(/PFM1)		U7.5/GD5	1,2	128
SEG7.4	CC5-OUT	CC5-IN	U7.4/GD4	1,2	1
			NC	1,2	2
			NC	1,2	3
SEG5.3	CC4-OUT	CC4-IN	U5.3/GD3	1	4
SEG5.2	SDA1	SDA1	U5.2/GD2	1	5
SEG5.1	SCL1	SCL1	U5.1/GD1	1	6
SEG5.0	PFM0		U5.0/GD0	1	7
SEG2.1	SDA0	SDA0/CAN0-RX	U2.1		8
SEG2.0	SCL0/CAN0-TX	SCL0	U2.0		9
SEG1.7	PFM0	PINT0	U1.7		10
SEG1.6	INTRES/CO0	PINT1	U1.6		11
SEG1.5	CO1/CO0Q	PINT2	U1.5		12
			TEST		13
			RESETQ/ALARMQ		14
			XTAL2		15
			XTAL1		16
			VSS		17
			VDD		18
SEG1.4	ITSTOUT/AM-OUT		U1.4		19
SEG1.3	MTO/AM-PWM		U1.3		20
SEG1.2	INTRES/T0-OUT	MTI/ITSTIN	U1.2		21
SEG1.1	T1-OUT		U1.1		22
SEG1.0	T2-OUT		U1.0		23
SEG0.7	T3-OUT		U0.7		24
SEG0.6	CC3-OUT/T4-OUT	CC3-IN	U0.6		25
SEG0.5	CC3-OUT	PINT4	U0.5		26
SEG0.4	CO1	PINT5	U0.4		27
SEG0.3	PWM0		U0.3		28
SEG0.2	PWM1		U0.2		29
SEG0.1	PWM2		U0.1		30
SEG0.0	PWM3		U0.0		31
	SME1+/PWM4		H7.3	1	32
	SME1-/PWM6		H7.2	1	33
	SME2+/PWM8		H7.1	1	34
	SME2-/PWM9	SME-COMP	H7.0	1	35
			HVDD2	1,2	36
			HVSS2	1,2	37
	PWM8		H6.3	1,2	38
	PWM9		H6.2	1,2	39
	PWM10		H6.1	1,2	40
	PWM11		H6.0	1,2	41
	SMD1+		H5.3		42
	SMD1-		H5.2		43
			HVDD0		44
			HVSS0		45
	SMD2+		H5.1		46
	SMD2-	SMD-COMP	H5.0		47
	SMA1+		H4.3		48
	SMA1-		H4.2		49
	SMA2+		H4.1		50
	SMA2-	SMA-COMP	H4.0		51



NC = not connected, leave vacant
(...) = future usage

Pin No.	Note	Basic Function	Port Special In	Port Special Out	LCD Mode
115		U3.2	CC0-IN / TCK	CC0-OUT	SEG3.2
114		U3.3		CO0/TDO	SEG3.3
113		U3.4	SPI0-CLK-IN	SPI0-CLK-OUT	SEG3.4
112		U3.5	SPI0-D-IN	TO3	SEG3.5
111		U3.6		SPI0-D-OUT	SEG3.6
110		U3.7	SPI1-CLK-IN	SPI1-CLK-OUT	SEG3.7
109		U4.0	SPI1-D-IN	CC0-OUT	BP0
108		U4.1	CC0-IN	SPI1-D-OUT	BP1
107		U4.2		CAN0-TX	BP2
106		U4.3	CAN0-RX	TO2	BP3
105	1,2	U8.0		CC4-OUT	SEG8.0
104	1,2	U8.1		CC3-OUT	SEG8.1
103	1,2	U8.2	LCD-CLK-IN		SEG8.2
102	1,2	U8.3		LCD-CLK-OUT	SEG8.3
101	1,2	U8.4	LCD-SYNC-IN		SEG8.4
100	1,2	U8.5	PINT3	LCD-SYNC-OUT	SEG8.5
99	1	U6.0		CAN1-TX	SEG6.0
98	1	U6.1	CAN1-RX	GOEQ	SEG6.1
97	1	U6.2		GWEQ	SEG6.2
96	1	P2.0			
95		P2.1			
94		P0.0	CC4-IN		
93		P0.1			
92		P0.2			
91		P0.3			
90		P0.4			
89		P0.5			
88		P0.6	P0.6 Comp.		
87		P0.7			
86		WAITH			
85		WAIT			
84		BVDD			
83		AVSS			
82		AVDD			
81		VREFINT			
80		VREF			
79		P1.0	VREF0		
78		P1.1	VREF1		
77		P1.2	PINT0		
76		P1.3	PINT1		
75		P1.4	PINT2		
74		P1.5	PINT3		
73		P1.6	PINT4		
72		P1.7	PINT5		
71	1	H0.0	SMG-COMP	SMG2-/PWM7	
70	1	H0.1		SMG2+/PWM5	
69	1	H0.2		SMG1-/PWM3	
68	1	H0.3		SMG1+/PWM1	
67	1,2	HVSS3			
66	1,2	HVDD3			
65	1,2	H1.0	SMF-COMP	SMF2-	
64	1,2	H1.1		SMF2+	
63	1,2	H1.2		SMF1-	
62	1,2	H1.3		SMF1+	
61		H2.0	SMC-COMP	SMC2-	
60		H2.1		SMC2+	
59		HVSS1			
58		HVDD1			
57		H2.2		SMC1-	
56		H2.3		SMC1+	
55		H3.0	SMB-COMP	SMB2-	
54		H3.1		SMB2+	
53		H3.2		SMB1-	
52		H3.3		SMB1+	

Fig. 2–2: Pin Assignment
Note 1 denotes pins that are not available in future 88 pin ROM parts.
Note 2 denotes pins that are not available in future 104 pin ROM parts.

2.3. External Components

To provide effective decoupling and to improve EMC behavior, the small decoupling capacitors must be located as close to the supply pins as possible. The self-inductance of these capacitors and the parasitic inductance and capacitance of the interconnecting traces determine the self-resonant frequency of the decoupling network. Too low a frequency will reduce decoupling effectiveness, will increase RF emissions and may adversely affect device operation.

XTAL1 and XTAL2 quartz connections are especially sensitive to capacitive coupling from other pc board signals. It is strongly recommended to place quartz and oscillation capacitors as close to the pins as possible and to shield the XTAL1 and XTAL2 traces from other signals by embedding them in a VSS trace.

The RESETQ pin adjacent to XTAL2 should be supplied with a small capacitor, to prevent fast RESETQ transients from being coupled into XTAL2, and to prevent XTAL2 from coupling into RESETQ.

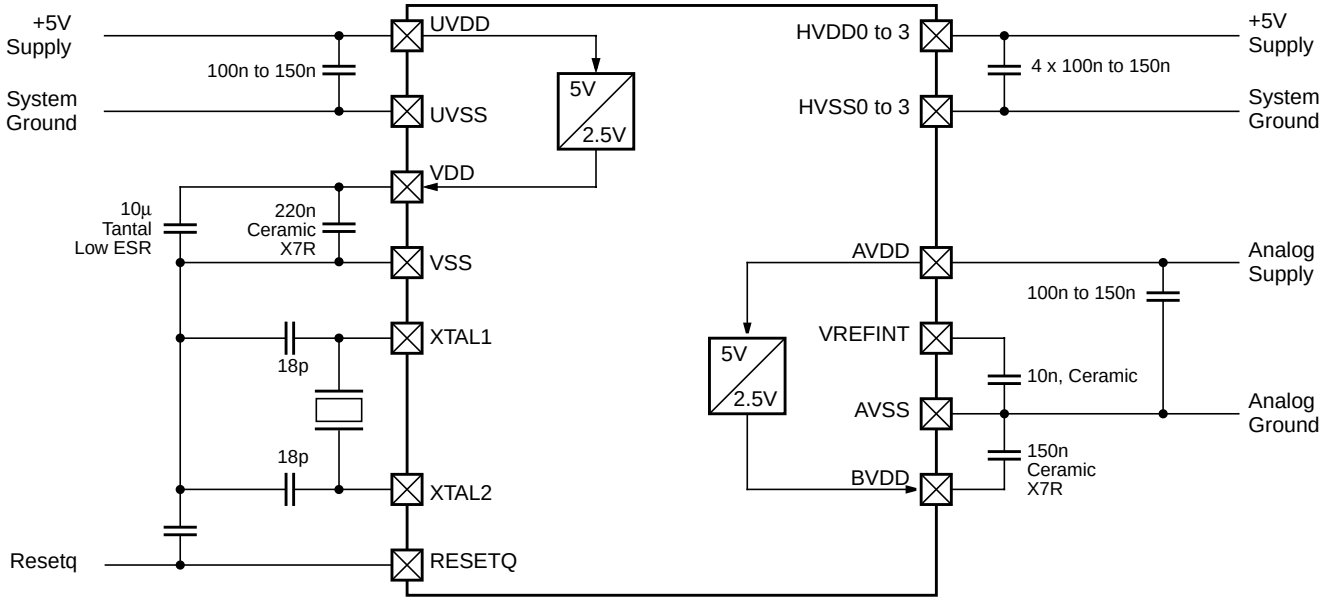


Fig. 2–3: CDC3272G-B: Recommended external supply and quartz connection

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Table 3–1: $UV_{SS}=HV_{SSn}=AV_{SS}=0V$

Symbol	Parameter	Pin Name	Min.	Max.	Unit
V_{SUP}	Main Supply Voltage Analog Supply Voltage SM Supply Voltage	UVDD AVDD HVDD0 .. HVDD3	-0.3	6.0	V
V_{EXT}	External Core Supply Voltage External Regulated Analog Supply Voltage	VDD BVDD	-0.3	3.0	V
I_{SUP}	Core Supply Current Main Supply Current	VDD, VSS, UVDD, UVSS	-100	100	mA
	Analog Supply Current	AVDD, AVSS	-20	20	mA
	SM Supply Current @T_j=105C, Duty Factor=0.71 [1])	HVDD0 .. HVDD3 HVSS0 .. HVSS3	-250	250	mA
	BVDD Regulator Output Current	BVDD	-20	20	mA
V_{in}	Input Voltage	U-Ports, XTAL,RESETQ, TEST, TEST2	UV_{SS}-0.5	UV_{DD}+0.7	V
		P-Ports VREF	UV_{SS}-0.5	AV_{DD}+0.7	V
		H-Ports	HV_{SS}-0.5	HV_{DD}+0.7	V
I_{in}	Input Current	all Inputs	0	2	mA
I_o	Output Current	U-Ports, RESETQ, WAITH	-5	5	mA
		H-Ports	-60	60	mA
t_{oshsl}	Duration of Short Circuit to UVSS or UVDD, Port SLOW Mode enabled	U-Ports, except in DP Mode		indefinite	s
T_j	Junction Temperature under Bias		-45	115	°C
T_s	Storage Temperature		-45	125	°C
P_{max}	Maximum Power Dissipation			0.8	W

[1]) This condition represents the worst case load with regard to the intended application

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.2. Recommended Operating Conditions

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

Keep UV_{DD}=AV_{DD} during all power-up and power-down sequences.

Failure to comply with the above recommendations will result in unpredictable behavior of the device and may result in device destruction**.**

Table 3–2: UV_{SS}=HV_{SSn}=AV_{SS}=0V

Symbol	Parameter	Pin Name	Min.	Typ	Max.	Unit
V_{SUP}	Main Supply Voltage Analog Supply Voltage	UV_{DD} AV_{DD}	3.5	5	5.5	V
HV_{SUP}	SM Supply Voltage	HV_{DDn}	4.75	5	5.25	V
dV_{DD}	Ripple, Peak to Peak	UV_{DD} AV_{DD} BV_{DD} V_{DD}			200	mV
dV_{DD}/dt	Supply Voltage Up/Down Ramping Rate	UV_{DD} AV_{DD}			20	V/µs
f_{XTAL}	XTAL Clock Frequency	XTAL1	4		5	MHz
f_{SYS}	CPU Clock Frequency, PLL on		For a list of available settings see Tables 4–1 and 4–2.			
f_{BUS}	Program Storage Clock Frequency, PLL on					
V_{il} (see Table 2-2 for a list of input types and their supply voltages)	Automotive Low Input Voltage	U-Ports H-Ports P-Ports			$0.5*xV_{DD}$	V
	CMOS Low Input Voltage	U-Ports, TEST, TEST2 H-Ports P-Ports			$0.3*xV_{DD}$	V
V_{ih} (see Table 2-2 for a list of input types and their supply voltages)	Automotive High Input Voltage	U-Ports H-Ports P-Ports	$0.86*xV_{DD}$			V
	CMOS High Input Voltage	U-Ports,TEST, TEST2 H-Ports P-Ports	$0.7*xV_{DD}$			V
RV_{il}	Reset Active Input Voltage	RESETQ			0.75	V
RV_{im}	Reset Inactive and Alarm Active Input Voltage	RESETQ	1.5		2.3	V
RV_{ih}	Reset Inactive and Alarm Inactive Input Voltage	RESETQ	3.2			V
V_{REFi}	Ext. ADC Reference Input Voltage	VREF	2.56		AV_{DD}	V
PV_i	ADC Port Input Voltage referenced to int. VREF Reference ADC Port Input Voltage referenced to ext. VREFINT Reference	P-Ports	0 0		V_{REFi} V_{REFINT}	V
Clock Input from External Generator						
XV_{il}	Clock Input Low Voltage	XTAL1			$0.2*V_{DD}$	V

Table 3–2: $UV_{SS}=HV_{SSn}=AV_{SS}=0V$

Symbol	Parameter	Pin Name	Min.	Typ	Max.	Unit
XV_{ih}	Clock Input High Voltage	XTAL1	$0.8*V_{DD}$			V
D_{XTAL}	Clock Input High to Low Ratio	XTAL1	0.45		0.55	

3.3. Characteristics

Listed are only those characteristics that are differing from Chapter 3.3 of Document “CDC32xxG-B V3.0, Automotive Controller Hardware Manual, CDC3205G-B EMU Data Sheet”

Table 3–3: $UV_{SS}=HV_{SSn}=AV_{SS}=0V$, $3.5V<AV_{DD}=UV_{DD}<5.5V$, $4.75V<HV_{DDn}<5.25V$, T_{CASE}=-40 to +105C, f_{XTAL}=5MHz, external components according to Fig. 2–3

Symbol	Parameter	Pin Na.	Min.	Typ.	Max.	Unit	Test Conditions
Package							
R_{thjc}	Thermal Resistance from Junction to Case			6		C/W	
R_{thja}	Thermal Resistance from Junction to Ambient			50		C/W	
Supply Currents (CMOS levels on all inputs, no loads on outputs)							
UI_{DDp}	UVDD PLL Mode Supply Current	UVDD			35	mA	CPU PLL Mode ON, Flash Read, f_{SYS}=24MHz
UI_{DDf}	UVDD FAST Mode Supply Current	UVDD			12	mA	CPU FAST Mode ON, all Modules OFF, [2])
UI_{DDs}	UVDD SLOW Mode Supply Current	UVDD			1.0	mA	CPU SLOW Mode ON, all Modules OFF, [2])
UI_{DDd}	UVDD DEEP SLOW Mode Supply Current	UVDD			0.7	mA	CPU DEEP SLOW Mode ON, all Modules OFF
		UVDD			1.0	mA	CPU DEEP SLOW Mode ON, only LCD Module ON
AI_{DDa}	AVDD Active Supply Current	AVDD		0.3	0.5	mA	ADC ON, Buffer and PLL OFF
				0.35	0.6	mA	ADC and Buffer ON, PLL OFF
				1	2	mA	ADC, Buffer and PLL ON, f_{SYS}=24MHz
AI_{DDq}	Quiescent Supply Current	AVDD			10	uA	ADC and PLL OFF
HI_{DDq}		Sum of all HVDDn			50	uA	no Output Activity, SM Module OFF

[2]) Value may be exceeded with unusual Hardware Option setting

3.4. Recommended Quartz Crystal Characteristics

See Chapter 3.4 of document “CDC32xxG-B V3.0, Automotive Controller Hardware Manual, CDC3205G-B EMU Data Sheet”.

4. CPU and Clock System

4.1. Recommended Register Settings

Other settings for PMF, IOP and WSR than those given in Tables 4–1 and 4–2 shall not be used and may result in undefined behaviour. It is required not to operate I/O faster than Flash.

Suppression Strength (SUP) and Clock Tolerance (TOL) may be varied between zero and the values for strong settings according to the rules in Section 4.4.2 of the CDC32xxG-B Hardware Manual. The given limits must not be exceeded.

Table 4–1: PLL and ERM Modes: Recommended Settings and Resulting Operating Frequencies (MHz)

f_{XTAL}	CPU		ROM		I/O		ERMC.EOM = 1						ERMC.EOM = 2 or 3					
							Weak		Normal		Strong		Weak		Normal		Strong	
	f_{SYS}	PLLC. PMF	f_{BUS}	WSR	f_{IO}= f_0	IOC. IOP	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL
4	8	1	8	0x00	8	0	0	4	0	7	0	11	4	2	7	4	11	6
	16	3	8	0x11	8	1	0	8	0	14	0	15	8	4	14	7	22	11
	24	5	8	0x22	8	2	0	12	0	15	0	15	12	6	21	11	31	12
			12	0x11			0	10	0	10	0	10	12	2	21	2	33	2
	32	7	8	0x33	8	3	0	12	0	12	0	12	16	8	28	12	31	12
			10.67	0x22			0	12	0	12	0	12	16	8	19 23 28	9 7 6	19 23 37	9 7 6
5	10	1	10	0x00	10	0	0	5	0	8	0	14	5	3	8	4	14	7
	20	3	10	0x11	10	1	0	10	0	15	0	15	10	5	17	8	28	8
	30	5	10	0x22	10	2	0	14	0	14	0	14	15	8	24 26	12 11	28 30 35	10 9 8

Table 4–2: PLL2 and ERM Modes: Settings Sacrificing Unlimited Operation of Peripheral Modules and Resulting Operating Frequencies (MHz)

f_{XTAL}	CPU		ROM		I/O		ERMC.EOM = 1						ERMC.EOM = 2 or 3					
							Weak		Normal		Strong		Weak		Normal		Strong	
	f_{SYS}	PLLC. PMF	f_{BUS}	WSR	f_{IO}= f_0	IOC. IOP	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL
4	12	2	6	0x11	4	2	0	6	0	10	0	15	6	3	10	5	16	8
			12	0x00			0	5	0	5	0	5	6	2	10	2	16	2
	20	4	10	0x11	4	4	0	10	0	15	0	15	10	5	17	8	28	8
5	15	2	7.5	0x11	5	2	0	7	0	13	0	15	7	4	13	7	21	11

5. Memory and Boot System

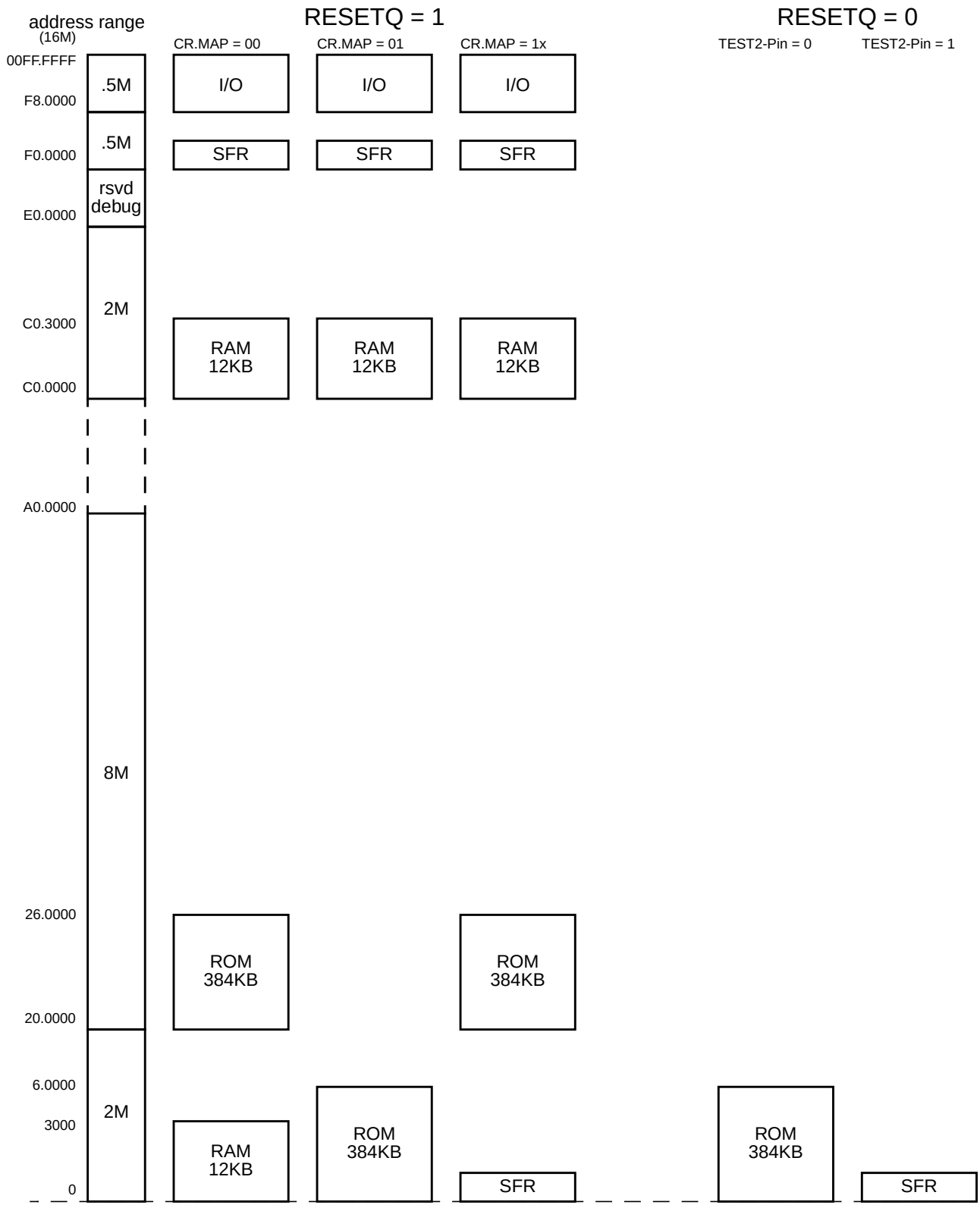


Fig. 5–1: Address Map. Most Common Settings

6. Core Logic

6.1. Control Word CW

Some system configuration items are freely selectable during device start-up by means of a unique Control Word (CW).

6.1.1. Reset Active

During Reset, the device fetches this CW from address locations 0x20 to 0x23 of a source that is determined by the state of pins TEST and TEST2, see Table 6–1 for MCM and ROM parts.

Table 6–1: CW fetch in MCM and ROM parts (QFP128)

Control Word Fetch desired from	Necessary Reset config. of pins	
	TEST2	TEST
Internal ROM/Flash	0	0
External via Multi Function port	0	1
Internal Special Function ROM 1)	1	x
1) Details on the Special Function ROM are found in the document “CDC32xxG-C V2.0 Hardware Manual and CDC3205G-C Data Sheet”.		

6.1.2. Reset Inactive

When exiting Reset, the CW is loaded into the Control Register (CR) and the system will start up according to the configuration defined therein.

Normally the CW is fetched from the same memory that the system will later start executing code from. Table 6–2 gives fix CWs for a list of the most commonly used configurations.

Table 6–2: Some common system configurations and the corresponding CW setting

Part Type	Program Start desired from	Additional desired properties	Necessary CW	
			31:16	15:0
MCM	int. 16-Bit Flash (Am29LV400BT)	-	Don’t care	0x7F5F
ROM	int. 32-Bit ROM, 16-Bit mode	-	Don’t care	0x7F5F
ROM	int. 32-Bit ROM, 32-Bit mode	-	0xFFBA	0x775F

7. Hardware Options

7.1. Functional Description

Hardware Options are available in several areas to adapt the IC function to the host system requirements. For details see the CDC32xxG-B Hardware Manual.

Hardware Option setting requires two steps:

1. selection is done by programming dedicated address locations in the HW Options field with the desired options' code.

2. activation is done by copying the HW Options field to the corresponding HW Options registers at least once after each reset.

All HW Options except those exempted in table 7–1 are SW progammable.

Table 7–1: Port, Clock and CM Option Programmability

IC Type	IC Name	Clock Opt.	CM.WCM setting
MCM	CDC3207G-B	SW	hard wired to 0
Mask ROM	CDC3272G-B	SW	
	Future ROM Parts	mask	

In future mask ROM derivatives the clock options and the Watchdog, Clock and Supply Monitors may be hard wired according to the HW Options field of the ROM code hex file. Those options can only be altered by changing production masks.

To ensure compatible option settings among EMU/MCM and mask ROM derivatives when run with the same ROM code, it is mandatory to always write the HW Options field to the HW option registers directly after reset.

8. Register Cross Reference Table

8.1. 8 Bit I/O Region

Table 8–1: Base address 0x00F80000

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0xFFC					6 CAN reserved	CAN RAM
0x400						
0x3FC					CAN 1	
0x200						
0x1FC					CAN 0	
0x000						

Table 8–2: Base address 0x00F81000

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x1FC					6 CAN reserved	CAN register
0x080						
0x07C					CAN1	
0x054						
0x050				CTIM		
0x04C	CTIM	REC	TEC	OCR		
0x048	ICR	BT3	BT2	BT1		
0x044	IDM					
0x040	IDX	ESTR	STR	CTR		
0x03C					CAN0	
0x014						
0x010				CTIM		
0x00C	CTIM	REC	TEC	OCR		
0x008	ICR	BT3	BT2	BT1		
0x004	IDM					
0x000	IDX	ESTR	STR	CTR		

Table 8–3: Base address 0x00F90000 (formerly 1F00)

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC	TST2	TST1	TST3	TST4		Test
0x0F8	TST5		TSTAD3	TSTAD2		
0x0F4	DGRTMA	DGTD	DGS1TA	DGTL		DIGITBus
0x0F0	DGRTMD	DGS0	DGC1	DGC0		
0x0EC					64 byte	
0x0B0						
0x0AC				ANAA		ADC
0x0A8			AD1	AD0		
0x0A4		UA0IF	UA0CA	UA0IM		UART0
0x0A0	UA0BR1	UA0BR0	UA0C	UA0D		
0x09C					32 byte	
0x080						
0x07C			CCC0H	CCC0L		CAPCOM0
0x078	CC3H	CC3L	CC3I	CC3M	CC3	
0x074	CC2H	CC2L	CC2I	CC2M	CC2	
0x070	CC1H	CC1L	CC1I	CC1M	CC1	
0x06C	CC0H	CC0L	CC0I	CC0M	CC0	
0x068					8 byte	
0x064						
0x060				CSW1		Core Logic
0x05C			SMVCMP	SMVCOS		Stepper Motor Module VDO
0x058	SMVSIN	SMVC				
0x054	TIM4	TIM3	TIM2	TIM1		Timer
0x050						
0x04C	TIM0H	TIM0L			Timer0	
0x048			CCC1H	CCC1L		CAPCOM1
0x044	CC5H	CC5L	CC5I	CC5M	CC5	
0x040	CC4H	CC4L	CC4I	CC4M	CC4	
0x03C					16 byte	
0x030						
0x02C	AMDEC	AMF	AMAS	AMPRE		Audio Module
0x028	IRPM1	IRPM0				Port Interrupt
0x024					8 byte	
0x020						
0x01C		UA1IF	UA1CA	UA1IM		UART1
0x018	UA1BR1	UA1BR0	UA1C	UA1D		
0x014				CO0SEL		Core Logic
0x010	SPI1M	SPI1D	SPI0M	SPI0D		SPI
0x00C	SR1					Core Logic
0x008	SR0					
0x004				ANAU		
0x000				CSW0		

Table 8–4: Base address 0x00F90100 (formerly 1E00)

Offs.	Byte Address				Remarks	
	3	**2**	**1**	**0**		**Module**
0x0FC					16 byte	HW Options
0x0F0						
0x0EC			UA1	UA0		
0x0E8		CM	PM			
0x0E4						
0x0E0						
0x0DC	P7P	P7C	P5P	P5C		
0x0D8	P3P	P3C	P1P	P1C		
0x0D4	P11P	P11C	P9P	P9C		
0x0D0	SP2C	SP1C	SP0C	SMC		
0x0CC	PF0C	AC	LC	DC		
0x0C8	C1C	C0C	CO1C	DMAC		
0x0C4	CO02C	CO01C	CO00C	T4C		
0x0C0	T3C	T2C	T1C	T0C		
0x0BC					96 byte	
0x060						
0x05C						PFM
0x054						
0x050	PFM0					
0x04C	PWMC					PWM
0x048	PWM11	PWM10	PWM9	PWM8		
0x044	PWM7	PWM6	PWM5	PWM4		
0x040	PWM3	PWM2	PWM1	PWM0		
0x03C					32 byte	
0x020						
0x01C					I2C1	I2C
0x018	I2CM1					
0x014	I2CRS1	I2CRD1	I2CWP11	I2CWP01		
0x010	I2CWD11	I2CWD01	I2CWS11	I2CWS01		
0x00C					I2C0	
0x008	I2CM0					
0x004	I2CRS0	I2CRD0	I2CWP10	I2CWP00		
0x000	I2CWD10	I2CWD00	I2CWS10	I2CWS00		

Table 8–5: Base address 0x00F90400

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC				HxPIN	H-Port7	H-Ports
0x0F8	HxLVL	HxNS	HxTRI	HxD		
0x0F4				HxPIN	H-Port6	
0x0F0	HxLVL	HxNS	HxTRI	HxD		
0x0EC				HxPIN	H-Port5	
0x0E8	HxLVL	HxNS	HxTRI	HxD		
0x0E4				HxPIN	H-Port4	
0x0E0	HxLVL	HxNS	HxTRI	HxD		
0x0DC				HxPIN	H-Port3	
0x0D8	HxLVL	HxNS	HxTRI	HxD		
0x0D4				HxPIN	H-Port2	
0x0D0	HxLVL	HxNS	HxTRI	HxD		
0x0CC				HxPIN	H-Port1	
0x0C8	HxLVL	HxNS	HxTRI	HxD		
0x0C4				HxPIN	H-Port0	
0x0C0	HxLVL	HxNS	HxTRI	HxD		
0x0BC						P-Ports
0x0B8	P2LVL		P2IE	P2PIN	P-Port 2	
0x0B4	P1LVL		P1IE	P1PIN	P-Port1	
0x0B0	P0LVL		P0IE	P0PIN	P-Port 0	
0x0AC					reserved	U-Ports
0x090						
0x084	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 8	
0x080	UxDPM	UxNS	UxTRI	UxD		
0x074	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 7	
0x070	UxDPM	UxNS	UxTRI	UxD		
0x064	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 6	
0x060	UxDPM	UxNS	UxTRI	UxD		
0x054	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 5	
0x050	UxDPM	UxNS	UxTRI	UxD		
0x044	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 4	
0x040	UxDPM	UxNS	UxTRI	UxD		
0x034	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 3	
0x030	UxDPM	UxNS	UxTRI	UxD		
0x024	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 2	
0x020	UxDPM	UxNS	UxTRI	UxD		
0x014	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 1	
0x010	UxDPM	UxNS	UxTRI	UxD		
0x004	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 0	
0x000	UxDPM	UxNS	UxTRI	UxD		

Table 8–6: Base address 0x00F90500

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					180 Bytes	reserved
0x050						
0x04C					reserved	GBus
0x048						
0x044				GC		
0x040				GD		
0x03C					reserved	Core Logic
0x030						
0x02C				WSR	Clock, PLL, ERM	
0x028				IOC		
0x024	ERMC					
0x020				PLLC		
0x01C					reserved	LCD
0x014						
0x010				ULCDLD		
0x00C						Patch
0x008	PER					
0x004	PDR					
0x000	PAR					

8.2. 32 Bit I/O Region

Table 8–7: Base address 0x00FFFD00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					252 bytes reserved	Core Logic
0x004						
0x000	CR				Control Register	

Table 8–8: Base address 0x00FFFE00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					rsvd Channel 4 to 31	DMA
0x020						
0x018			DC3M		Channel 3	
0x010			DC2M		Channel 2	
0x008			DC1M		Channel 1	
0x004				DST	Control	
0x000	DVB					

Table 8–9: Base address 0x00FFFF00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					12 bytes reserved	IRQ and FIQ Interrupt Controller
0x0F4						
0x0F0			CRF	PRF	FIQ registers	
0x0EC					40 bytes reserved	
0x0C8						
0x0C4	VTB				IRQ registers	
0x0C0	PESRC	PEPRIO	AFP	CRI		
0x0BC					128 bytes reserved	
0x040						
0x03C					Interrupt source nodes	
0x028						
0x024	ISN39	ISN38	ISN37	ISN36		
:	:	:	:	:		
0x004	ISN7	ISN6	ISN5	ISN4		
0x000	ISN3	ISN2	ISN1	ISN0		

8.3. Modified Registers

Listed are only those registers that are differing from Document “CDC32xxG-B V3.0, Automotive Controller Hardware Manual, CDC3205G-B EMU Data Sheet”

8.3.1. Standby Registers (cf. chapter 6.2 in Hardware Manual)

SR0 Standby Register 0

	7	6	5	4	3	2	1	0	Offs
r/w	I2C1	I2C0	x	x	x	x	x	CAN1	3
r/w	TIM2	TIM3	TIM4	UART1	x	DGB	CCC1	x	2
r/w	LCD	x	PSLW	UART0	ADC	x	TIM1	XTAL	1
r/w	SM	x	x	x	SPI1	CAN0	CCC0	SPI0	0
	0x00000100								Res

Standby Register 0 (SR0) flag CAN2 at byte offest 3, bit number 1 is not available in this part.

8.3.2. UVDD Analog Registers (cf. chapter 6.3.9 in Hardware Manual)

ANAU Analog UVDD Register

	7	6	5	4	3	2	1	0
r/w	EAL	x	LS		x	x	x	VE
	0		0	0			0	0

Analog UVDD Register flag FVE at bit number 1 is not available in this part.

9. Data Sheet History

1. Advance Information: “CDC3272G-B V1.0 Automotive Controller Specification”, 24 JUL 02, 6251-601-1AI.
First release of the advance information.
Originally created for HW version CDC3272G-B1.

Revision bars in this document denote changes against the prior document “CDC3207G-B V3.0 Automotive Controller Specification”, 3 DEC 01, 6251-578-1AI“.

Chapters only corrected and edited:

Chapters changed due to changed functionality:
1., 2., 3., 4., 5., 6.1., 7.
Chapters added:
8., 8.3

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