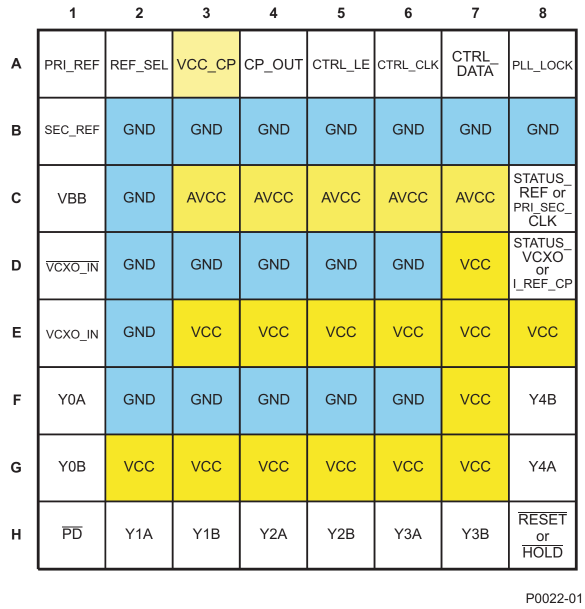
3.3-V HIGH PERFORMANCE CLOCK SYNCHRONIZER AND JITTER CLEANER

Check for Samples: CDCM7005

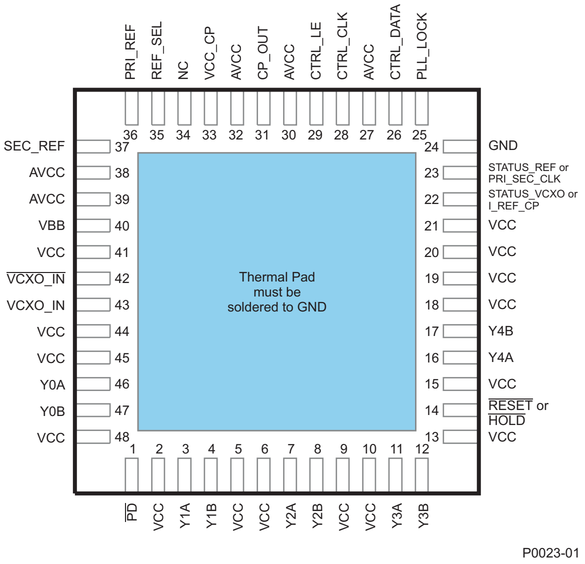
FEATURES

- High Performance LVPECL and LVCMOS PLL Clock Synchronizer
- Two Reference Clock Inputs (Primary and Secondary Clock) for Redundancy Support With Manual or Automatic Selection
- Accepts LVCMOS Input Frequencies Up to 200 MHz
- VCXO_IN Clock is Synchronized to One of the Two Reference Clocks
- VCXO_IN Frequencies Up to 2.2 GHz (LVPECL)
- Outputs Can Be a Combination of LVPECL and LVCMOS (Up to Five Differential LVPECL Outputs or Up to 10 LVCMOS Outputs)
- Output Frequency is Selectable by x1, /2, /3, /4, /6, /8, /16 on Each Output Individually
- Efficient Jitter Cleaning From Low PLL Loop Bandwidth
- Low Phase Noise PLL Core
- Programmable Phase Offset (PRI_REF and SEC_REF to Outputs)
- Wide Charge Pump Current Range From 200 µA to 3 mA
- Dedicated Charge Pump Supply (VCC_CP) for Wide Tuning Voltage Range VCOs
- Presets Charge Pump to VCC_CP/2 for Fast Center-Frequency Setting of VC(X)O
- Analog and Digital PLL Lock Indication
- Provides VBB Bias Voltage Output for Single-Ended Input Signals (VCXO_IN)
- Frequency Hold-Over Mode Improves Fail-Safe Operation
- Power-Up Control Forces LVPECL Outputs to 3-State at $V_{CC} < 1.5$ V
- SPI Controllable Device Setting
- 3.3-V Power Supply
- Packaged in 64-Pin BGA (0,8 mm Pitch – ZVA) or 48-Pin QFN (RGZ)
- Industrial Temperature Range –40°C to 85°C

PIN ASSIGNMENTS (TOP VIEW)



	1	2	3	4	5	6	7	8
A	PRI_REF	REF_SEL	VCC_CP	CP_OUT	CTRL_LE	CTRL_CLK	CTRL_ DATA	PLL_LOCK
B	SEC_REF	GND	GND	GND	GND	GND	GND	GND
C	VBB	GND	AVCC	AVCC	AVCC	AVCC	AVCC	STATUS_ REF or PRI_SEC_ CLK
D	$\overline{\text{VCXO\_IN}}$	GND	GND	GND	GND	GND	VCC	STATUS_ VCXO or I_REF_CP
E	VCXO_IN	GND	VCC	VCC	VCC	VCC	VCC	VCC
F	Y0A	GND	GND	GND	GND	GND	VCC	Y4B
G	Y0B	VCC	VCC	VCC	VCC	VCC	VCC	Y4A
H	$\overline{\text{PD}}$	Y1A	Y1B	Y2A	Y2B	Y3A	Y3B	$\overline{\text{RESET}}$ or $\overline{\text{HOLD}}$



DESCRIPTION

The CDCM7005 is a high-performance, low phase noise and low skew clock synchronizer that synchronizes a VCXO (voltage controlled crystal oscillator) or VCO (voltage controlled oscillator) frequency to one of the two reference clocks. The programmable pre-divider M and the feedback-dividers N and P give a high flexibility to the frequency ratio of the reference clock to VC(X)O:

- VC(X)O_IN / PRI_REF = (N x P) / M or
- VC(X)O_IN / SEC_REF = (N x P) / M

VC(X)O_IN clock operates up to 2.2 GHz. Through the selection of external VC(X)O and loop filter components, the PLL loop bandwidth and damping factor can be adjust to meet different system requirements.

The CDCM7005 can lock to one of two reference clock inputs (PRI_REF and SEC_REF), supports frequency hold-over mode and fast-frequency-locking for fail-safe and increased system redundancy. The outputs of the CDCM7005 are user definable and can be any combination of up to five LVPECL outputs or up to 10 LVCMOS outputs. The LVCMOS outputs are arranged in pairs (Y0A:Y0B, Y1A:Y1B, …), so that each pair has the same frequency. But each output can be separately inverted and disabled. The built in synchronization latches ensure that all outputs are synchronized for low output skew.

All device settings, like outputs signaling, divider value, input selection, and many more, are programmable by SPI (3-wire serial peripheral interface). SPI allows individually control of the device settings.

The device operates in 3.3-V environment and is characterized for operation from –40°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM

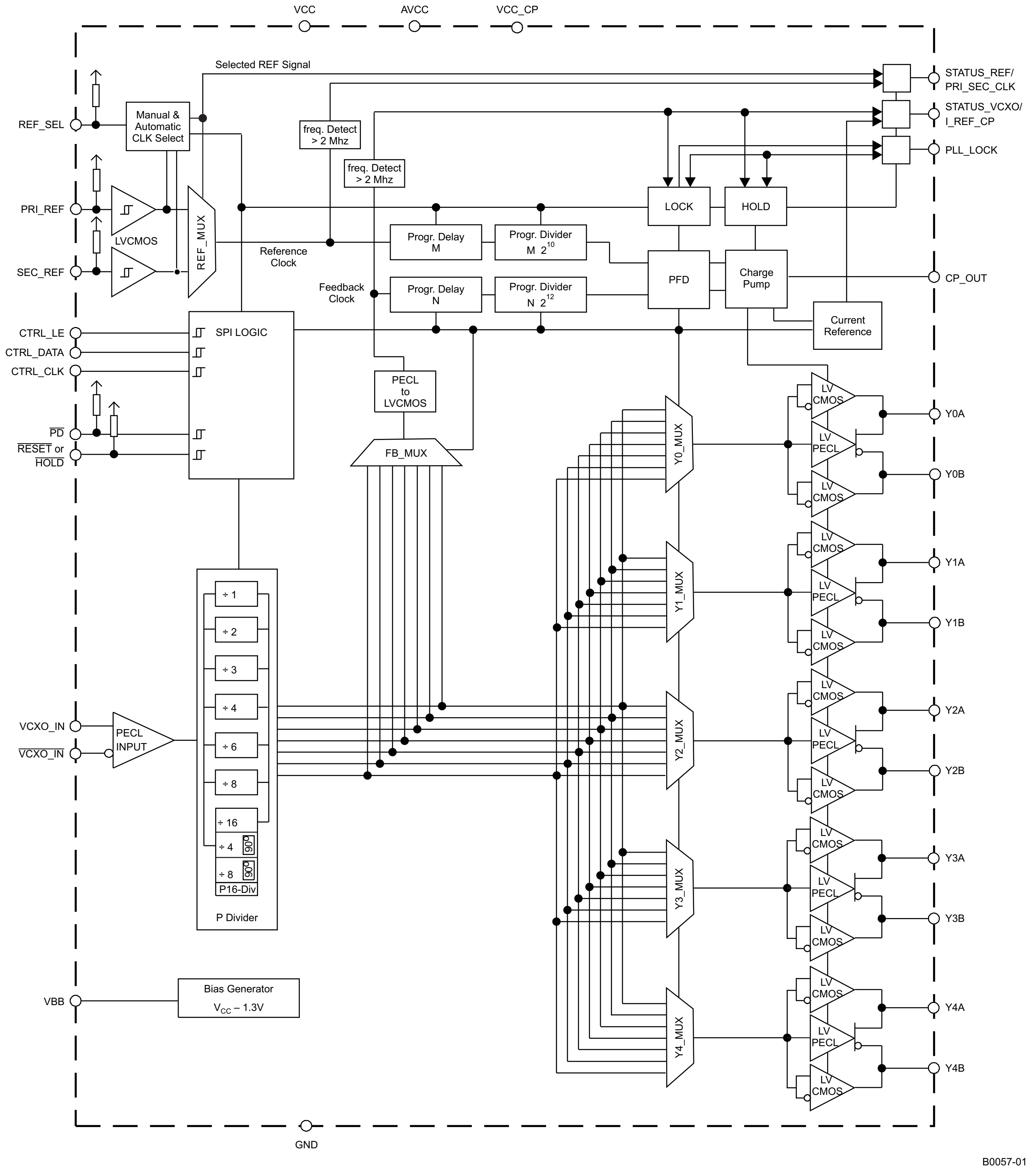


Table 1. PIN ASSIGNMENT

TERMINAL			I/O	DESCRIPTION
NAME	BGA	QFN		
VCC	D7, E3, E4, E5, E6, E7, E8, F7, G2, G3, G4, G5, G6, G7	2, 5, 6, 9, 10, 13, 15, 18, 19, 20, 21, 41, 44, 45; 48	Power	3.3-V supply. V_{CC} and AV_{CC} should always have the same supply voltage. It is recommended that AV_{CC} use its own supply filter.
GND	B2, B3, B4, B5, B6, B7, B8, C2, D2, D3, D4, D5, D6, E2, F2, F3, F4, F5, F6	Thermal pad and pin 24	Ground	Ground
AVCC	C3, C4, C5, C6, C7	27, 30, 32, 38, 39	Analog Power	3.3-V analog power supply. There is no internal connection between AV_{CC} and V_{CC}. It is recommended that AV_{CC} use its own supply filter.
VCC_CP	A3	33	Power	This is the charge pump power supply pin used to have the same supply as the external VCO. It can be set from 2.3 V to 3.6 V.
CTRL_LE	A5	29	I	LVCMOS input, control latch enable for serial programmable Interface (SPI), with hysteresis. Unused or floating inputs must be tied to proper logic level. A 20kΩ or larger pull−up resistor to VCC is recommended.
CTRL_CLK	A6	28	I	LVCMOS input, serial control clock input for SPI, with hysteresis. Unused or floating inputs must be tied to proper logic level. A 20kΩ or larger pull−up resistor to VCC is recommended.
CTRL_DATA	A7	26	I	LVCMOS input, serial control data input for SPI, with hysteresis. Unused or floating inputs must be tied to proper logic level. A 20kΩ or larger pull−up resistor to VCC is recommended.
$\overline{\text{PD}}$	H1	1	I	LVCMOS input, asynchronous power down ($\overline{\text{PD}}$) signal. This pin is low active and can be activated external or by the corresponding bit in the SPI register (in case of logic high, the SPI setting is valid). Switches the device into power-down mode. Resets M- and N-Divider, 3-states charge pump, STATUS_REF, or PRI_SEC_CLK pin, STATUS_VCXO or I_REF_CP pin, PLL_LOCK pin, VBB pin and all Yx outputs. Sets the SPI register to default value; has internal 150-kΩ pullup resistor. It is recommended to ramp up the $\overline{\text{PD}}$ with the same time as V_{CC} and AV_{CC} or later. The ramp up rate of the $\overline{\text{PD}}$ should not be faster than the ramp up rate of V_{CC} and AV_{CC}.
$\overline{\text{RESET}}$ or $\overline{\text{HOLD}}$	H8	14	I	This LVCMOS input can be programmed (SPI) to act as $\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ is the default function. This pin is low active and can be activated external or via the corresponding bit in the SPI register. In case of $\overline{\text{RESET}}$, the charge pump (CP) is switched to 3-state and all counters (N, M, P) are reset to zero (the initial divider settings are maintained in SPI registers). The LVPECL outputs are static low and high respectively and the LVCMOS outputs are all low or high if inverted. $\overline{\text{RESET}}$ is not edge triggered and should have a pulse duration of at least 5 ns. In case of $\overline{\text{HOLD}}$, the CP is switched in to 3-state mode only. After $\overline{\text{HOLD}}$ is released and with the next valid reference clock cycle the charge pump is switched back in to normal operation (CP stays in 3-state as long as no reference clock is valid). During $\overline{\text{HOLD}}$, the P divider and all outputs Yx are at normal operation. This mode allows an external control of the frequency hold-over mode. The input has an internal 150-kΩ pullup resistor.
VCXO_IN	E1	43	I	VCXO LVPECL input
$\overline{\text{VCXO\_IN}}$	D1	42	I	Complementary VCXO LVPECL input
PRI_REF	A1	36	I	LVCMOS input for the primary reference clock, with an internal 150-kΩ pullup resistor and input hysteresis.
SEC_REF	B1	37	I	LVCMOS input for the secondary reference clock, with an internal 150-kΩ pullup resistor and input hysteresis.

Table 1. PIN ASSINGMENT (continued)

TERMINAL			I/O	DESCRIPTION
NAME	**BGA**	**QFN**		
REF_SEL	A2	35	I	LVCMOS reference clock selection input. In the manual mode the REF_SEL signal selects one of the two input clocks: REF_SEL [1]: PRI_REF is selected; REF_SEL [0]: SEC_REF is selected; The input has an internal 150-kΩ pullup resistor.
CP_OUT	A4	31	O	Charge pump output
VBB	C1	40	O	Bias voltage output to be used to bias unused complementary input $\overline{\text{VCXO\_IN}}$ for single ended signals. The output of VBB is V_{CC} – 1.3 V. The output current is limited to about 1.5 mA.
STATUS_REF or PRI_SEC_CLK	C8	23	O	This output can be programmed (SPI) to provide either the STATUS_REF or PRI_SEC_CLK information. This pin is set high if one of the STATUS conditions is valid. STATUS_REF is the default setting. In case of STATUS_REF, the LVCMOS output provides the Status of the Reference Clock. If a reference clock with a frequency above 2 MHz is provided to PRI_REF or SEC_REF STATUS_REF will be set high. In case of PRI_SEC_CLK, the LVCMOS output indicates whether the primary clock [high] or the secondary clock [low] is selected.
STATUS_VCXO or I_REF_CP	D8	22	O	This LVCMOS output can be programmed (SPI) to provide either the STATUS_VCXO information or serve as current path for the charge pump (CP). STATUS_VCXO is the default setting. In case of STATUS_VCXO, the LVCMOS output provides the status of the VCXO input (frequencies above 2 MHz are interpreted as valid clock; active high). In case of I_REF_CP, it provides the current path for the external reference resistor (12 kΩ ±1%) to support an accurate charge pump current, optional. Do not use any capacitor across this resistor to prevent noise coupling via this node. If the internal 12 kΩ is selected (default setting), this pin can be left open.
PLL_LOCK	A8	25	I/O	LVCMOS output for PLL_LOCK information. This pin is set high if the PLL is in lock (see feature description). This output can be programmed to be digital lock detect or analog lock detect (see feature description). The PLL is locked (set high), if the rising edge either of PRI_REF or SEC_REF clock and VCXO_IN clock at the phase frequency detector (PFD) are inside the lock detect window for a predetermined number of successive clock cycles. The PLL is out-of-lock (set low), if the rising edge of either the PRI_REF or SEC_REF) clock and VCXO_IN clock at the PFD are outside the lock detect window or if a certain frequency offset between reference frequency and feedback frequency (VCXO) is detected. Both, the lock detect window and the number of successive clock cycles are user definable (via SPI).
Y0A:Y0B Y1A:Y1B Y2A:Y2B Y3A:Y3B Y4A:Y4B	F1, G1, H2, H3, H4, H5, H6, H7, G8, F8	46, 47, 3, 4, 7, 8, 11,12, 16, 17	O	The outputs of the CDCM7005 are user definable and can be any combination of up to five LVPECL outputs or up to 10 LVCMOS outputs. The outputs are selectable via SPI (Word 1, Bit 2-6). The power-up setting is all outputs are LVPECL.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE / UNIT
V_{CC}, AV_{CC}, V_{CC_CP}	Supply voltage range (2)	–0.5 V to 4.6 V
V_I	Input voltage range (3)	–0.5 V to V_{CC} + 0.5 V
V_O	Output voltage range (3)	–0.5 V to V_{CC} + 0.5 V
I_{OUT}	Output current for LVPECL/LVCMOS outputs ($0 < V_O < V_{CC}$)	±50 mA
I_{IN}	Input current ($V_I < 0$, $V_I > V_{CC}$)	±20 mA
T_{stg}	Storage temperature range	–65°C to 150°C
T_J	Maximum junction temperature	125°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All supply voltages have to be supplied at the same time.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Package Thermal Resistance for RGZ (QFN) Package(1) (2)

Airflow (lfm)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JP} (°C/W) (3)	ψ_{JT} (°C/W)
0	29.9	22.4	1.5	0.2
150	24.7			0.2
250	23.2			0.2
500	21.5			0.3

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) Connected to GND with nine thermal vias (0,3 mm diameter).
(3) θ_{JP} (junction pad) is used for the QFN package, because the main heat flow is from the junction to the GND pad of the QFN.

Package Thermal Resistance for ZVA (BGA) Package(1)

Airflow (m/s)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JB} (°C/W) (2)	ψ_{JT} (°C/W)
0 m/s	53.9	28.3	38.6	0.7
1 m/s	49.8			0.7
2 m/s	48.5			0.8

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) θ_{JB} (junction board) is used for the BGA package, because the main heat flow is from junction to the board.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}, AV_{CC}	Supply voltage	3	3.3	3.6	V
V_{CC_CP}		2.3		V_{CC}	
V_{IL}	Low-level input voltage LVCMOS, see (1)			0.3 V_{CC}	V
V_{IH}	High-level input voltage LVCMOS, see (1)	0.7 V_{CC}			V
I_{OH}	High-level output current LVCMOS (includes all status pins)			–8	mA
I_{OL}	Low-level output current LVCMOS (includes all status pins)			8	mA
V_I	Input voltage range LVCMOS	0		3.6	V
V_{INPP}	Input amplitude LVPECL ($V_{VCXO\_IN} - V_{\overline{VCXO\_IN}}$)(2)	0.5		1.3	V
V_{IC}	Common-mode input voltage LVPECL	1		V_{CC}–0.3	V
T_A	Operating free-air temperature	–40		85	°C

(1) V_{IL} and V_{IH} are required to maintain ac specifications; the actual device function tolerates a smaller input level of 1V, if an ac-coupling to $V_{CC}/2$ is provided.
(2) V_{INPP} minimum and maximum is required to maintain ac specifications; the actual device function tolerates at a minimum V_{INPP} of 150 mV.

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load and operating free air temperature

PARAMETER		MIN	TYP	MAX	UNIT
PRI_REF/SEC_REF_IN REQUIREMENTS					
f_{REF_IN}	LVCMOS primary or secondary reference clock frequency[1] [2]	0		200	MHz
t_r/ t_f	Rise and fall time of PRI_REF or SEC_REF signals from 20% to 80% of V_{CC}			4	ns
dutyREF	Duty cycle of PRI_REF or SEC_REF at $V_{CC}/2$	40%		60%	
VCXO_IN, $\overline{\text{VCXO\_IN}}$ REQUIREMENTS					
f_{VCXO_IN}	VCXO clock frequency[3]	0		2200	MHz
t_r/ t_f	Rise and fall time 20% to 80% of VINPP at 80 MHz to 800 MHz[4]			3	ns
dutyVCXO	Duty cycle of VCXO clock	40%		60%	
SPI/CONTROL REQUIREMENTS (see Figure 14)					
f_{CTRL_CLK}	CTRL_CLK frequency			20	MHz
t_{su1}	CTRL_DATA to CTRL_CLK setup time	10			ns
t_{h2}	CTRL_DATA to CTRL_CLK hold time	10			ns
t_3	CTRL_CLK high duration	25			ns
t_4	CTRL_CLK low duration	25			ns
t_{su5}	CTRL_LE to CTRL_CLK setup time	10			ns
t_{su6}	CTRL_CLK to CTRL_LE setup time	10			ns
t_7	CTRL_LE pulse width	20			ns
t_r/ t_f	Rise and fall time of CTRL_DATA CTRL_CLK, CTRL_LE from 20% to 80% of V_{CC}			4	ns
$\overline{\text{PD}}$, $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, REF_SEL REQUIREMENTS					
t_r / t_f	Rise and fall time of the PD, RESET, HOLD, REF_SEL signal from 20% to 80% of V_{CC}			4	ns

(1) At *Reference Clock* less than 2 MHz, the device stays in normal operation mode but the frequency detection circuitry resets the STATUS_REF signal to low. In this case, the status of the STATUS_REF is no longer relevant.
(2) f_{REF_IN} can be up to 250 MHz in typical operating mode (25°C / 3.3-V V_{CC}).
(3) If the *Feedback Clock* (derives from VCXO input) is less than 2 MHz, the device stays in normal operation mode but the frequency detection circuitry resets the STATUS_VCXO signal and PLL_LOCK signal to low. Both status signals are no longer relevant. This effects the HOLD-over function as well, as the PLL_LOCK signal is no longer valid!
(4) Use a square wave for lower frequencies (< 80 MHz).

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
I_{CC_LVPECL}	Supply current (I_{CC} over frequency see Figure 1 through Figure 4)	f_{VCXO} = 245.76 MHz, f_{REF_IN} = 30.72 MHz, PFD = 240 kHz, I_{CP} = 2 mA, all outputs are LVPECL and Div-by-8 (load, see Figure 13)		210	260	mA
I_{CC_LVCMOS}		f_{VCXO} = 245.76 MHz, f_{REF_IN} = 30.72 MHz, PFD = 240 kHz, I_{CP} = 2 mA, All outputs are LVCMOS and Div-by-8 (load, 10 pF)		120	150	mA
I_{CCPD}	Power-down current	f_{IN} = 0 MHz, V_{CC} = 3.6 V, AV_{CC} = 3.6 V, V_{CC_CP} = 3.6 V, V_I = 0 V or V_{CC}		100	300	μA
I_{OZ}	High-impedance state output current for Yx outputs	V_O = 0 V or V_{CC} – 0.8 V			±40	μA
		V_O = 0 V or V_{CC}			±100	μA
$V_{I\_REF\_CP}$	Voltage on I_REF_CP (external current path for accurate charge pump current)	12 kΩ to GND at pin D8 (BGA), pin 22 (QFN)		1.21		V
V_{BB}	Output reference voltage	V_{CC} = 3 V – 3.6 V; I_{BB} = –0.2 mA		V_{CC}–1.3		V
C_O	Output capacitance for Yx	V_{CC} = 3.3 V, V_O = 0 V or V_{CC}		2		pF
C_I	Input capacitance at PRI_REF and SEC_REF	V_I = 0 V or V_{CC}, V_I = 0 V or V_{CC}		2.7		pF
	Input capacitance at CTRL_LE, CTRL_CLOCK, CTRL_DATA	V_I = 0 V or V_{CC}		2		

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS						
f_{clk}	Output frequency, see [1], [2], Figure 6, and Figure 7	Load = 5 pF to GND, 1 kΩ to V_{CC}, 1 kΩ to GND			250	MHz
V_{IK}	LVCMOS input clamp voltage	V_{CC} = 3 V, I_I = –18 mA			–1.2	V
I_I	LVCMOS input current for CTRL_LE, CTRL_CLK, CTRL_DATA	V_I = 0 V or V_{CC}, V_{CC} = 3.6 V			±5	µA
I_{IH}	LVCMOS input current for $\overline{\text{PD}}$, $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, REF_SEL, PRI_REF, SEC_REF, (see [3])	V_I = V_{CC}, V_{CC} = 3.6 V			5	µA
I_{IL}	LVCMOS input current for $\overline{\text{PD}}$, $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, REF_SEL, PRI_REF, SEC_REF, (see [3])	V_I = 0 V, V_{CC} = 3.6 V	–15		–35	µA
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = min to max, I_{OH} = –100 µA	V_{CC}–0.1			V
		V_{CC} = 3 V, I_{OH} = –6 mA	2.4			
		V_{CC} = 3 V, I_{OH} = –12 mA	2			
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = min to max, I_{OL} = 100 µA			0.1	V
		V_{CC} = 3 V, I_{OL} = 6 mA			0.5	
		V_{CC} = 3 V, I_{OL} = 12 mA			0.8	
I_{OH}	High-level output current	V_{CC} = 3.3 V, V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V, V_O = 1.65 V		33		mA
tpho	Phase offset (REF_IN to Y output)[4]	VREF_IN = V_{CC}/2, Y = V_{CC}/2, see Figure 11, Load = 10 pF		1.8		ns
$t_{sk(p)}$	LVCMOS pulse skew, see Figure 10	Crosspoint to V_{CC}/2 load, see Figure 12			150	ps
$t_{pd(LH)}$ $t_{pd(HL)}$	Propagation delay from VCXO_IN to Yx, see Figure 10	Crosspoint to V_{CC}/2, Load = 10 pF, see Figure 12 (PLL bypass mode)	2	2.5	3	ns
$t_{sk(o)}$	LVCMOS single-ended output skew, see [5] and Figure 10	All outputs have the same divider ratio			55	ps
		Outputs have different divider ratios			70	
Duty cycle	LVCMOS	V_{CC}/2 to V_{CC}/2	49%		51%	
$t_{slew-rate}$	Output rise/fall slew rate	20% to 80% of swing (load see Figure 12)	2.4	3.5		V/ns
LVPECL						
f_{clk}	Output frequency, see [6] and Figure 5	Load, see Figure 13	0		1500	MHz
I_I	LVPECL input current	V_I = 0 V or V_{CC}			±20	µA
V_{OH}	LVPECL high-level output voltage	Load, See Figure 13	V_{CC}–1.18		V_{CC}–0.81	V
V_{OL}	LVPECL low-level output voltage	Load, See Figure 13	V_{CC}–2		V_{CC}–1.55	V
$\lvert V_{OD} \rvert$	Differential output voltage	See Figure 9 and load, see Figure 13	500			mV
t_{pho}	Phase offset (REF_IN to Y output)[5]	VREF_IN = V_{CC}/2 to cross point of Y, see Figure 11	–200		100	ps
$t_{pd(LH)}$ $t_{pd(HL)}$	Propagation delay time, VCXO_IN to Yx, see Figure 10	Cross point-to-cross point, load see Figure 13	340	490	640	ps
$t_{sk(p)}$	LVPECL pulse skew, see Figure 10	Cross point-to-cross point, load see Figure 13			10	ps

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(1) f_{clk} can be up to 400 MHz in the typical operating mode (25°C / 3.3-V V_{CC}). The total power consumption limit of 700 mW for the BGA package can be violated if several LVCMOS outputs switch at high frequency (see Figure 3 and Figure 4).

(2) Operating the LVCMOS or LVPECL output above the maximum frequency will not cause a malfunction to the device, but the output signal swing may no longer meet the output specification.

(3) These inputs have an internal 150-kΩ pullup resistor.

(4) This is valid only for the same frequency of REF_IN clock and Y output clock. It can be adjusted by the SPI controller (reference delay M and VCXO delay N).

(5) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

(6) Operating the LVCMOS or LVPECL output above the maximum frequency will not cause a malfunction to the device, but the output signal swing may no longer meet the output specification.

DEVICE CHARACTERISTICS (continued)

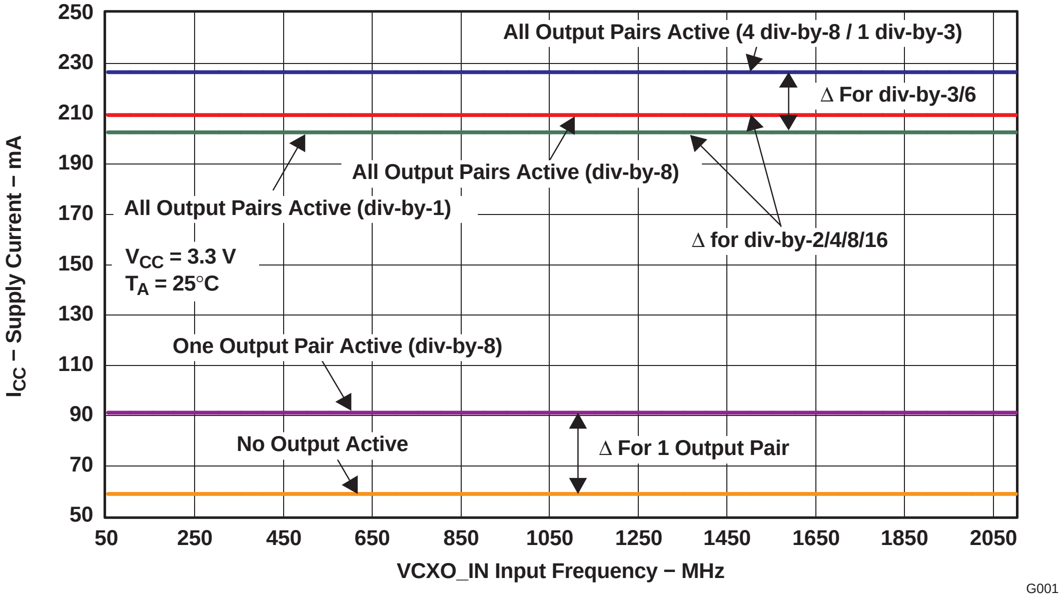
over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(o)}$	LVPECL output skew[5]	Load see Figure 13, all outputs have the same divider ratio			20	ps
		Load see Figure 13, outputs have different divider ratios			50	
t_r / t_f	Rise and fall time	20% to 80% of V_{OUTPP}, see Figure 9	120	170	220	ps
C_I	Input capacitance at VCXO_IN, $\overline{\text{VCXO\_IN}}$			1.5		pF
LVCMOS-TO-LVPECL						
$t_{sk(P\_C)}$	Output skew between LVCMOS and LVPECL outputs, see [7] and Figure 10	Cross point to V_{CC}/2; load, see Figure 12 and Figure 13	1.7	2	2.4	ns
PLL ANALOG LOCK						
I_{OH}	High-level output current	V_{CC} = 3.6 V, V_O = 1.8 V		–110		µA
I_{OL}	Low-level output current	V_{CC} = 3.6 V, V_O = 1.8 V		110		µA
$I_{OZH\ LOCK}$	High-impedance state output current for PLL LOCK output[8]	V_O = 3.6 V ($\overline{PD}$ is set low)		45	65	µA
$I_{OZL\ LOCK}$	High-impedance state output current for PLL LOCK output[8]	V_O = 0 V ($\overline{PD}$ is set low)			±5	µA
V_{IT+}	Positive input threshold voltage	V_{CC} = min to max		V_{CC}×0.55		V
V_{IT-}	Negative input threshold voltage	V_{CC} = min to max		V_{CC}×0.35		V
PHASE DETECTOR						
f_{CPmax}	Maximum charge pump frequency	Default PFD pulse width delay			100	MHz
CHARGE PUMP						
I_{CP}	Charge pump sink/source current range [9]	V_{CP} = 0.5 V_{CC_CP}	±0.2		±3	mA
I_{CP3St}	Charge pump 3-state current	0.5 V < V_{CP} < V_{CC_CP} – 0.5 V			10	nA
I_{CPA}	ICP absolute accuracy	V_{CP} = 0.5 V_{CC_CP}, internal reference resistor, SPI default settings		10%		
		V_{CP} = 0.5 V_{CC_CP}, external reference resistor 12 kΩ (1%) at I_REF_CP, SPI default settings		5%		
I_{CPM}	Sink/source current matching	0.5 V < V_{CP} < V_{CC_CP} – 0.5 V, SPI default settings		2.5%		
I_{VCPM}	ICP vs VCP matching	0.5 V < V_{CP} < V_{CC_CP} – 0.5 V		5%		

(7) The phase of LVCMOS is lagging in reference to the phase of LVPECL.
(8) Lock output has an 80-kΩ pulldown resistor.
(9) Defined by SPI settings.

TYPICAL CHARACTERISTICS

LVPECL SUPPLY CURRENT
vs
NUMBER OF ACTIVE OUTPUTS



A. If div-by-2/4/8/16 is activated for one or more outputs, 'Δ for div-by-2/4/8/16' has to be added to I_{CC} of div-by-1. If div-by-3 or div-by-6 is activated, 'Δ for div-by-2/4/8/16' and 'Δ for div-by3/6' has to be added to I_{CC} of div-by-1.

Figure 1.

LVPECL DEVICE POWER CONSUMPTION
vs
NUMBER OF ACTIVE OUTPUTS

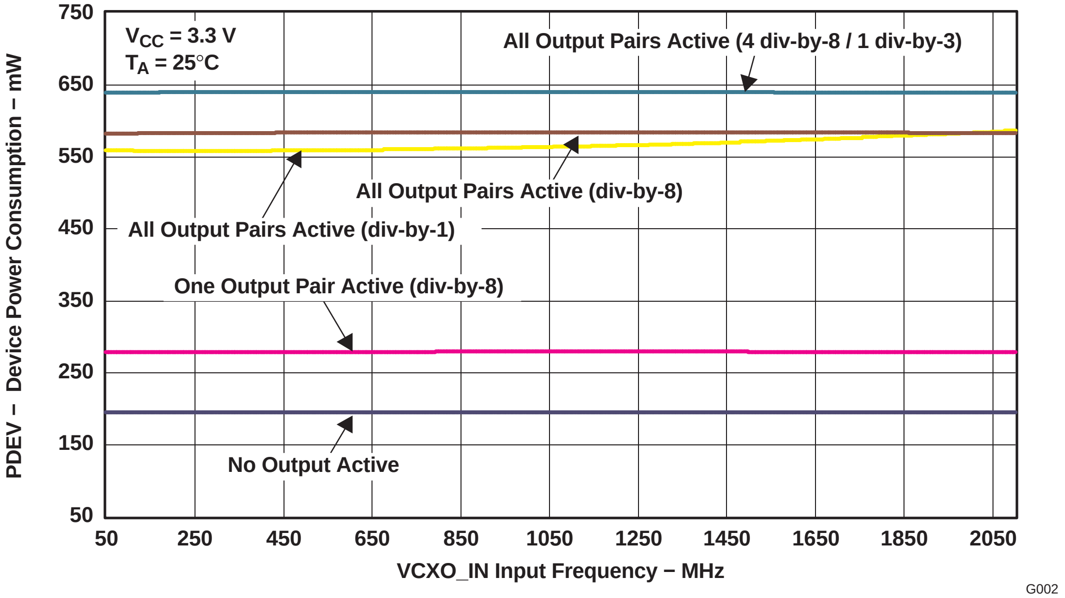
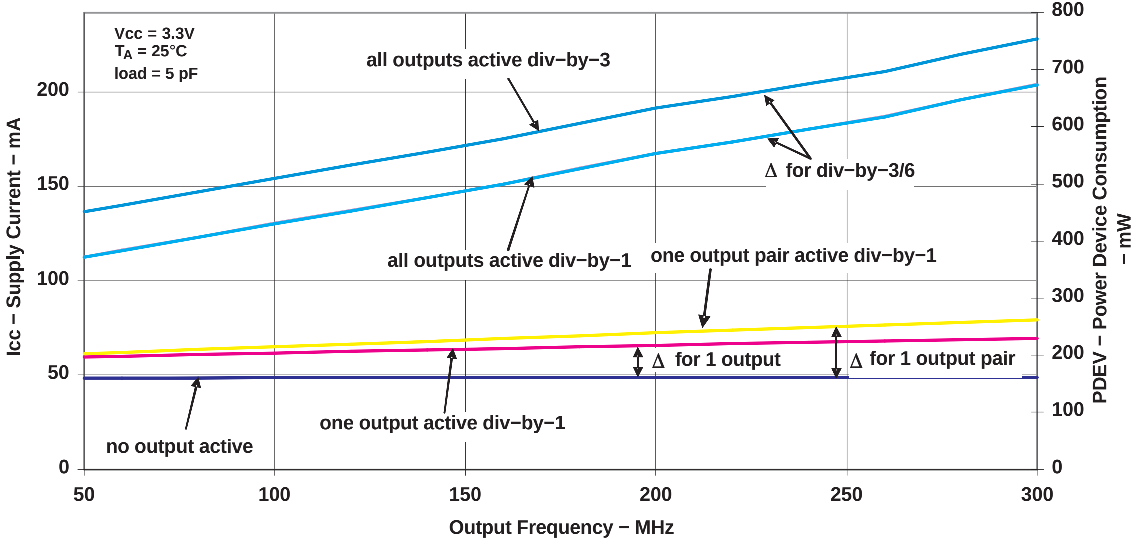


Figure 2.

TYPICAL CHARACTERISTICS (continued)

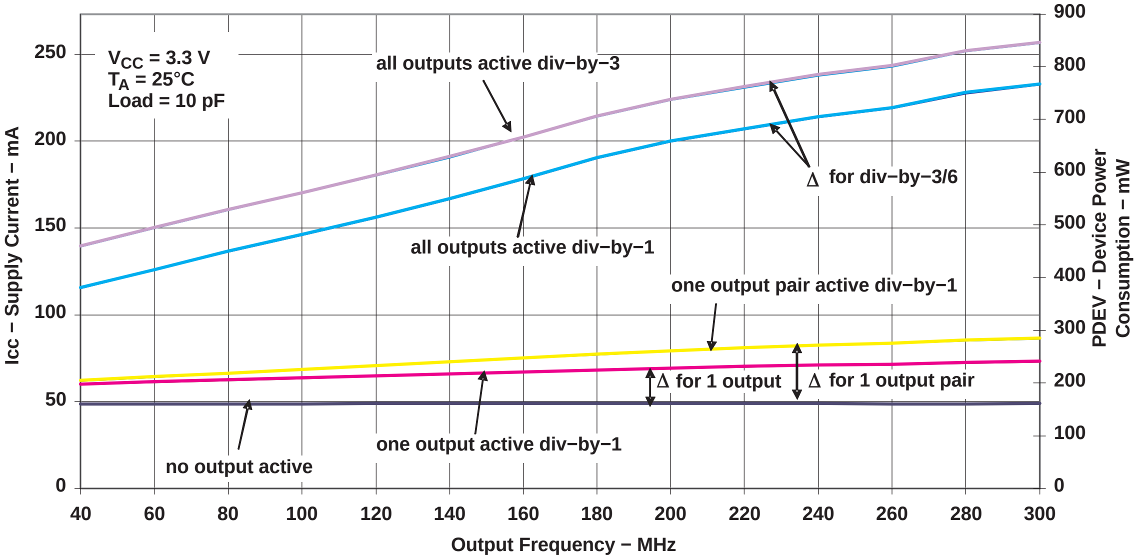
LVCMOS SUPPLY CURRENT / DEVICE POWER CONSUMPTION
vs
NUMBER OF ACTIVE OUTPUTS (Load = 5 pF)



B. It is not recommended to exceed power dissipation of 700 mW for the BGA package at T_A 85°C.

Figure 3.

LVCMOS SUPPLY CURRENT / DEVICE POWER CONSUMPTION
vs
NUMBER OF ACTIVE OUTPUTS (Load = 10 pF)



B. It is not recommended to exceed power dissipation of 700 mW for the BGA package at T_A 85°C.

Figure 4.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL LVPECL OUTPUT VOLTAGE
vs
OUTPUT FREQUENCY

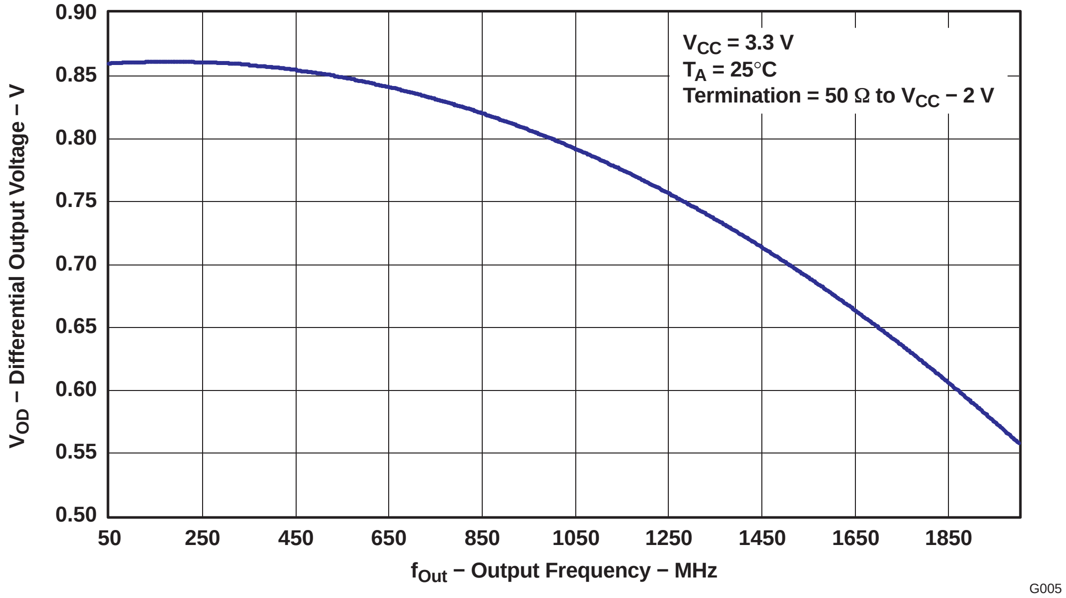


Figure 5.

LVCMOS OUTPUT SWING
vs
FREQUENCY

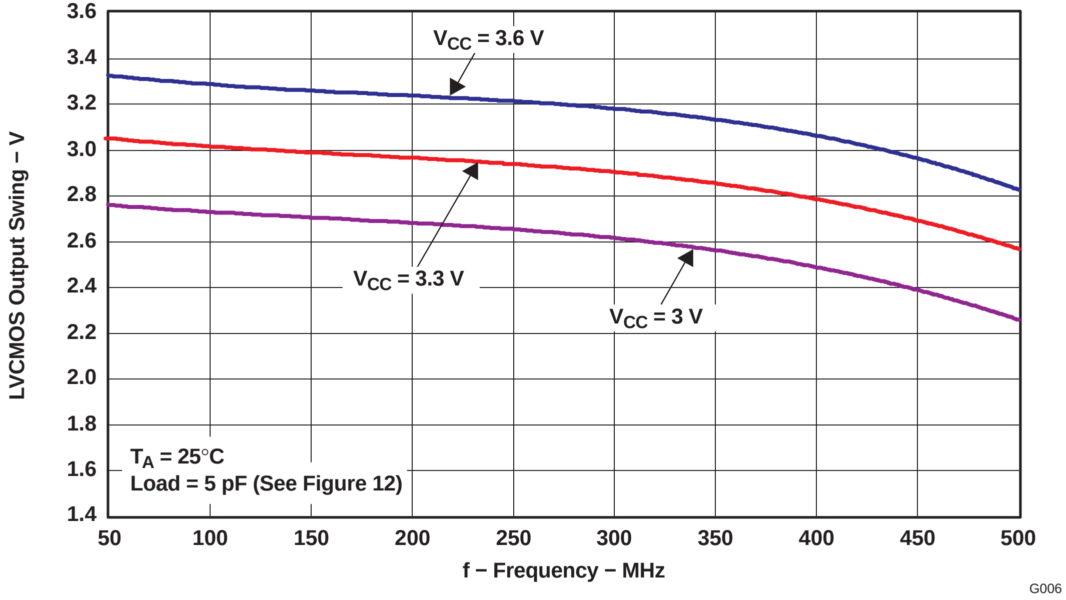


Figure 6.

TYPICAL CHARACTERISTICS (continued)

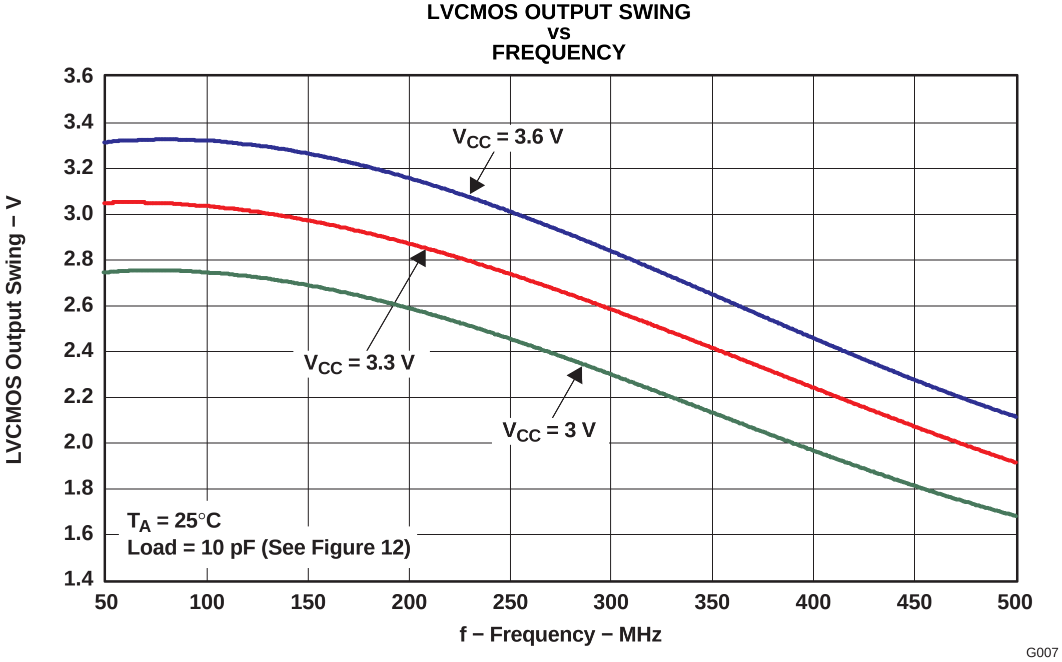


Figure 7.

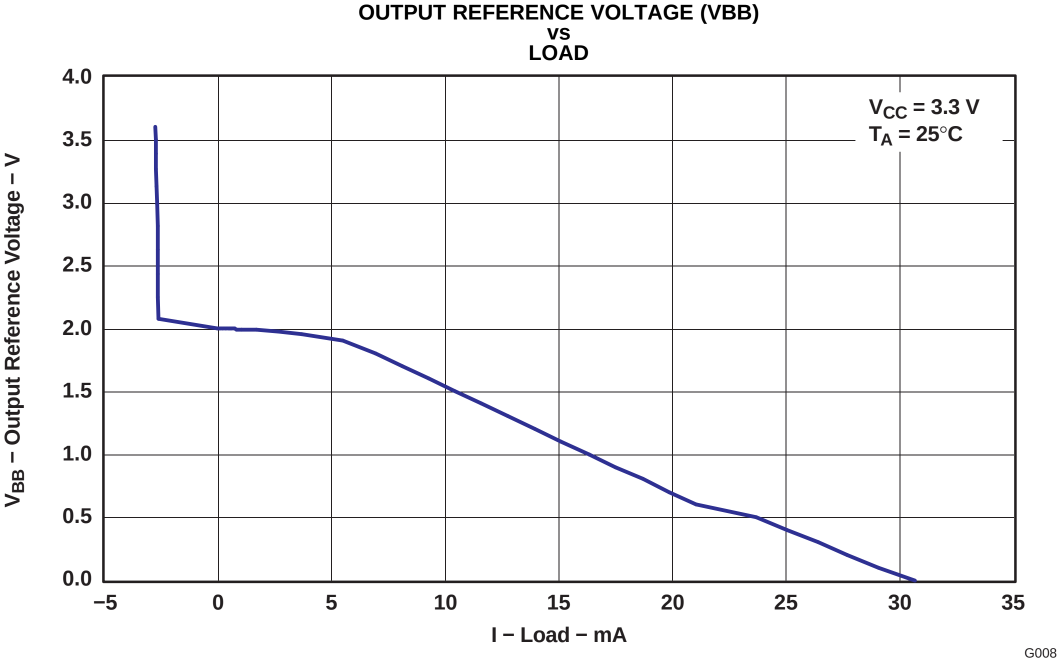


Figure 8.

PARAMETER MEASUREMENT INFORMATION

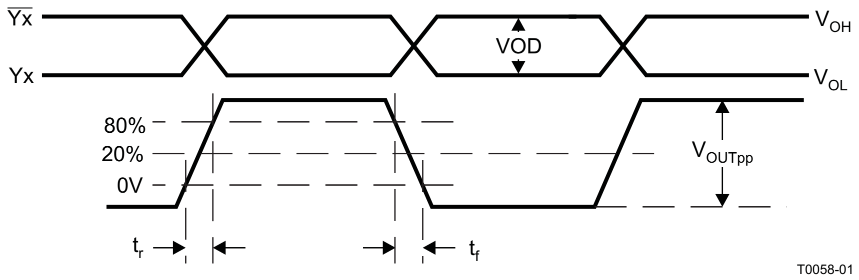
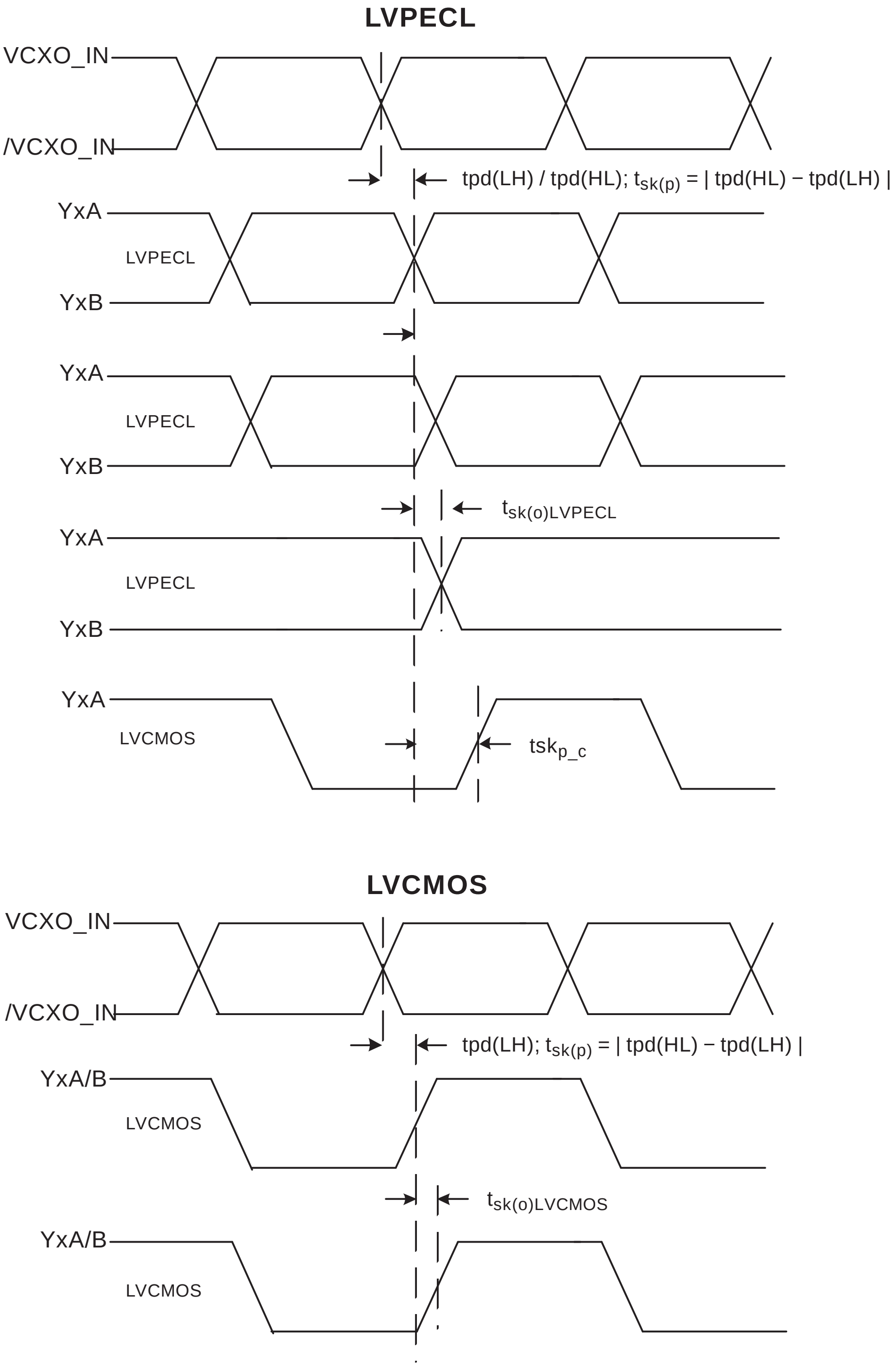


Figure 9. LVPECL Differential Output Voltage and Rise/Fall Time

PARAMETER MEASUREMENT INFORMATION (continued)



A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
The difference between the fastest and the slowest t_{pd}(LH)n (n = 0...4)
The difference between the fastest and the slowest t_{pd}(HL)n (n = 0...4)

B. Pluse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low (t_{pd}(HL)) and the low-to-high (t_{pd}(LH)) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)}$ = |t_{pd}(HL) – t_{pd}(LH) |. Pulse skew is sometimes refered to as *pulse width distortion or duty cycle skew*.

Figure 10. Output Skew

PARAMETER MEASUREMENT INFORMATION (continued)

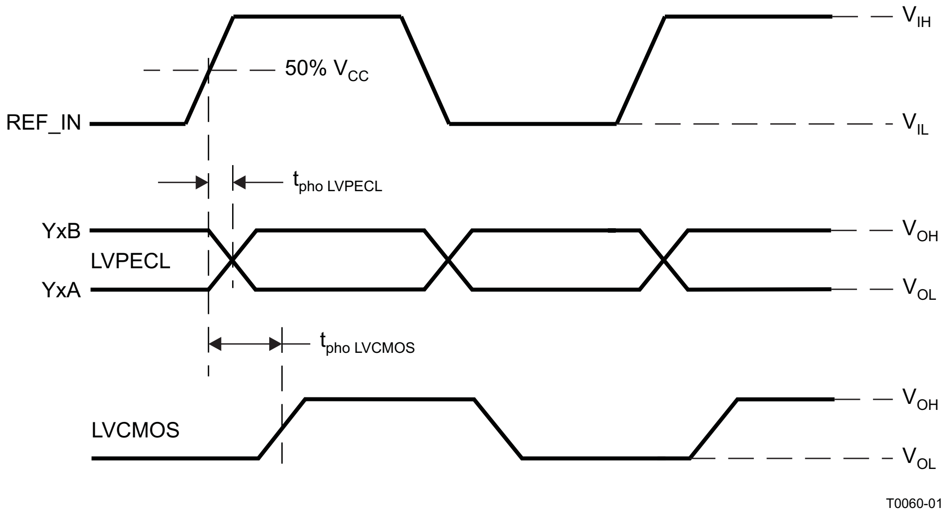


Figure 11. Phase Offset

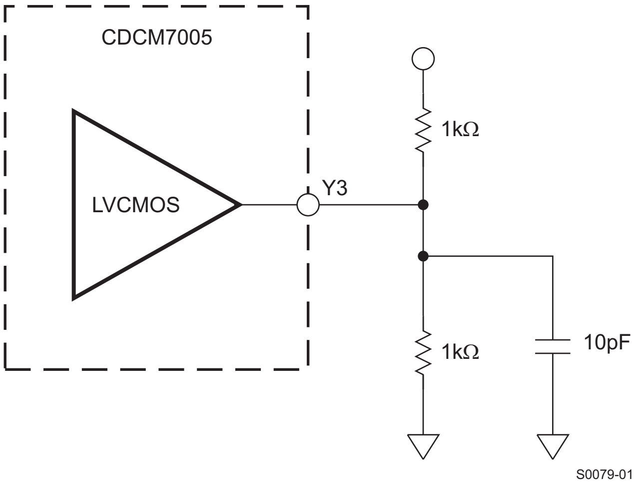


Figure 12. LVCMOS Output Loading During Device Test

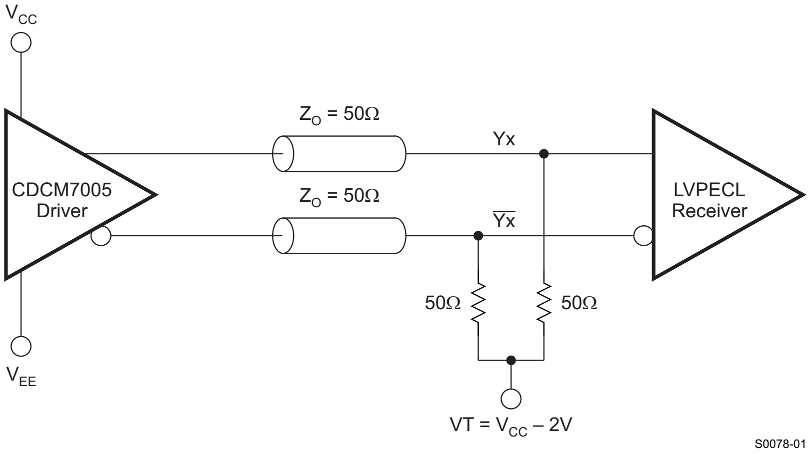


Figure 13. LVPECL Output Loading During Device Test

PARAMETER MEASUREMENT INFORMATION (continued)

SPI CONTROL INTERFACE

The serial interface of the CDCM7005 is a simple SPI-compatible interface for writing to the registers of the device and consists of three control lines: CTRL_CLK, CTRL_DATA, and CTRL_LE. There are four 32-bit wide registers, which can be addressed by the two LSBs of a transferred word (bit 0 and bit 1). Every transmitted word must have 32 bits, starting with MSB first. Each word can be written separately. Bit 7, 8, 10, and Bit 12 to 31 of Word 3 are reserved for factory test purposes and must be filled with zeros. The transfer is initiated with the falling edge of CTRL_LE; as long as CTRL_LE is high, no data can be transferred. During CTRL_LE, low data can be written. The data has to be applied at CTRL_DATA and has to be stable before the rising edge of CTRL_CLK. The transmission is finished by a rising edge of CTRL_LE. With the rising edge of CTRL_LE, the new word is asynchronously transferred to the internal register (e.g., N, M, P, ...). Each word has to be separately transmitted by this procedure. Unused or floating inputs must be tied to proper logic level. A 20kΩ or larger pull−up resistor to VCC is recommended.

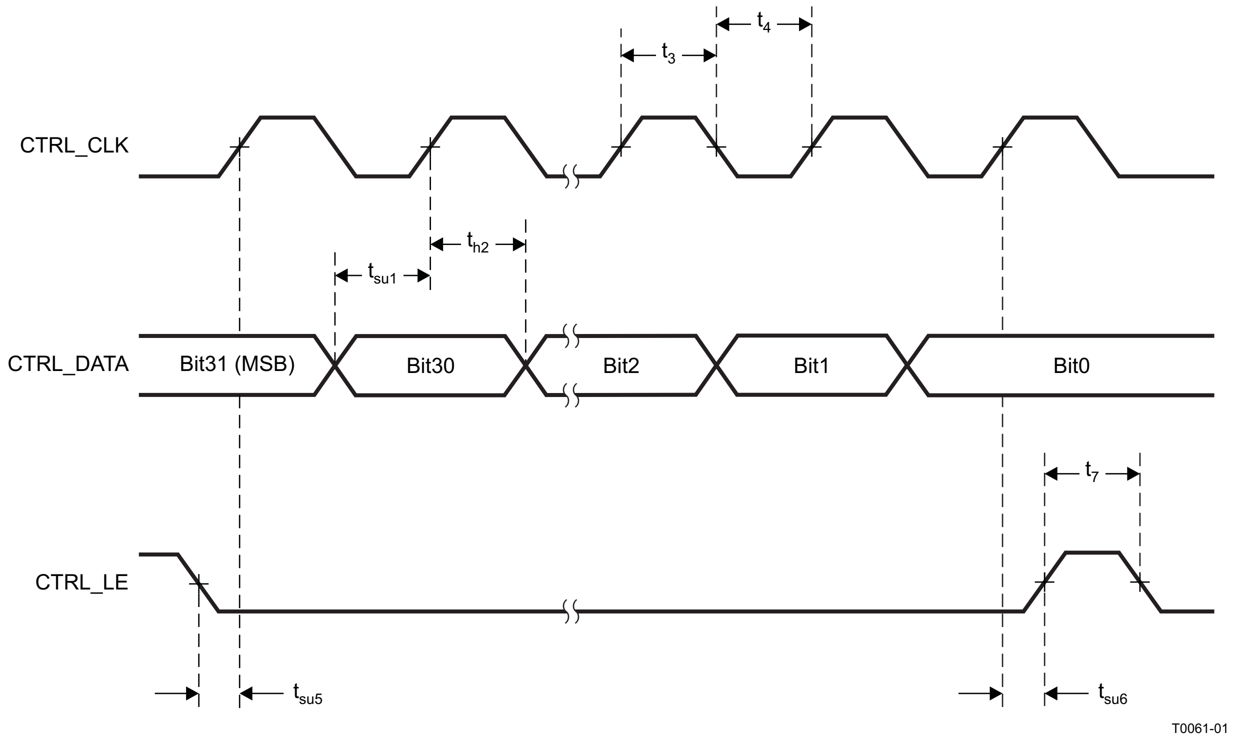


Figure 14. Timing Diagram SPI Control Interface

The SPI serial protocol accepts word Write operation only. There is neither a read, acknowledge, nor a handshake operation.

The following four words include the register settings of the programmable functions of the CDCM7005. It can be modified to the customer application by changing one or more bits. It comes up with a default register setting after power up or if the power down ($\overline{PD}$) control signal is applied. The default setting is shown in column five of the following words.

It is recommended to program Word 0, Word 1, Word 2 and Word 3 right after power up and $\overline{PD}$ becomes HIGH.

A low active function is shown as [0] and a high active function is shown as [1].

PARAMETER MEASUREMENT INFORMATION (continued)

Word 0

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PIN AFFECTED	
					BGA	QFN
0	C0		Register Selection	0		
1	C1		Register Selection	0		
2	M0	Reference Divider M	Reference Divider M Bit 0	1		
3	M1		Reference Divider M Bit 1	1		
4	M2		Reference Divider M Bit 2	1		
5	M3		Reference Divider M Bit 3	1		
6	M4		Reference Divider M Bit 4	1		
7	M5		Reference Divider M Bit 5	1		
8	M6		Reference Divider M Bit 6	1		
9	M7		Reference Divider M Bit 7	0		
10	M8		Reference Divider M Bit 8	0		
11	M9		Reference Divider M Bit 9	0		
12	N0	VC(X)O Divider N (1)	VCXO Divider N Bit 0	1		
13	N1		VCXO Divider N Bit 1	1		
14	N2		VCXO Divider N Bit 2	1		
15	N3		VCXO Divider N Bit 3	1		
16	N4		VCXO Divider N Bit 4	1		
17	N5		VCXO Divider N Bit 5	1		
18	N6		VCXO Divider N Bit 6	1		
19	N7		VCXO Divider N Bit 7	0		
20	N8		VCXO Divider N Bit 8	0		
21	N9		VCXO Divider N Bit 9	0		
22	N10		VCXO Divider N Bit 10	0		
23	N11		VCXO Divider N Bit 11	0		
24	DLYM0	Progr. Delay M	Reference Phase Delay M Bit 0	0		
25	DLYM1		Reference Phase Delay M Bit 1	0		
26	DLYM2		Reference Phase Delay M Bit 2	0		
27	DLYN0	Progr. Delay N	Feedback Phase Delay N Bit 0	0		
28	DLYN1		Feedback Phase Delay N Bit 1	0		
29	DLYN2		Feedback Phase Delay N Bit 2	0		
30	MANAUT	Manual or Auto Ref.	Manual Reference Clock Selection [0] Automatic Reference Clock Selection [1]	0	A1, B1	36, 37
31	REFDEC	Freq. Detect	Reference Frequency Detection on [0], off [1] (2)	0	C8	23

(1) The frequency applied to the Divider N must be smaller than 300 MHz. A sufficient P Divider must be selected with the FB_MUX to maintain this criteria.

(2) If set to low, STATUS_REF will be in normal operation. If set to high, STATUS_REF will be high, even if no valid clock is detected (<2 MHz). This is useful for reference inputs frequencies less than 2 MHz where the frequency detection circuitry normally resets the STATUS_REF signal to low.

Word 1

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PIN AFFECTED	
					BGA	QFN
0	C0		Register Selection	1		
1	C1		Register Selection	0		
2	OUTSEL0	Output (Yx) Signaling Selection	For Output Y0A, Y0B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	F1, G1	46, 47
3	OUTSEL1		For Outputs Y1A, Y1B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	H2, H3	3, 4
4	OUTSEL2		For Outputs Y2A, Y2B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	H4, H5	7, 8
5	OUTSEL3		For Outputs Y3A, Y3B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	H6, H7	11, 12
6	OUTSEL4		For Outputs Y4A, Y4B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	G8, F8	16,17
7	OUT0A0	Output Y0 Mode	Output Y0A Mode Bit 0	0	F1	46
8	OUT0A1		Output Y0A Mode Bit 1	0	F1	46
9	OUT0B0		Output Y0B Mode Bit 0	0	G1	47
10	OUT0B1		Output Y0B Mode Bit 1	0	G1	47
11	OUT1A0	Output Y1 Mode	Output Y1A Mode Bit 0	0	H2	3
12	OUT1A1		Output Y1A Mode Bit 1	0	H2	3
13	OUT1B0		Output Y1B Mode Bit 0	0	H3	4
14	OUT1B1		Output Y1B Mode Bit 1	0	H3	4
15	OUT2A0	Output Y2 Mode	Output Y2A Mode Bit 0	0	H4	7
16	OUT2A1		Output Y2A Mode Bit 1	0	H4	7
17	OUT2B0		Output Y2B Mode Bit 0	0	H5	8
18	OUT2B1		Output Y2B Mode Bit 1	0	H5	8
19	OUT3A0	Output Y3 Mode	Output Y3A Mode Bit 0	0	H6	11
20	OUT3A1		Output Y3A Mode Bit 1	0	H6	11
21	OUT3B0		Output Y3B Mode Bit 0	0	H7	12
22	OUT3B1		Output Y3B Mode Bit 1	0	H7	12
23	OUT4A0	Output Y4 Mode	Output Y4A Mode Bit 0	0	G8	16
24	OUT4A1		Output Y4A Mode Bit 1	0	G8	16
25	OUT4B0		Output Y4B Mode Bit 0	0	F8	17
26	OUT4B1		Output Y4B Mode Bit 1	0	F8	17
27	SREF	Status Ref.	Displays the status of the reference clock at the STATUS_REF output [0] Displays the selected clock (high for PRI_REF and low for SEC_REF clock) at the STATUS_REF output [1]	0	C8	23
28	SXOIREF	Status VCXO or I_REF_CP	Selects STATUS_VCXO [0] Selects I_REF_CP [1] which enable external reference resistor used for charge pump current and analog PLL lock detect output current.	0	D8, A8	22, 25
29	ADLOCK	Analog or Digital Lock	Selects Digital PLL_LOCK [0] Selects Analog PLL_LOCK [1]	0	A8	25
30	90DIV4	90 degree shift div-4	90 degree output phase shift in div-4 mode on [1]; off [0](1)	0	Yx	Yx
31	90DIV8	90 degree shift div-8	90 degree output phase shift in div-8 mode on [1]; off [0](1)	0	Yx	Yx

(1) The P 16-Div has to be selected to obtain the 90 degree phase shift. If bit 30 or bit 31 is set, the Div-by-16 mode is no longer available. The outputs are switched in pairs. Only one bit can be set at a time. If both bits set to [1] at the same time, no 90 degree phase shift mode is selected (equal to off-mode setting).

Word 2

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PIN AFFECTED	
					BGA	QFN
0	C0		Register Selection	0		
1	C1		Register Selection	1		
2	CP_DIR	CP Direction	Determines in which direction CP current regulates (Reference Clock leads to Feedback Clock – see Figure 23) – positive CP output current [0]; – negative CP output current [1];	0	A4	31
3	PRECP		Preset charge pump output voltage to VCC_CP/2, on [1], off [0]	0	A4	31
4	CP0	CP Current	CP Current Setting Bit 0	0	A4	31
5	CP1		CP Current Setting Bit 1	1	A4	31
6	CP2		CP Current Setting Bit 2	0	A4	31
7	CP3		CP Current Setting Bit 3	1	A4	31
8	PFD0	PFD Pulse Width	PFD Pulse Width PFD Bit 0	0	A4	31
9	PFD1		PFD Pulse Width PFD Bit 1	0	A4	31
10	FBMUX0	FB_MUX	Feedback MUX Select Bit 0	1		
11	FBMUX1		Feedback MUX Select Bit 1	0		
12	FBMUX2		Feedback MUX Select Bit 2	1		
13	Y0MUX0	Y0_MUX	Output Y0x Select Bit 0	1	F1, G1	46, 47
14	Y0MUX1		Output Y0x Select Bit 1	0	F1, G1	46, 47
15	Y0MUX2		Output Y0x Select Bit 2	1	F1, G1	46, 47
16	Y1MUX0	Y1_MUX	Output Y1x Select Bit 0	1	H2, H3	3, 4
17	Y1MUX1		Output Y1x Select Bit 1	0	H2, H3	3, 4
18	Y1MUX2		Output Y1x Select Bit 2	1	H2, H3	3, 4
19	Y2MUX0	Y2_MUX	Output Y2x Select Bit 0	1	H4, H5	7, 8
20	Y2MUX1		Output Y2x Select Bit 1	0	H4, H5	7, 8
21	Y2MUX2		Output Y2x Select Bit 2	1	H4, H5	7, 8
22	Y3MUX0	Y3_MUX	Output Y3x Select Bit 0	1	H6, H7	11, 12
23	Y3MUX1		Output Y3x Select Bit 1	0	H6, H7	11, 12
24	Y3MUX2		Output Y3x Select Bit 2	1	H6, H7	11, 12
25	Y4MUX0	Y4_MUX	Output Y4x Select Bit 0	1	G8, F8	16, 17
26	Y4MUX1		Output Y4x Select Bit 1	0	G8, F8	16, 17
27	Y4MUX2		Output Y4x Select Bit 2	1	G8, F8	16, 17
28	$\overline{\text{PD}}$		Power Down mode on [0], off [1]	1	Yx	Yx
29	RESHOL		$\overline{\text{RESET}}$ or $\overline{\text{HOLD}}$ Pin definition: $\overline{\text{RESET}}$ [0] or $\overline{\text{HOLD}}$ [1]	0	H8	14
30	$\overline{\text{RESET}}$		Resets all dividers [0] - (equal to $\overline{\text{RESET}}$ pin function)	1		
31	$\overline{\text{HOLD}}$		3-state charge pump [0] - (equal to $\overline{\text{HOLD}}$ pin function)	1	A4	31

Word 3

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PIN AFFECTED	
					BGA	QFN
0			Register selection	1		
1			Register selection	1		
2	LOCKW 0	Lock Window	Lock-detect window Bit 0	1	A8	25
3	LOCKW 1		Lock-detect window Bit 1	0	A8	25
4	LOCKC0	Lock Cycles	Number of coherent lock events Bit 0	0	A8	25
5	LOCKC1		Number of coherent lock events Bit 1	1	A8	25
6	FOFF	Frequency Offset	Frequency offset mode only for out-of-lock detection on [1] or off [0](1)	0	A8	25
7	RES		RESERVED	0	RES	RES
8	RES		RESERVED	0	RES	RES
9	HOLDF	HOLD Function	Enables the frequency hold-over function on [1], off [0]	0		
10			RESERVED	0	RES	RES
11	HOLDTR	HOLD Trigger Condition	HOLD function always activated [1];(2) Triggered by analog PLL lock detect outputs [0] (if analog PLL Lock signal is set then HOLD is activated; if analog PLL lock signal is reset then HOLD is de-activated).	0		
12	RES		RESERVED	0	RES	RES
13	RES		RESERVED	0	RES	RES
14	RES		RESERVED	0	RES	RES
15	RES		RESERVED	0	RES	RES
16	GTME		General Test Mode Enable. Test Mode is only enabled if this bit is set to 1.	0		
17	RES		RESERVED	0	RES	RES
18	RES		RESERVED	0	RES	RES
19	RES		RESERVED	0	RES	RES
20	RES		RESERVED	0	RES	RES
21	RES		RESERVED	0	RES	RES
22	RES		RESERVED	0	RES	RES
23	RES		RESERVED	0	RES	RES
24	RES		RESERVED	0	RES	RES
25	RES		RESERVED	0	RES	RES
26	RES		RESERVED	0	RES	RES
27	RES		RESERVED	0	RES	RES
28	PFDFC		PFD Frequency Control. Data provided to the PFD are feed through to the corresponding STATUS pins(3)	0	D8	22
29	RES		RESERVED	0	RES	RES
30	RES		RESERVED	0	RES	RES
31	RES		RESERVED	0	RES	RES

(1) If Frequency offset mode only for out-of-lock detection is on, the selected lock detect window is valid for lock detect. Independent from this, out of lock is valid if a frequency offset is detected.
(2) HOLD function always activated is recommended for test purposes only.
(3) The maximum frequency for the STATUS_VCXO pin is 100 MHz.

FUNCTIONAL DESCRIPTION OF THE LOGIC

Reference Divider M (Word 0)(4)

M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	Div by	Default
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	1	2	
0	0	0	0	0	0	0	0	1	0	3	
0	0	0	0	0	0	0	0	1	1	4	
					• • •						
0	0	0	1	1	1	1	1	1	1	128	Yes
					• • •						
1	1	1	1	1	1	1	1	0	1	1022	
1	1	1	1	1	1	1	1	1	0	1023	
1	1	1	1	1	1	1	1	1	1	1024	

(4) If the divider value is Q, then the code will be the binary value of (Q–1).

VC(X)O Feedback Divider N (Word 0)(1) (2)

N11	N10	N0	N8	N7	N6	N5	N4	N3	N2	N1	N0	Div by	Default
0	0	0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	0	0	1	2	
0	0	0	0	0	0	0	0	0	0	1	0	3	
0	0	0	0	0	0	0	0	0	0	1	1	4	
						• • •							
0	0	0	0	0	1	1	1	1	1	1	1	128	Yes
						• • •							
1	1	1	1	1	1	1	1	1	1	0	1	4094	
1	1	1	1	1	1	1	1	1	1	1	0	4095	
1	1	1	1	1	1	1	1	1	1	1	1	4096	

(1) If the divider value is Q, then the code will be the binary value of (Q–1).
(2) The frequency applied to the Divider N must be smaller than 300 MHz. A sufficient P Divider must be selected with the FB_MUX to maintain this criteria.

Output Mode Selection for LVCMOS and LVPECL Outputs: Y0A, Y0B, Y1A …Y4B (Word 1)[1]

	OUTSELx	OUTxB1	OUTxB0	LVCMOS [YxB]	OUTxA1	OUTxA0	LVCMOS [YxA]	Default
LVCMOS	0	0	0	Active	0	0	Active	
	0	0	1	3-state	0	1	3-state	
	0	1	0	Inverting	1	0	Inverting	
	0	1	1	Low	1	1	Low	
	OUTSELx	**OUTxB1**	**OUTxB0**		**OUTxA1**	**OUTxA0**	**LVCMOS [YxA]**	**Default**
LVPECL	1	x	x		x	0	Active	Yx
	1	x	x		x	1	3-state	

[1] If the differential LVPECL output e.g. Y0A:Y0B is selected (bit 2 of word 1), then only bit 7 of word 1 defines the output mode for Y0A:Y0B. The settings of bit 8, bit 9, and bit 10 of word 1 are therefore not relevant to the Y0A:Y0B. This applies for the other LVPECL outputs as well.

Reference Delay M (PRI_REF or SEC_REF) and Feedback Delay N (VCXO) Phase Adjustment (Word 0)[1]

DLYM2 / DLYN2	DLYM1 / DLYN1	DLYM0 / DLYN0	Phase Offset	Default
0	0	0	0 ps	Yes
0	0	1	±160 ps	
0	1	0	±320 ps	
0	1	1	±480 ps	
1	0	0	±830 ps	
1	0	1	±1130 ps	
1	1	0	±1450 ps	
1	1	1	±1750 ps	

[1] If Progr. Delay M is set, all Yx outputs are lagging to the reference clock according to the value set. If Progr. If Delay N is set; all Yx outputs are leading to the reference clock according to the value set. Above are typical values at V_{CC} = 3.3 V, Temp = 25°C, PECL-output relate to Div4 mode.

PFD Pulse Width Delay (Word 2)

PFD1[1]	PFD0[1]	PFD Pulse Width[1] [2]	Default[1]
0	0	1.5 ns	Yes
0	1	3 ns	
1	0	4.5 ns	
1	1	6 ns	

[1] The *PFD pulse width delay* gets around the dead zone of the PFD transfer function and reduces phase noise and reference spurs.
[2] Typical values at V = 3.3 V_{CC}, Temp = 25°C .

Lock-Detect Window (Word 3)

LOCKW1	LOCKW0	Phase-Offset at PFD Input[1]	Default
0	0	3.5 ns	
0	1	8.5 ns	Yes
1	0	18.5 ns	
1	1	Frequency offset[2]	

[1] Typical Values at V_{CC} = 3.3 V, Temp = 25°C.
[2] The PLL is out-of-lock (PLL_LOCK set low) if a certain frequency offset between reference frequency and feedback frequency (VCXO) at PFD input is detected. The minimum detectable frequency offset depends on the device setting and can be calculated:
(a) $f_{offsetPDF} = f_{PFD} - 1/(1/f_{PFD} + PWD)$
(b) $f_{offsetPFD}$ = detectable frequency offset at PFD between the reference frequency (f_{REF}) and feedback frequency (f_{FB})
(c) f_{PFD} = frequency at phase-frequency detection circuitry
(d) PWD = PFD Pulse Width Delay

Number of Successive Lock Events Inside the Lock Detect Window (Word 3)

LOCKC1[1]	LOCKC0[1]	No. of Successive Lock Events[1]	Default[1]
0	0	1	
0	1	16	
1	0	64	Yes
1	1	256	

(1) This does not apply to Out-of-Lock condition.

Charge Pump Current (Word 2)

CP3	CP2	CP1	CP0	Typical Charge Pump Current	Default
0	0	0	0	0 µA (3-state)	
0	0	0	1	200 µA	
0	0	1	0	400 µA	
0	0	1	1	600 µA	
0	1	0	0	800 µA	
0	1	0	1	1 mA	
0	1	1	0	1.2 mA	
0	1	1	1	1.4 mA	
1	0	0	0	1.6 mA	
1	0	0	1	1.8 mA	
1	0	1	0	2.0 mA	Yes
1	0	1	1	2.2 mA	
1	1	0	0	2.4 mA	
1	1	0	1	2.6 mA	
1	1	1	0	2.8 mA	
1	1	1	1	3 mA	

FB_MUX Selection (Word 2)

FBMUX2	FBMUX1	FBMUX0	Selected VC(X)O Signal for the Phase Discriminator	Default
0	0	0	Div by 1	
0	0	1	Div by 2	
0	1	0	Div by 3	
0	1	1	Div by 4	
1	0	0	Div by 6	
1	0	1	Div by 8	Yes
1	1	0	Div by 16[1]	
1	1	1	Div by 8	

(1) This divider setting depends on the selected P-divider mode for the “Div-by-16” divider. In the default mode (after power up), Div-by-16 is selected. But if bit 30 or bit 31 of word 1 is set to [1], then the Div-by-4 and 90 degree phase shift or Div-by-8 and 90 degree phase shift is selected.

Yx_MUX – Output Divider Selection for Y0, Y1, Y2, Y3, Y4 (Word 2)

YxMUX2	YxMUX1	YxMUX0	Selected Divided V(C)XO Signal for the Yx Outputs	Default
0	0	0	Div by 1	
0	0	1	Div by 2	
0	1	0	Div by 3	

YxMUX2	YxMUX1	YxMUX0	Selected Divided V(C)XO Signal for the Yx Outputs	Default
0	1	1	Div by 4	
1	0	0	Div by 6	
1	0	1	Div by 8	all Yx
1	1	0	Div by 16[1]	
1	1	1	Div by 8	

(1) This divider setting depends on the selected P-divider mode for the “Div-by-16” divider. In the default mode (after power up), Div-by-16 is selected. But if bit 30 or bit 31 of word 1 is set to [1], then the Div-by-4 and 90 degree phase shift or Div-by-8 and 90 degree phase shift is selected.

FEATURE DESCRIPTION

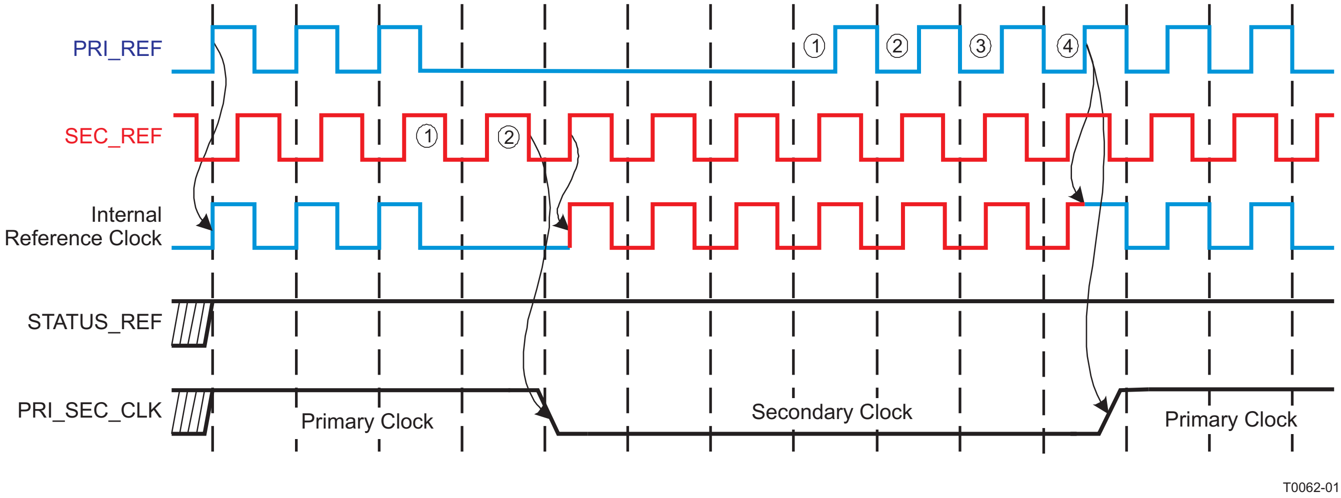
Automatic/Manual Reference Clock Switching

The CDCM7005 supports two reference clock inputs, the primary clock input, PRI_REF, and the secondary clock input, SEC_REF. The clocks can be selected manually or automatically. The respective mode is selected by the dedicated SPI register bit (Word 0, Bit 30).

In the manual mode, the external REF_SEL signal selects one of the two input clocks:

REF_SEL [1] -> primary clock is selected
REF_SEL [0] -> secondary clock is selected

In the automatic mode, the primary clock is selected by default even if both clocks are available. In case the primary clock is not available or fails, then the input switches to the secondary clock as long until the primary clock is back. Figure 15 shows the automatic clock selection.



NOTE: PRI_REF is the preferred clock input.

Figure 15. Behavior of STATUS_REF and PRI_SEC_CLK

In the automatic mode, the frequencies of both clock signals have to be similar, but may differ by up to 20%. The phase of the clock signal can be any.

The clock input circuitry is design to suppress glitches during switching between the primary and secondary clock in the manual and automatic mode. This avoids an undefined switching of the following circuitries.

The phase of the output clock slowly follows the new input phase. There will be no phase-jump at the output. How quick the phase adjustment is done depends on the selected loop parameter, i.e., at a loop bandwidth of <100 Hz; the phase adjustment can take several ms. There is no phase build-out function supported (like in SONET/SDH applications).

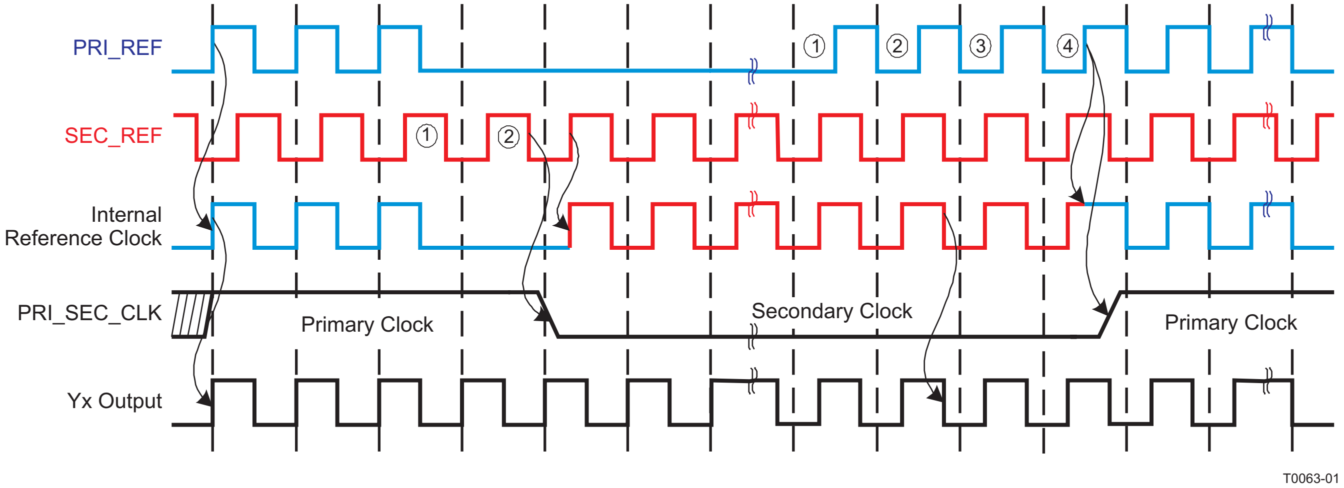


Figure 16. Phase Approach of Output to New Reference Clock

PLL Lock for Analog and Digital Detect

The CDCM7005 supports two PLL lock indications: the digital lock signal or the analog lock signal. Both signals indicate logic high-level at PLL_LOCK if the PLL locks according the selected lock condition.

PLL Lock/Out-of-Lock Definition

The PLL is locked (set high), if the rising edge of the Reference Clock (PRI_REF or SEC_REF clock) and Feedback Clock (VCXO_IN clock) at the PFD (phase frequency detect) are inside a predefined lock detect window, or if no frequency offset appears, for a pre-defined number of successive clock cycles.

The PLL is out-of-lock (set low), if the rising edge of the Reference Clock (PRI_REF or SEC_REF clock) and Feedback Clock (VCXO_IN clock) at the PFD are outside the predefined lock detect window or if a frequency offset appears.

Both, the lock detect window and the number of successive clock cycles are user definable (Word 3, Bit 2-6).

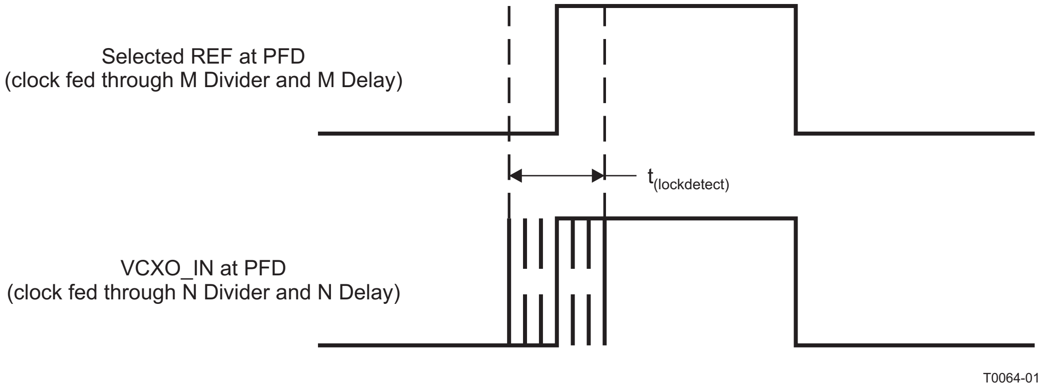


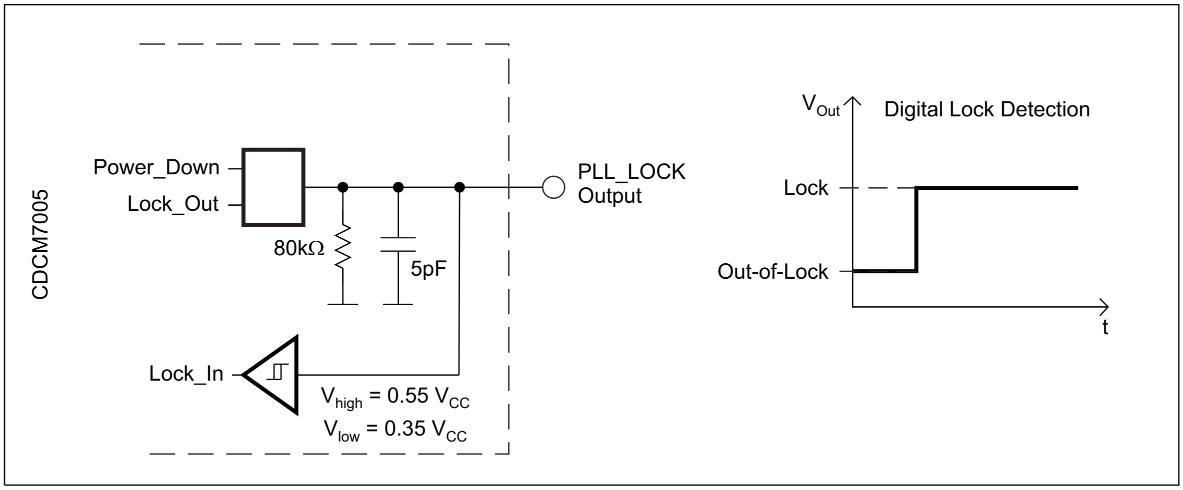
Figure 17. Lock Detect Window

The lock detect window describes the maximum allowed time difference for lock detect between the rising edge of PRI_REF or SEC_REF and VCXO_IN. The time difference is detected at the phase frequency detector. The rising edge of PRI_REF or SEC_REF is taken as reference. The rising edge of VCXO_IN is outside the lock detect window if there is a phase displacement of more than $+0.5 \times t_{(lockdetect)}$ or $-0.5 \times t_{(lockdetect)}$.

Digital vs Analog Lock

Figure 18 and Figure 19 show the circuit for the digital and analog lock. The analog lock operates with an external load capacitor.

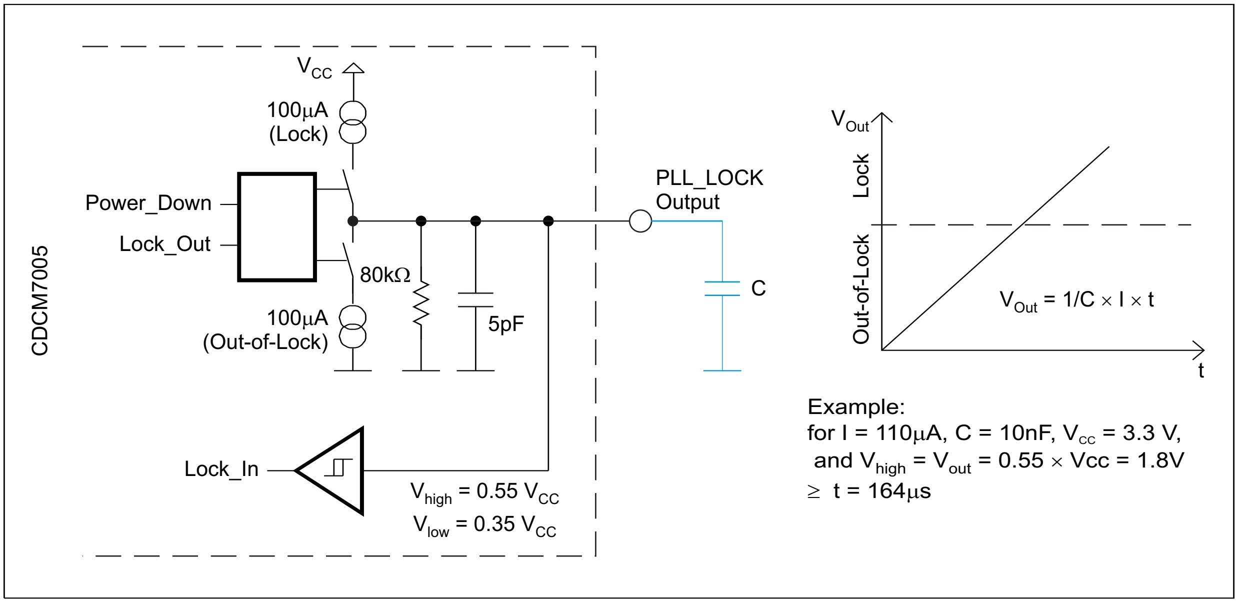
When selecting the digital PLL lock option, PLL_LOCK will possibly jitter several times between lock and out of lock until a stable lock is detected. A single low-to-high step can be reached with a wide lock detect window and high number of successive clock cycles. PLL_LOCK returns to out of lock if just one cycle is outside the lock detect window or a frequency offset occurs.



S0080-01

Figure 18. Digital Lock-Detect

When selecting the analog PLL Lock option, the high-pulses load the external capacitor via the internal 110-µA current source until logic high-level is reached. Therefore, more time is needed to detect logic high level, but jittering of PLL_LOCK will be suppressed in case of digital lock. The time PLL_LOCK needs to return to out of lock depends on the level of V_{Out}, when the current source starts to unload the external capacitor.



S0081-01

Figure 19. Analog Lock-Detect

Differential LVPECL Outputs and Single-Ended LVCMOS Outputs

The CDCM7005 supports up to 5 × LVPECL outputs or 10 × LVCMOS/LVTTL outputs or any combination of these. The single-ended LVCMOS outputs are arranged in pairs which mean both outputs of a LVCMOS pair have the same frequency but can separately be disabled or inverted. The power up output arrangement is five LVPECL (default setting).

The LVPECL outputs are designed to terminate in to a 50-Ω load to V_{CC} – 2 V. The LVCMOS outputs supports the standard LVCMOS load (see Figure 12). The LVPECL and LVCMOS outputs can be enabled (normal operation) or disabled (3-state).

In addition, the output phase can be shifted by 90 degrees when using the additional div-by-4 or div-by-8 mode of the P16-Div (see Figure 20). In the default mode (after power up), the div-by-16 mode of the P16-Div is active. To change it to a 90 degree phase shift, bit 30 or bit 31 of word 1 has to be programmed accordingly. The P 16-Div has to be selected via the dedicated YxMUX to obtain the 90 degree phase shift. The outputs are switched in pairs. When selecting the 90 degree phase shift mode, the div-by-16 functions will no longer be available. The 90 degree phase shifted signal is lagging to the non-shifted signal.

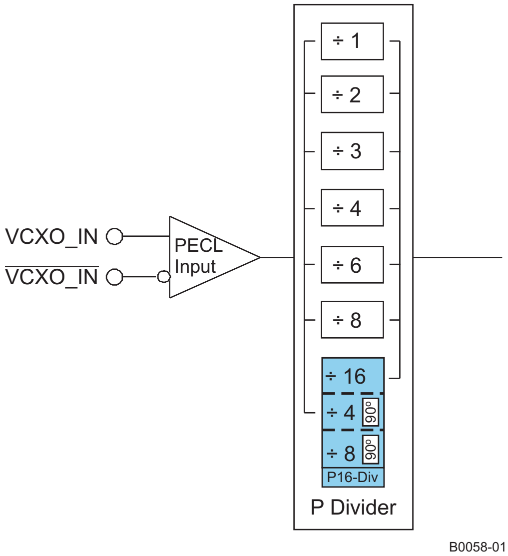


Figure 20. 90 Degree Phase Shift Option of P-Divider

The following diagram shows the LVCMOS and LVPECL output signal when 90 degree phase shift is on.

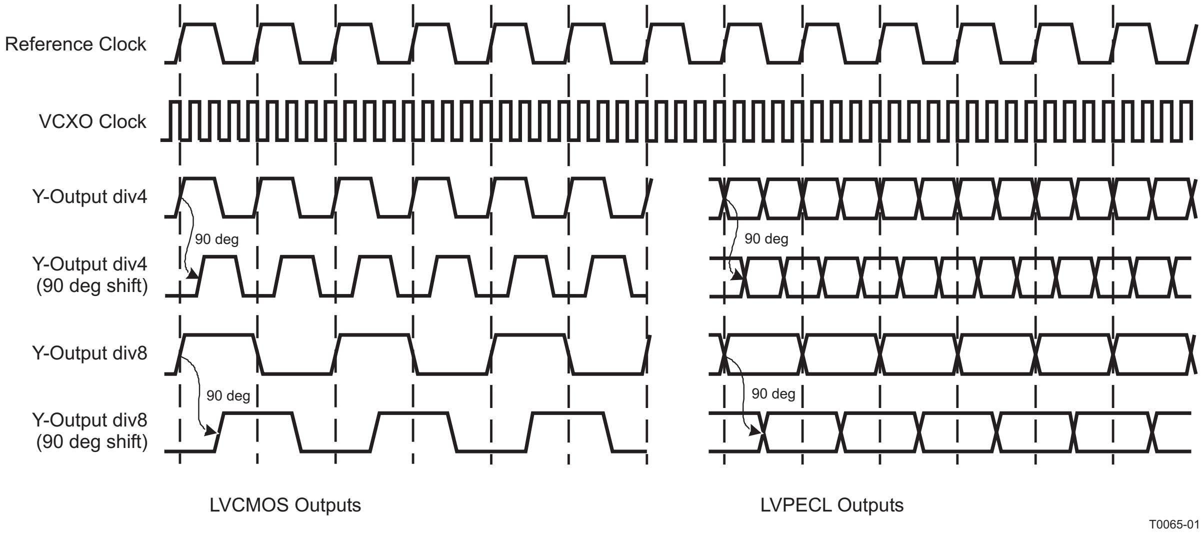


Figure 21. Output Switching Diagram

In addition, the LVCMOS supports disabled-to-low and 180 degree output phase shift for each output individually. When selecting the 180 degree phase shift together with the 90 degree phase shift, the respective outputs has a total phase shift of 270 degree (see Table 2).

Table 2. LVCMOS Phase Shift Options

Phase	P-Divider	180°Phase-Shift	P16-Div - Function
0°	Any P-Divider	No	div-by-16
90°	P16-Div	No	div-by-4 or div-by-8
180°	Any P-Divider	Yes	div-by-16
270°	P16-Div	Yes	div-by-4 or div-by-8

If the P16-Div is selected by the FB_MUX and div-by-4 or div-by-8 is active, the 90 degree phase shifted clock will be synchronized to PRI_REF or SEC_REF. This means all outputs Yxx, which are switched to div-by-4 or div-by-8, are in phase to PRI_REF or SEC_REF. All other outputs are 90 degree phase shifted with leading phase.

Frequency Hold-Over Mode

The HOLD function is a useful feature which helps the designer to improve the system reliability. The HOLD function holds the output frequency in case the input reference clock fails or is disrupted. During HOLD, the charge pump is switched off (3-state) freezing the last valid output frequency. The hold function will be released after a valid reference clock is back. For proper HOLD function, the analog PLL lock detect mode has to be active.

The following register settings are involved with the HOLD function:

- *Lock Detect Window (Word 3, Bit 2, 3, 6)*: Defines the window in ns inside the lock is valid. The size is 3.5 ns, 8.5 ns, 18.5 ns, or a certain frequency offset. Lock is set if reference clock and the feedback clock are inside this predefined lock-detect window for a pre-selected number of successive cycles or if no frequency offset appears.
- *Out-of-Lock:* Defines the out-of-lock condition: If the reference clock and the feedback clock at the PFD are outside the predefined Lock Detect Window or if a certain frequency offset occurs.
- *Cycle-Slip (Word 3, Bit 6)*: A Frequency offset occurs if a certain frequency offset between reference frequency and feedback frequency (VCXO) at PFD input is detected. The minimum detectable frequency offset depends on the device setting and can be calculated:

  $f_{offsetPDF} = f_{PFD} - 1/(1/f_{PFD} + PWD)$

  where

  - $f_{offsetPFD}$ = detectable frequency offset at PFD between the reference frequency (f_{REF}) and feedback frequency (f_{FB})
  - f_{PFD} = frequency at phase-frequency detection circuitry
  - PWD = PFD Pulse Width Delay (1)
- *Number of Clock Cycles (Word 3, Bit 4, 5)*: Defines the number of successive PFD cycles which have to occur inside the lock window to set Lock detect. This applies not for out-of-lock condition.
- *Hold-Function (Word 3, Bit 9)*: Selects HOLD function (see more details below).
- *Hold-Trigger (Word 3, Bit 11)*: Defines whether the HOLD function is always activated (Bit 11 = [1]) or whether it is dependent on the state of the analog PLL lock detect output (Bit 11 = [0]). In the latter case, HOLD is activated, if lock is set (high) and de-activated if Lock is reset (low).
- *Analog PLL Lock Detect (Word 1, Bit 29)*: Analog lock output charges or discharges an external capacitor with every valid lock cycle. The time constant for Lock detect can be set by the value of the capacitor.

The CDCM7005 supports two types of HOLD functions, one external controllable $\overline{\text{HOLD}}$ mode and one internal mode, HOLD.

With the *external $\overline{\text{HOLD}}$ function* the charge pump can directly be switched into 3-state (pin H8 [BGA] or pin 14 [QFN] can be programmed for $\overline{\text{HOLD}}$ [Word 2, Bit 29]). This function is also available via SPI register (Word 2, Bit 31).

If logic low is applied to the HOLD pin, the charge pump will be switched to 3-state. After the HOLD pin is released, the charge pump is switched back in to normal operation with the next valid reference clock cycle at PRI_REF or SEC_REF and the next valid feedback clock cycle at the PFD. During HOLD, the P divider and all outputs Yx are at normal operation.

HOLD-Over-Function: The PLL has to be in lock to start the HOLD function. It switches the charge pump in to 3-State when an out-of-lock event occurs. It leaves the 3-state charge pump state when the reference clock is back. Then it starts a locking sequence of 64 cycles before it goes back to the beginning of the HOLD-over loop. The dedicated looking sequence and a digital phase alignment enable a fast lock.

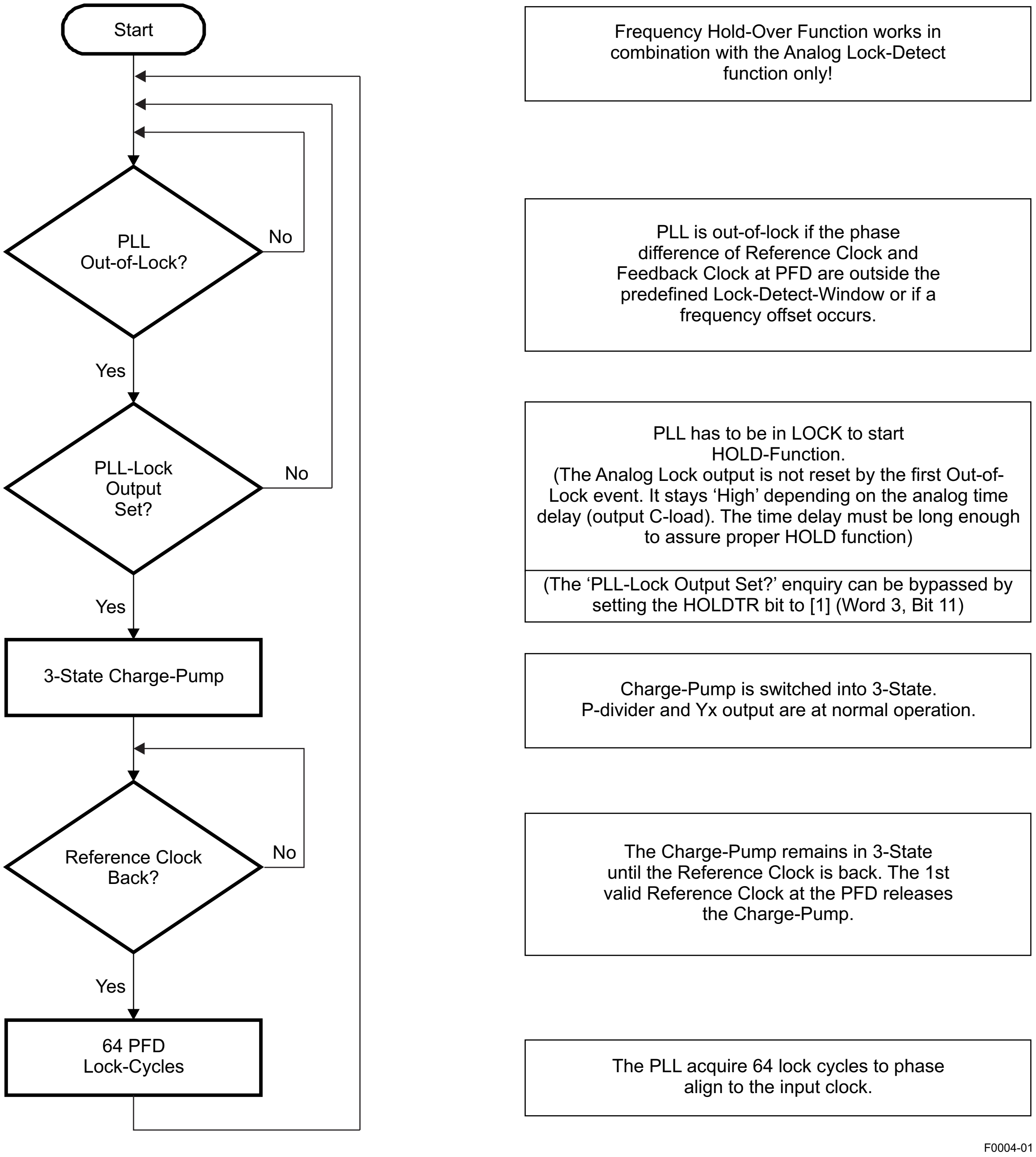


Figure 22. Frequency HOLD-Over Function

Charge Pump Preset to VCC_CP/2

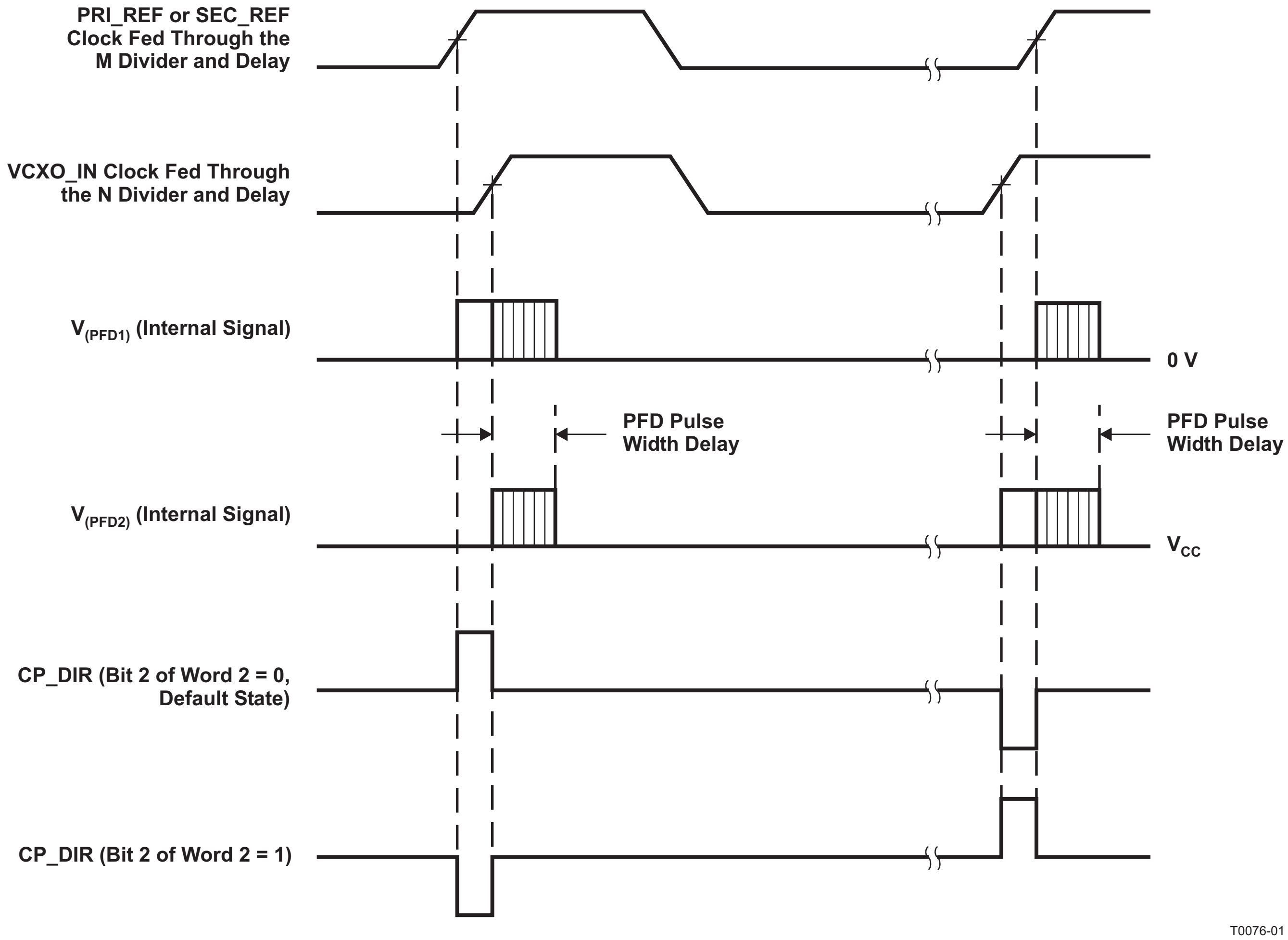
The preset charge pump to VCC_CP/2 is a useful feature to quickly set the center frequency of the VC(X)O after powerup or reset. The adequate control voltage for the VC(X)O will be provided to the charge-pump output by an internal voltage divider of 1 kΩ/1 kΩ to VCC_CP and GND (VCC_CP/2).

This feature helps to get the initial frequency accuracy, i.e. required at CPRI (Common Public Radio Interface) or OBSAI (Open Base Station Architecture Initiative).

The preset charge pump to VCC_CP/2 can be set and reset by SPI register (word 2, bit 3). This feature must be disabled for PLL locking.

Charge Pump Current Direction

The direction of the charge pump (CP) current pulse can be changed by the SPI register (word 2, bit 2). It determines in which direction the CP current regulates (reference clock leads to feedback clock). Most applications use the positive CP output current (power-up condition) because of the use of a passive loop filter. The negative CP current is useful when using an active loop filter concept with inverting operational amplifier. Figure 23 shows the internal PFD signal and the corresponding CP current.



NOTE: The purpose of the PFD pluse width delay is to improve spurious suppression.

Figure 23. Charge Pump Current Direction (VCXO and VCO Support)

APPLICATION INFORMATION

Phase Noise Reference Circuit

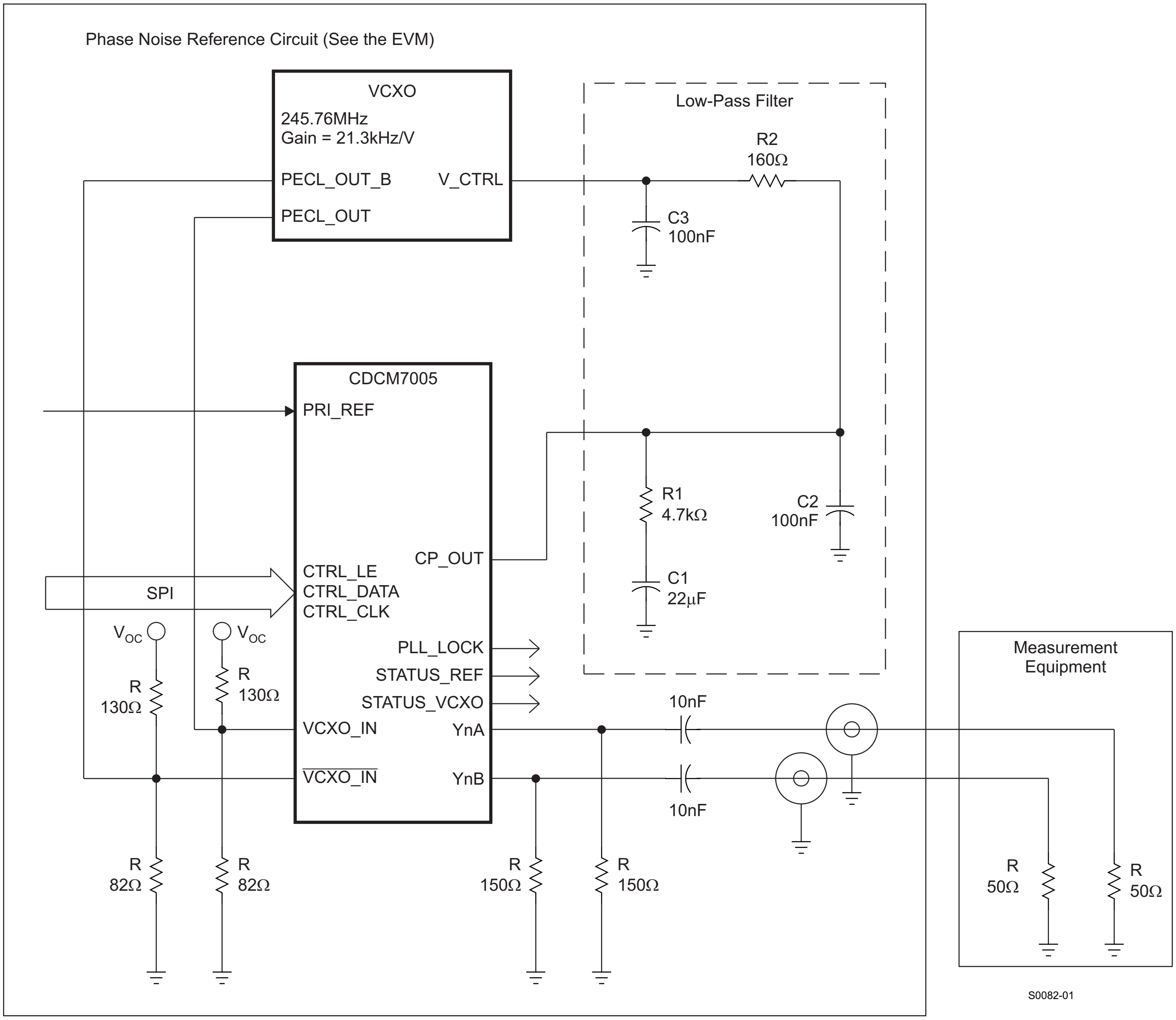


Figure 24. Typical Applications Diagram With Passive Loop Filter

Phase Noise Performance

PARAMETER(1)		TEST CONDITIONS	REF_IN PHASE NOISE AT 30.72 MHz	VCXO PHASE NOISE AT 245.76 MHz	Yx PHASE NOISE AT 30.72 MHz		UNIT
					LVCMOS	LVPECL	
					TYP(2)	TYP(2)	
phn10	Phase noise at 10 Hz	Y = 30.72 MHz; f_{PFD} = 200 kHz, Loop BW = 20 Hz, Feedback Divider = 8 x 128 (N x P), f_{REF_IN} = 30.72 MHz, M-Divider = 128, I_{CP} = 2 mA	–109	–75	–104	–100	dBc/Hz
phn100	Phase noise at 100 Hz		–125	–97	–116	–116	dBc/Hz
phn1k	Phase noise at 1 kHz		–134	–117	–140	–140	dBc/Hz
phn10k	Phase noise at 10 kHz		–136	–138	–153	–152	dBc/Hz
phn100k	Phase noise at 100 kHz		–138	–148	–156	–153	dBc/Hz
phn1Mk	Phase noise at 1 MHz		–144	–148	–156	–153	dBc/Hz
phn10M	Phase noise at 10 MHz		–144	–148	–156	–153	dBc/Hz
PLL Stabilization Time							
tstabi	PLL stabilization time(3)	Y = 30.72 MHz, f_{PFD} = 200 kHz, Loop BW = 20 Hz, Feedback Divider = 8 x 128 (N x P), f_{REF_IN} = 30.72 MHz, M-Divider = 128, I_{CP} = 2 mA			400		ms

(1) Output phase noise is dependent on the noise of the REF_IN clock and VCXO clock noise floor. The phase noise performance of the BGA and the QFN package is equal. The phase noise measurements were taken with the CDCM7005 EVM and CDCM7005 SPI default settings.

(2) The typical stabilization time is based on the above application example. The stabilization criterion was a stable high level of PLL_LOCK.

(3) For further explanations, as well as phase noise/jitter test results using various VCXOs, see application note SCAA067.

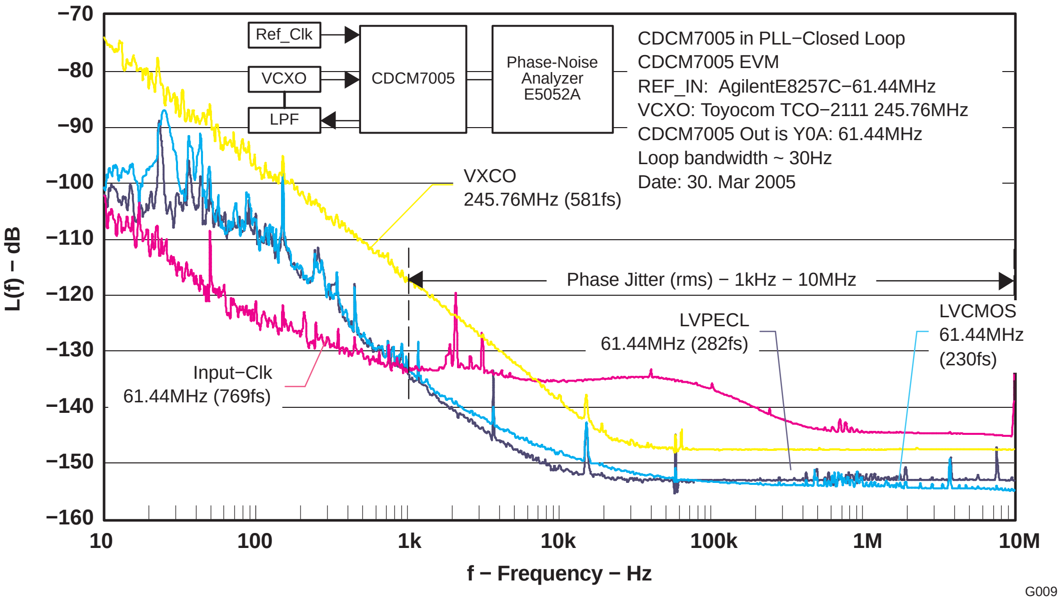


Figure 25. Phase Noise (61.44-MHz REF_IN and 61.44-MHz Output Frequency)

In-Band Noise Performance

Table 3.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$pn_{in\text{-}band}$	In-band phase noise test conditions	Y = 900 MHz, f_{PFD} = 400 kHz, Loop BW = 27 kHz, Feedback Divider = 8 x 282 (N x P), f_{REF_IN} = 10 MHz; M-Divider = 25, I_{CP} = 3 mA		–95		dBc/Hz
pn_{f400}	Phase noise floor at 400 kHz f_{PFD}, in-band noise – 20log(feedback div) (1)			–162		dBc/Hz
pn_{f1}	Phase noise floor at 1 Hz f_{PFD}, in-band noise – 20log(feedback div) – 10log(f_{PFD}) (2)			–218		dBc/Hz

(1) The synthesizer phase noise floor can be estimated by measuring the in-band noise at the output of the CDCM7005 and subtracting 20log(Feedback Divider) N (in case of CDCM7005 it is the N+P divider). The calculated phase noise floor still based on the PFD update frequency, in the above specification, is 400 kHz.

(2) The in-band noise can also be normalized to a comparison frequency of 1 Hz. The resulting phase noise floor is: pnfloor = PNmeasured - 20log(N+P) - 10log(f_{PFD})
where:
pnNfloor = normalized phase noise floor in dBc/Hz
PNmeasured = in-band phase noise measurement in dBc/Hz
20log(N+P) = divider ratio of feedback loop
10log(f_{PFD}) = PFD update frequency in Hz

APPLICATION INFORMATION ON THE CLOCK GENERATION FOR INTERPOLATING DACS WITH THE CDCM7005

The CDCM7005, with its specified phase noise performance, is an ideal sampling clock generator for high speed ADCs and DACs. The CDCM7005 is especially of interest for the new high speed DACs, which have integrated interpolation filter. Such DACs achieve sampling rates up to 500 MSPS. This high data rate can typically not be supported from the digital side driving the DAC (e.g., DUC, digital up-converter). Therefore, one approach to interface the DUC to the DAC is the integration of an interpolation filter within the DAC to reduce the data rate at the digital input of the DAC. In 3G systems, for example, a common sampling rate of a high speed DAC is 491.52 MSPS. With a four times interpolation of the digital data, the required input data rate results into 122.88 MSPS, which can be supported easily from the digital side. The DUC GC5016, which supports up to four WCDMA carriers, provides a maximum output data rate of 150 MSPS. An example is shown in Figure 26, where the CDCM7005 supplies the clock signal for the DUC/DDC and ADC/DAC.

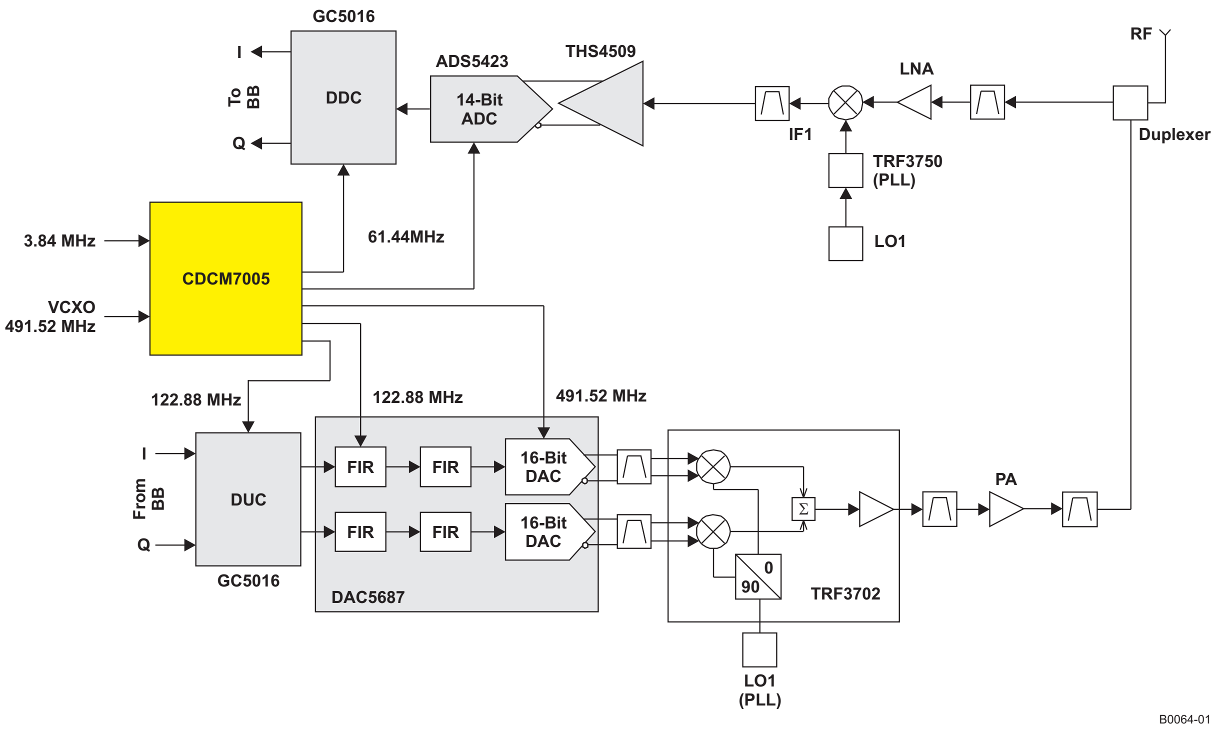


Figure 26. CDCM7005 as a Clock Generator for High Speed ADCs and DACs

The generation of the two required clock signals (data input clock, clock for DAC) for such an interpolating DAC can be done in different ways. The recommended way is to use the CDCM7005, which generates the fast sampling clock for the DAC from the data input clock signal. The DAC5687 demands that the edges of the two input clocks must be phase aligned within ±500 ps for latching the data properly. This phase alignment is well achieved with the CDCM7005, which assures a maximum skew of 70 ps of the different different outputs to each other.

AC-Coupled Interface to ADC/DAC

Another advantage of this clock solution is that the ADC or DAC can be driven directly in an ac-coupling interface as shown in Figure 27, with an external termination in a differential configuration. There is no need for a transformer to generate a differential signal from a single-ended clock source.

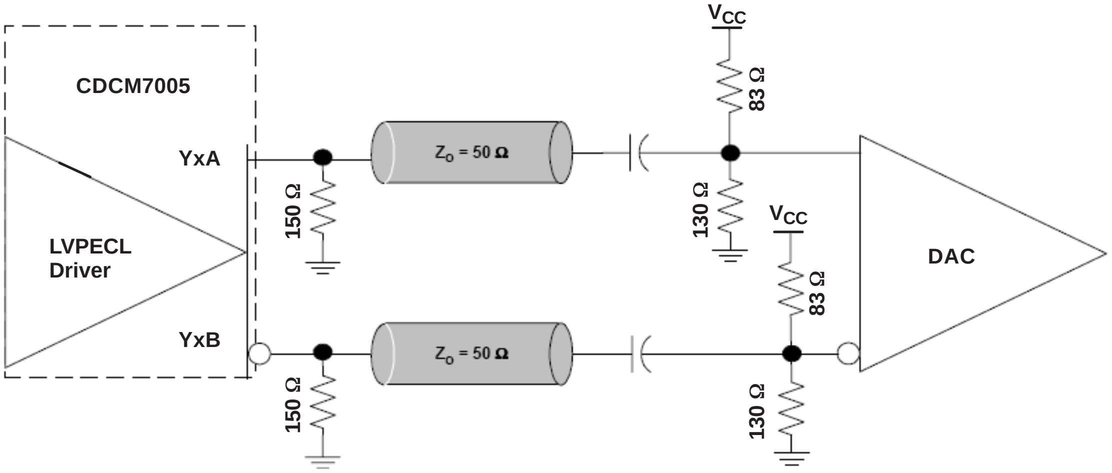


Figure 27. Driving DAC or ADC With PECL Output of the CDCM7005

REVISION HISTORY

Changes from Original (June 2005) to Revision A	Page
• Changed data sheet from Product Preview to Production data.	1

Changes from Revision A (June 2005) to Revision B	Page
• Added minor updates.	1

Changes from Revision B (October 2005) to Revision C	Page
• Changed N2, From: 1 To: 0	22
• Changed N3, From: 1 To: 0	22
• Changed N3, From: 1 To: 0	22
• Changed N2, From: 1 To: 0	22

Changes from Revision C (December 2007) to Revision D — Page

- Changed VCC pin text From: 3.3-V supply. There is no internal connection between V_{CC} and AV_{CC}. It is recommended that AV_{CC} use its own supply filter. To: 3.3-V supply. V_{CC} and AV_{CC} should always have the same supply voltage. It is recommended that AV_{CC} use its own supply filter. 4
- Added text to the CTRL_LE pin - Unused or floating inputs must be tied to proper logic level. A 20kΩ or larger pull−up resistor to VCC is recommended. 4
- Added text to the CTRL_CLK pin - Unused or floating inputs must be tied to proper logic level. A 20kΩ or larger pull−up resistor to VCC is recommended. 4
- Added text to the CTRL_DATA pin - Unused or floating inputs must be tied to proper logic level. A 20kΩ or larger pull−up resistor to VCC is recommended. 4
- Added text to the $\overline{PD}$ pin - It is recommended to ramp up the $\overline{PD}$ with the same time as V_{CC} and AV_{CC} or later. The ramp up rate of the $\overline{PD}$ should not be faster than the ramp up rate of V_{CC} and AV_{CC}. 4
- Added text to the SPI CONTROL INTERFACE section - Unused or floating inputs must be tied to proper logic level. A 20kΩ or larger pull−up resistor to VCC is recommended. 17
- Added text to the SPI CONTROL INTERFACE section - It is recommended to program Word 0, Word 1, Word 2 and Word 3 right after power up and $\overline{PD}$ becomes HIGH. 17
- Changed From: RES To: GTME 21
- Changed From: RES To: PFDFC 21

Changes from Revision D (August 2009) to Revision E — Page

- Changed PLL_LOCK pin description, replaced cycle-slip text. 5
- Changed Note 1 of table Word 3 21
- Changed table Word 3, Cycle Slip (Bit 6) To: Frequency Offset 21
- Changed table Lock-Detect Window (Word 3) - Clip slip To: Frequency offset, and Note 2 23
- Changed the Frequency Hold-Over Mode section 29
- Changed text From: Cycle-Slip To: Frequency Offset in Figure 22 30

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCM7005RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	CDCM7005	Samples
CDCM7005RGZRG4	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	CDCM7005	Samples
CDCM7005RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	CDCM7005	Samples
CDCM7005RGZTG4	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	CDCM7005	Samples
CDCM7005ZVA	ACTIVE	BGA	ZVA	64	348	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85	CDCM7005	Samples
CDCM7005ZVAR	ACTIVE	BGA	ZVA	64	1000	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85	CDCM7005	Samples
CDCM7005ZVAT	ACTIVE	BGA	ZVA	64	250	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85	CDCM7005	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF CDCM7005 :

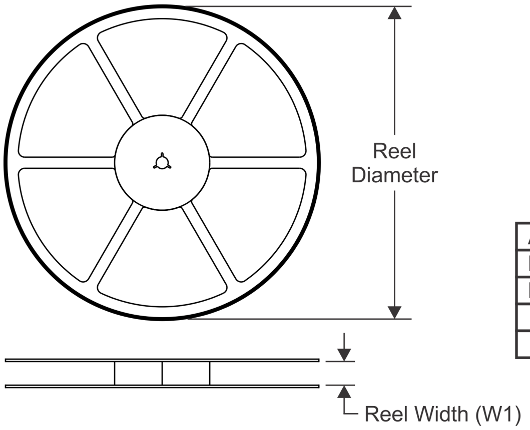
- Space: CDCM7005-SP

NOTE: Qualified Version Definitions:

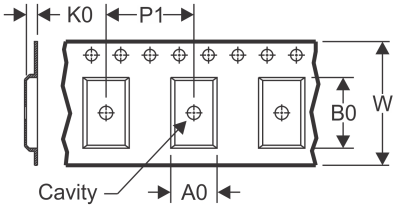
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

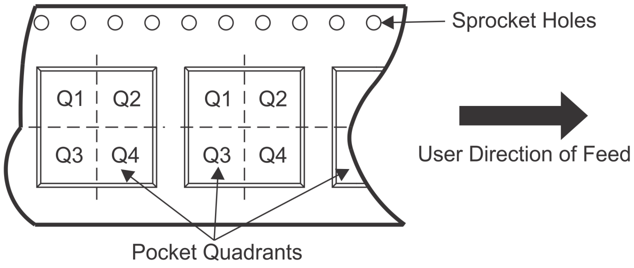


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

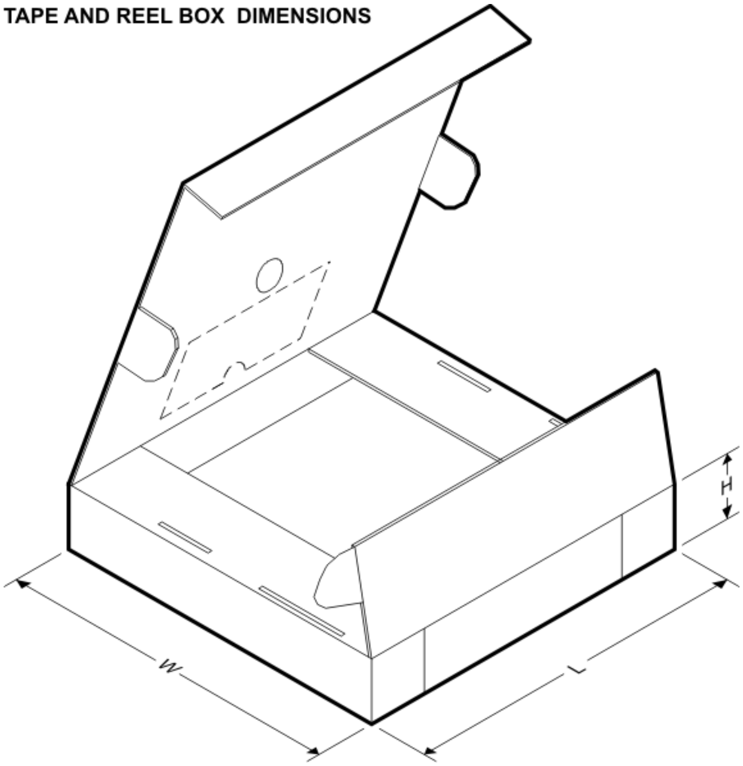
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM7005RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDCM7005RGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDCM7005ZVAR	BGA	ZVA	64	1000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1
CDCM7005ZVAT	BGA	ZVA	64	250	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1

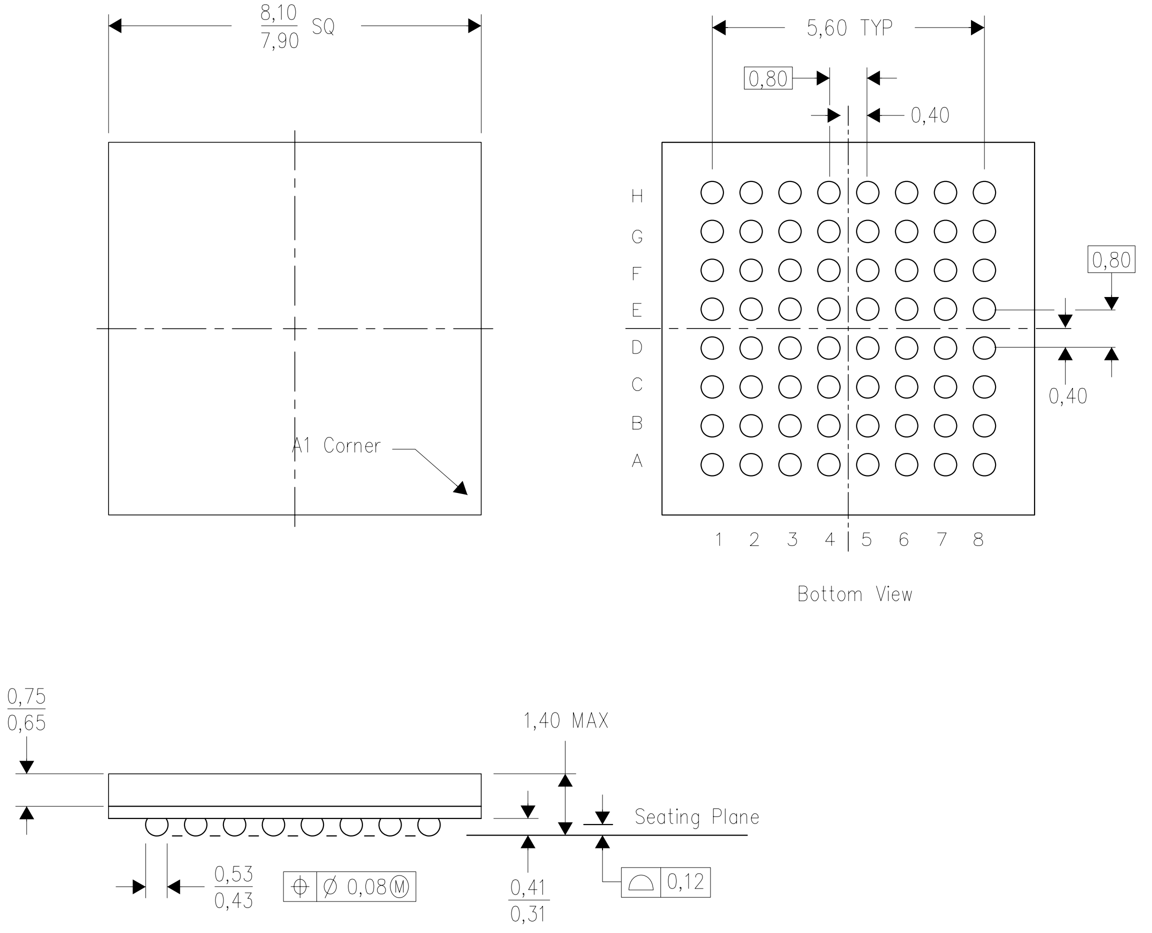
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM7005RGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
CDCM7005RGZT	VQFN	RGZ	48	250	336.6	336.6	28.6
CDCM7005ZVAR	BGA	ZVA	64	1000	336.6	336.6	28.6
CDCM7005ZVAT	BGA	ZVA	64	250	336.6	336.6	28.6

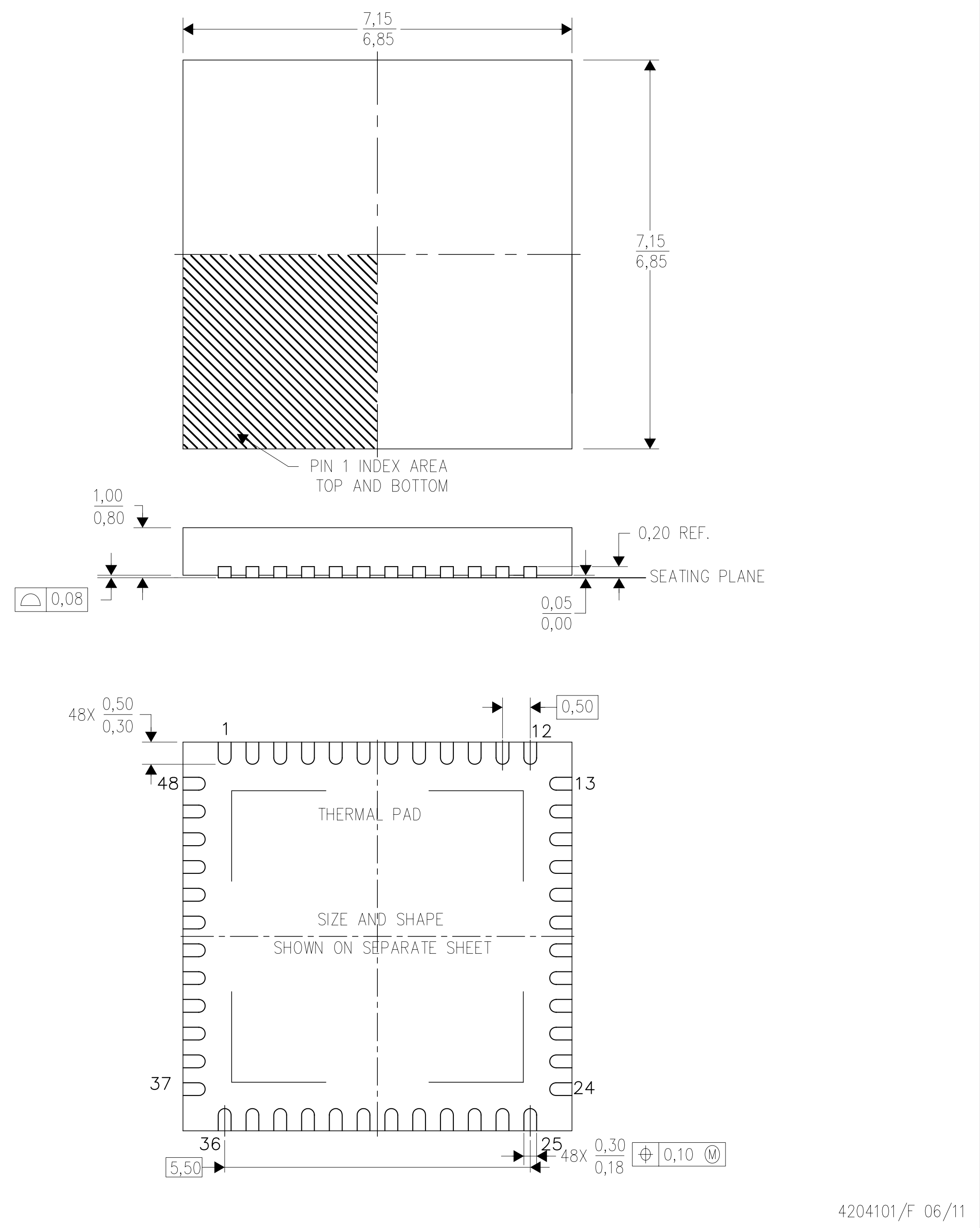
ZVA (S-PBGA-N64) PLASTIC BALL GRID ARRAY



4204388/B 08/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free package.

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

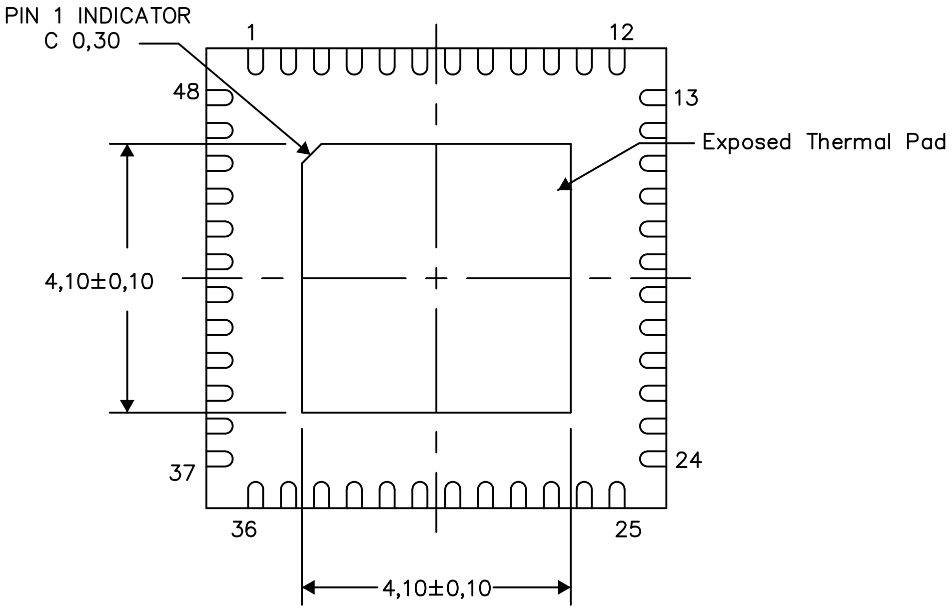
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



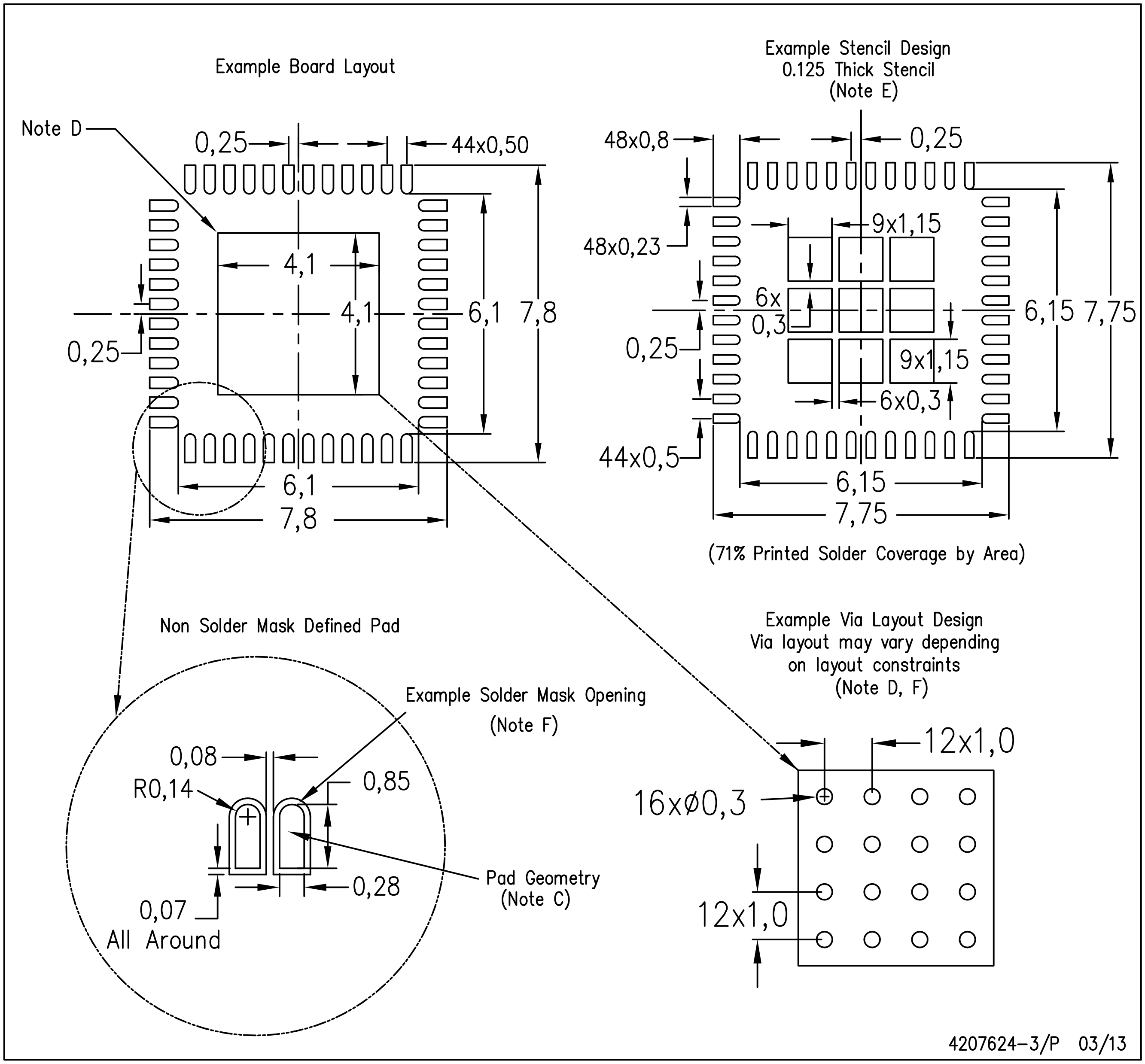
Bottom View

Exposed Thermal Pad Dimensions

4206354-3/T 03/13

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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