CIRRUS LOGIC

CL-CD180

Product Bulletin

Intelligent Octal-Channel Asynchronous Communications Controller

FEATURES

Key features:

- Eight full-duplex asynchronous channels
- Sophisticated Interrupt schemes -
  - Vectored interrupts
  - *Fair- Share Interrupt* ™
  - *Good Data Interrupt* ™ for improved throughput
  - Simultaneous interrupt requests for three classes of interrupts: Rx, Tx and modem state changes
- On-chip interrupt scanner to manage interrupts among all channels
- Improved host/controller software interface
- Generation and detection of four special characters or two-character pairs per channel
- On-chip Flow Control -
  - In-band (Xon, Xoff generation and detection)
  - Out-of-band (DTR/DSR or RTS/CTS)
- On-chip FIFO – 8 bytes each for Rx, Tx and Status FIFOs
- Line break detection and generation
- Multi-chip daisy-chain cascading feature
- Two timers per channel
- Echo mode
- Excellent diagnostic features - local and remote

Other features:

- Independent baud rate generators for each transmitter and receiver to support data rates of up to 38.4Kbps
- 5-8 bits per character
- 1, 1 1/2 or 2 Stop bits
- Odd, even, forced or no parity
- Four modem / general purpose I/O signals per channel
- System clock – up to 10MHz

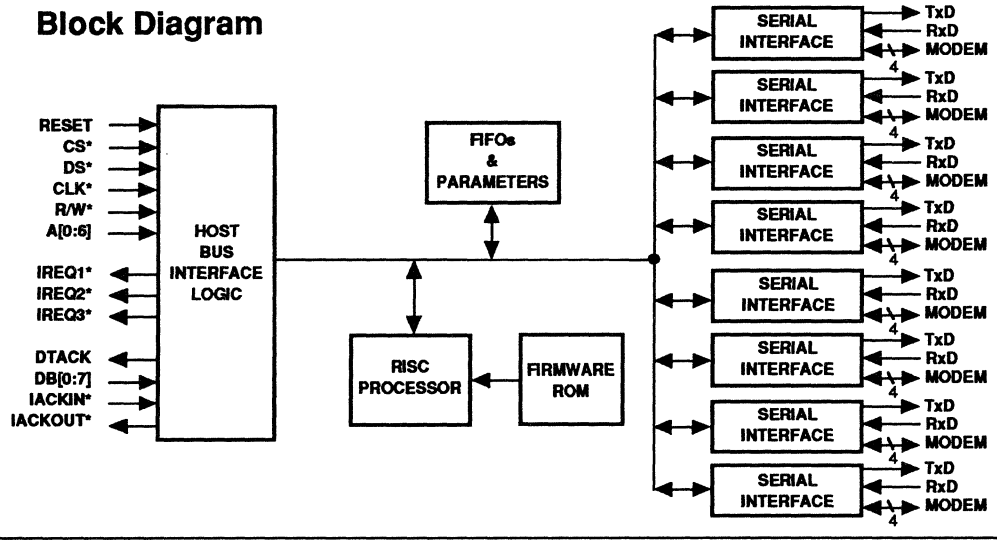
Technology:

- S/LA™ design technology
- Low power advanced CMOS process technology
- 84-pin PLCC

Application Areas:

- Communications Processors
- Terminal servers
- Protocol converters
- Statistical/T1 Mux
- Data Concentrators
- Cluster controllers

Functional Block Diagram



OVERVIEW

The CL-CD180 is a single chip VLSI communications controller which can support eight independent full duplex asynchronous serial communications channels. Each channel is capable of transmitting and receiving data independently at selectable baud rates up to 38.4Kbps. Baud rates are derived directly from the system clock, thus requiring no additional clock source.

Several key features of the CD180 design significantly improve system-level performance: vectored interrupt, good data transfer scheme, on-chip interrupt scanner, on-chip FIFOs and a greatly improved host-to-controller interface using context switching. These features eliminate numerous microprocessor overhead tasks, resulting in more than a five-fold improvement in system throughput at the interrupt servicing level.

Performance improvement hardware functions included in the CL–CD180 are:

FIFO – 24 bytes of FIFO are dedicated to each channel partitioned as 8 bytes for transmitter, 8 bytes for receiver, and 8 bytes for status. The Receive FIFO has a user-programmable threshold to match the system requirements. Receive FIFO threshold programming range is from 1-8 characters. The transmit FIFO will interrupt the host only when it is empty.

Interrupt structure – Three interrupt signals (IREQ[1:3]) are used. Each IREQ signal represents one of the three interrupt groups: transmit data, receive data and modem signal state changes. Additional priority arbitration can be achieved externally using a priority encoder circuit or any other logic to resolve priority among multiple communications or peripheral devices.

Scanner – An on-chip scanner is used to manage and resolve interrupts from each channel. The three groups of interrupts are monitored separately.

Vectored Interrupt – Upon servicing by the host, an interrupt vector will be generated by the controller to convey the controller ID number as well as the interrupt group to be serviced. This allows the host software to jump directly into the proper interrupt service routine reducing the amount of interaction between the host and the controller to determine the nature of the interrupt.

Good Data Interrupt™ – If data transfer is for good data, the host is advised of the number of consecutive good data bytes in the FIFO, allowing the host to read data without further status queries, until all good data has been transferred.

Fair Share Interrupt™ scheme – To ensure equal service of all channels, a *Fair Share* scheme is used for each interrupt group. No channel can interrupt for the same condition until all others have a chance to be serviced for the same interrupt condition.

Improved Host/Controller Interface – A common set of registers is used to facilitate the host/controller interface including: Receive Data Register, Transmit Data Register and Status Register. All channel-related information is maintained by the controller transparent to the host. The controller uses context switching to route the proper channel-related information to these registers for presentation to the host. Using this technique, the host only needs to monitor one set of addresses, letting the controller provide the proper channel number. This feature significantly increases system throughput by greatly reducing the number of addressing cycles. When a large number of data bytes needs to be transferred or the number of channels transferring data increases, the advantage of this feature quickly becomes apparent.

Flow control /special character detection and generation – Both in-band and out-of-band flow control can be supported by the controller independently for each channel.

In-band flow control using Xon, Xoff – The controller can detect and generate four special flow control characters such as Xoff, Xon or any other patterns. Xon, Xoff characters can be programmed to be single characters or a double character sequence. The user may invoke the automatic mode or control the flow based on Special Character detect status.

Out-of-band flow control using modem control signals – RTS/CTS and DTR/DSR are provided in pairs to support flow control.

SIGNAL DESCRIPTIONS – 84-PIN PLCC

SYMBOL	TYPE	DESCRIPTION
Vcc	I	Power Supply.
GND	I	Ground.
RESET*	I	RESET*: An active low signal asynchronously resets any device activity and clears the mode, command and status registers. During RESET*, CLK must be active. A minimum of five CLK periods is required.
CLK	I	SYSTEM CLOCK input: Up to 10 Mhz can be used as the master clock.
A [0:6]	I	ADDRESS BITS 0-6: Select internal registers of the selected channel. A6 high selects a Global register. A6 low selects a Channel register.
DB [0:7]	I/O	DATA BUS 0-7: 8-bit bidirectional data bus for transfer of data, status and commands between the CD180 and the host CPU.
R/W*	I	READ/WRITE*: A high indicates a READ; a low indicates a WRITE .
CS*	I	CHIP SELECT*: When low, an internal register is read or written depending on A [0:6], R/W* . When high, sets the DB[0:7] to high impedance.
DS*	I	DATA STROBE*: An active low signal strobes the data off the data bus.
IREQ [1:3]*	O	INTERRUPT REQUEST [1:3]*: Active low, open drain outputs to indicate that an interrupt is pending. When low, the IREQ signal indicates that an interrupt is pending for that group (Three possible interrupt groups).
IACKIN*	I	INTERRUPT ACKNOWLEDGE INPUT*: System IACK* input or IACKOUT* from previous CD180.
IACKOUT*	O	INTERRUPT ACKNOWLEDGE OUTPUT: This signal is used for cascading multiple CD180s.
DTACK*	O	DATA TRANSFER ACKNOWLEDGE*: Open-drain output. Asserted by the CD180 during any processor-initiated read or write operation to the CD180. Also asserted by the CD180 to indicate a valid interrupt vector on the data bus during a read operation initiated by an interrupt acknowledge.
RxD [0:7]	I	RECEIVE DATA 0-7: Receiver serial data inputs. One per channel.
TxD [0:7]	O	TRANSMIT DATA 0-7: Transmitter serial data outputs. One per channel.
RTS*/GPO0* [0:7]	O	REQUEST TO SEND*/GENERAL PURPOSE OUTPUT 0*[0:7].
CTS*/GPI1* [0:7]	I	CLEAR TO SEND*/GENERAL PURPOSE INPUT 1* [0 : 7].
DTR*/GPO2* [0:7]	O	DATA TERMINAL READY*/GENERAL PURPOSE OUTPUT 2* [0:7].
DSR*/GPI3* [0:7]	I	DATA SET READY*/GENERAL PURPOSE INPUT 3* [0 :7].
TEST	I	TEST: This is a test function pin and is active high. This pin is not intended for general use and should be tied low at all times.

(*) denotes active low signal

ADVANTAGES

Unique Features	Benefits
On-chip FIFO	Greatly reduces real-time interrupt response time requirement of the MPU. Simplifies system tasks in a real-time multitasking environment.
User-programmable Receive FIFO threshold	Enables tailoring of interrupt conditions to different system requirements. Facilitates software development.
Good Data Interrupt™ for transferring multiple bytes of data	Reduces the number of MPU cycles required to transfer data. Improves system performance significantly. Frees up extra bandwidth for MPU to perform higher level system tasks.
Interrupt vectoring by device ID and type of service required.	Allows direct jump into proper interrupt service routine, improving overall system performance.
Automatic flow control	Real-time control of data flow reduces risk of losing valuable data.
Advanced CMOS process	Provides high performance with low power consumption and low heat dissipation.

REGISTER TABLES

Global Registers

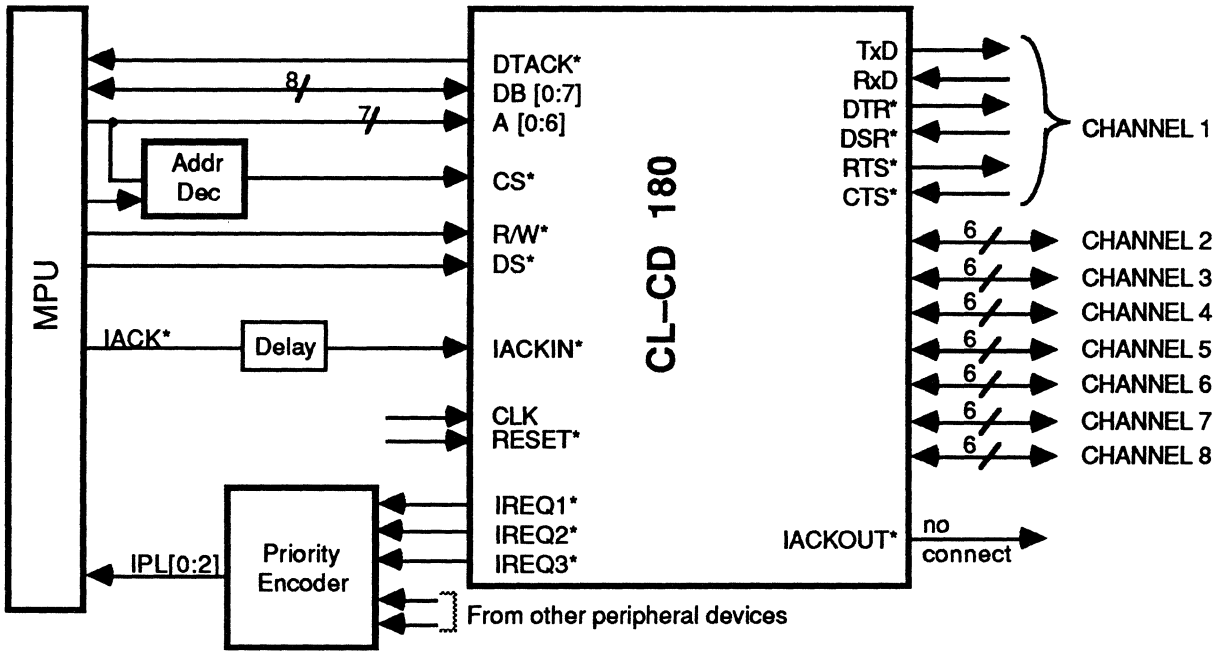
REGISTER	ACCESS	DESCRIPTION/FUNCTION
CAR	R/W	Channel Access
EOIR	W	End of Interrupt
GICR	R/W	Global Interrupting Channel
GIVR	R/W	Global Interrupt Vector
PILR1	R/W	Priority Interrupt Level 1
PILR2	R/W	Priority Interrupt Level 2
PILR3	R/W	Priority Interrupt Level 3
PPR_H	R/W	Prescaler Period High
PPR_L	R/W	Prescaler Period Low
RCSR	R	Receive Character Status
RDCR	R	Receive Data Count
RDR	R	Receive Data
TDR	W	Transmit Data

Channel Registers

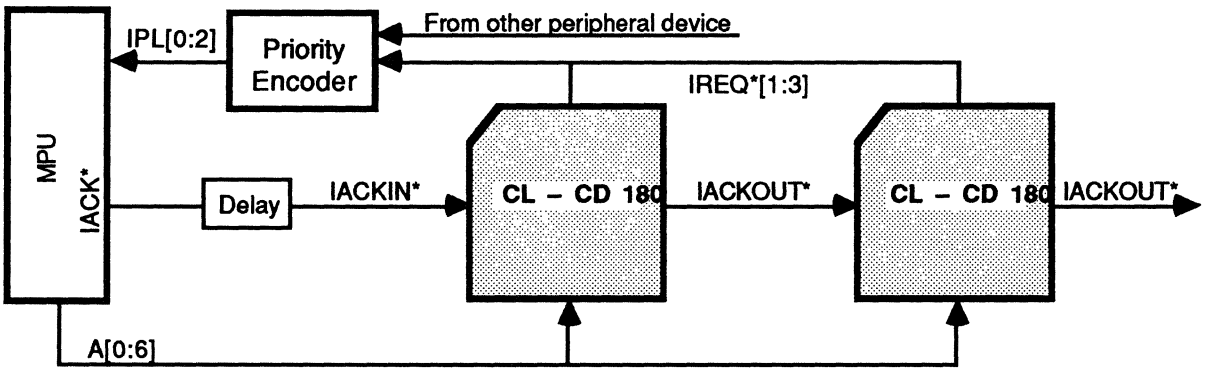
REGISTER	ACCESS	DESCRIPTION/FUNCTION
CCR	R/W	Channel Command
CCSR	R	Channel Control Status
COR1	R/W	Channel Option 1
COR2	R/W	Channel Option 2
COR3	R/W	Channel Option 3
COR4	R/W	Channel Option 4
IER	R/W	Interrupt Enable
MCOR1	R/W	Modem Change Option 1
MCOR2	R/W	Modem Change Option 2
MCR	R/W	Modem Change
MSVR	R/W	Modem Signal Value
$RBPR_H$	R/W	Receive Baud Rate Period – High
$RBPR_L$	R/W	Receive Baud Rate Period – Low
RTPR	R/W	Receive Timeout Period
SCHR1	R/W	Special Character 1
SCHR2	R/W	Special Character 2
SCHR3	R/W	Special Character 3
SCHR4	R/W	Special Character 4
$TBPR_H$	R/W	Transmit Baud Rate Period – High
$TBPR_L$	R/W	Transmit Baud Rate Period – Low

SYSTEM BLOCK DIAGRAMS

Single Device System



Multiple Device System



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Direct Sales Offices

Domestic

N. CALIFORNIA
San Jose
TEL: 408/436-7110
FAX: 408/437-8960

S. CALIFORNIA
Laguna Hills
TEL: 714/472-3939
FAX: 714/472-4804

Thousand Oaks
TEL: 805/371-5381
FAX: 805/371-5382

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Boulder, CO
TEL: 303/939-9739
FAX: 303/440-5712

NORTH CENTRAL AREA
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TEL: 708/449-7715
FAX: 708/449-7804

SOUTH CENTRAL AREA
Austin, TX
TEL: 512/794-8490
FAX: 512/794-8069

NORTHEASTERN AREA
Andover, MA
TEL: 508/474-9300
FAX: 508/474-9149

Philadelphia, PA
TEL: 215/251-6881
FAX: 215/651-0147

SOUTH EASTERN AREA
Boca Raton, FL
TEL: 407/994-9883
FAX: 407/994-9887

Atlanta, GA
TEL: 404/263-7601
FAX: 404/729-6942

International

JAPAN
Kanagawa-Ken
TEL: 81/462-76-0601
FAX: 81/462-76-0291

SINGAPORE
TEL: 65/3532122
FAX: 65/3532166

TAIWAN
Taipei
TEL: 886/2-718-4533
FAX: 886/2-718-4526

GERMANY
Herrsching
TEL: 49/8152-2030
FAX: 49/8152-6211

The Company

Cirrus Logic, Inc., is a leading supplier of high-integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

† U.S. Patent No. 4,293,783

CIRRUS LOGIC, Inc., 3100 West Warren Ave. Fremont, CA 94538
TEL: 415/623-8300 FAX: 415/226-2160