National Semiconductor

COP440/COP441/COP442 and COP340/COP341/COP342 Single-Chip N-Channel Microcontrollers

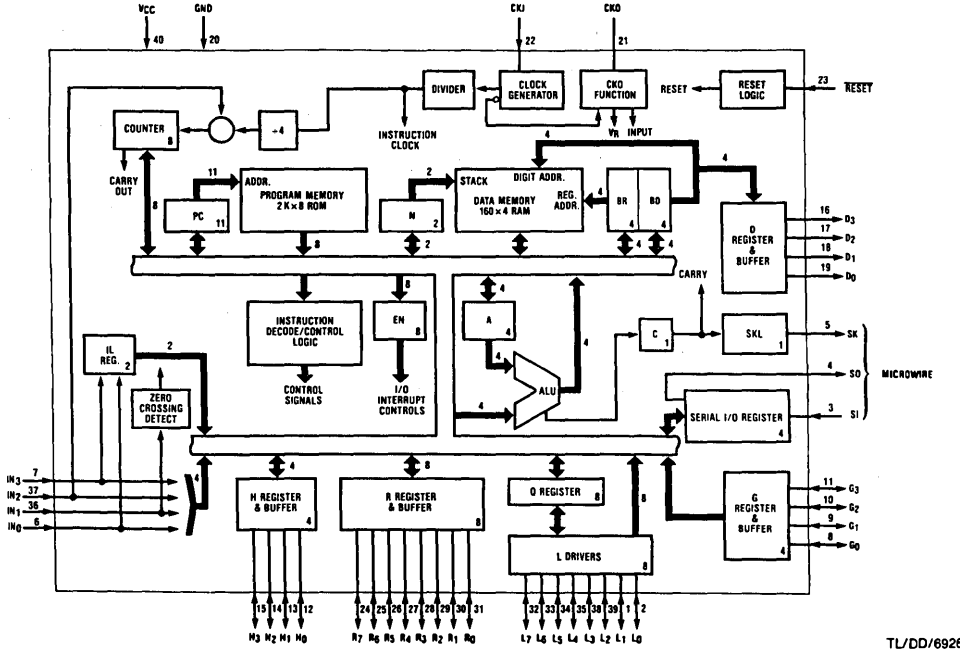
General Description

The COP440, COP441, COP442, COP340, COP341, and COP342 Single-Chip N-Channel Microcontrollers are members of the COPS™ microcontrollers family, fabricated using N-channel, silicon gate MOS technology. These are complete microcontrollers with all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, various output configuration options, and an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and data manipulation. The COP440 is a 40-pin chip and the COP441 is a 28-pin version of the same circuit (12 I/O lines removed). The COP442 is a 24-pin version (4 more input lines removed). The COP340, COP341, COP342 are functional equivalents of the above devices respectively, but operate with an extended temperature range (−40°C to +85°C). Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized controller oriented processor at a low end-product cost.

Features

- Enhanced, more powerful instruction set
- 2k x 8 ROM, 160 x 4 RAM
- 35 I/O lines (COP440)
- Zero-crossing detect circuitry with hysteresis
- True multi-vectored interrupt from 4 selectable sources (plus restart)
- Four-level subroutine stack (in RAM)
- 4 μs cycle time
- Single supply operation (4.5V–6.3V)
- Programmable time-base counter
- Internal binary counter/register with MICROWIRE™ compatible serial I/O
- General purpose and TRI-STATE® outputs
- TTL/CMOS compatible in and out
- LED drive capability
- MICROBUS™ compatible
- Software/hardware compatible with other members of the COP400 family
- Extended temperature range devices COP340, COP341, COP342 (−40°C to +85°C)
- Compatible dual CPU device available (COP2440 series)

Block Diagram



TL/DD/6926–1

FIGURE 1

COP440/COP441/COP442
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Zero-Crossing Detect Pin Relative to GND	−1.2V to +15V
Voltage at Any Other Pin Relative to GND	−0.5V to +7V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	0.75W at 25°C 0.4W at 70°C
Total Source Current	150 mA
Total Sink Current	75 mA

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 6.3V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})	(Note 3)	4.5	6.3	V
Power Supply Ripple	(Peak to Peak)		0.4	V
Operating Supply Current	(All Inputs and Outputs Open)			
	T_A = 0°C		44	mA
	T_A = 25°C		35	mA
	T_A = 70°C		27	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷16, ÷8)				
Logic High (V_{IH})	V_{CC} = Max	3.0		V
Logic High (V_{IH})	V_{CC} = 5V ±5%	2.0		V
Logic Low (V_{IL})		−0.3	0.4	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		−0.3	0.6	V
$\overline{\text{RESET}}$ Input Levels	(Schmitt Trigger Input)			
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.6	V
Zero-Crossing Detect Input	See *Figure 7*			
Trip Point		−0.15	0.15	V
Logic High (V_{IH}) Limit			12	V
Logic Low (V_{IL}) Limit		−0.8		V
SO Input Level (Test Mode)	(Note 5)	2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	V_{CC} = 5V ±5%	2.0		V
Logic Low		−0.3	0.8	V
Input Levels High Trip Option				
Logic High		3.6		V
Logic Low		−0.3	1.2	V
Input Capacitance			7.0	pF
Hi-Z Input Leakage		−1.0	+1.0	µA

Note 1: Duty Cycle = $t_{WI}/(t_{WI} + t_{WO})$.

Note 2: See Figure for additional I/O Characteristics.

Note 3: V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 4: Exercise great care not to exceed maximum device power dissipation limits when direct-driving LEDs (or sourcing similar loads) at high temperature.

Note 5: SO output "0" level must be less than 0.8V for normal operation.

COP440/COP441/COP442

DC Electrical Characteristics $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 6.3V$ unless otherwise noted (Continued)

Parameter	Conditions	Min	Max	Units
Output Voltage Levels				
Standard Output				
TTL Operation				
Logic High (V_{OH})	$I_{OH} = -100\ \mu A$	2.4		V
Logic Low (V_{OL})	$I_{OL} = 1.6$ mA		0.4	V
CMOS Operation (Note 1)				
Logic High (V_{OH})	$I_{OH} = -10\ \mu A$	$V_{CC} - 0.4$		V
Logic Low (V_{OL})	$I_{OL} = 10\ \mu A$		0.2	V
Output Current Levels				
Standard Output Source Current	$V_{CC} = 4.5V$, $V_{OH} = 2.4V$	−100	−650	μA
LED Direct Drive Output	$V_{CC} = 6V$, $V_{OH} = 2V$			
Logic High (I_{OH})		−2.5	−17	mA
TRI-STATE Output Leakage Current		−2.5	+2.5	μA
CKO Output				
Oscillator Output Option				
Logic High	$V_{OH} = 2V$	−0.2		mA
Logic Low	$V_{OL} = 0.4V$	0.4		mA
V_R RAM Power Supply Option				
Supply Current	$V_R = 3.3V$		3.0	mA
CKI Sink Current (RC Option)	$V_{IH} = 3.5V$, $V_{CC} = 4.5V$	2.0		mA
Input Current Levels				
Zero-Crossing Detect Input				
Resistance	$V_{IH} = 1.0V$	0.9	4.6	kΩ
Input Load Source Current	$V_{IH} = 2.0V$, $V_{CC} = 4.5V$	14	230	μA
Total Sink Current Allowed				
All I/O Combined			75	mA
Each L, R Port			20	mA
Each D, G, H Port			10	mA
SO, SK			2.5	mA
Total Source Current Allowed				
All I/O Combined			150	mA
L Port			120	mA
L_7–L_4			70	mA
L_3–L_0			70	mA
Each L Pin			23	mA
All Other Output Pins			1.6	mA

Note 1: TRI-STATE and LED configurations are excluded.

COP340/COP341/COP342
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Zero-Crossing Detect Pin Relative to GND	−1.2V to +15V
Voltage at Any Other Pin Relative to GND	−0.5V to +7V
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	0.75W at 25°C 0.25W at 85°C
Total Source Current	150 mA
Total Sink Current	75 mA

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 5.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})	(Note 3)	4.5	5.5	V
Power Supply Ripple	(Peak to Peak)		0.4	V
Operating Supply Current	(All Inputs and Outputs Open)			
	$T_A = -40°C$		54	mA
	$T_A = 25°C$		35	mA
	$T_A = 85°C$		25	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷16, ÷8)	V_{CC} = Max	3.0		V
Logic High (V_{IH})		2.2		V
Logic Low (V_{IL})		−0.3	0.3	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		−0.3	0.4	V
$\overline{\text{RESET}}$ Input Levels	(Schmitt Trigger Input)			
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.4	V
Zero-Crossing Detect Input	See *Figure 7*			
Trip Point		−0.15	0.15	V
Logic High (V_{IH}) Limit			12	V
Logic Low (V_{IL}) Limit		−0.8		V
SO Input Level (Test Mode)	(Note 5)	2.2	2.4	V
All Other Inputs	V_{CC} = Max	3.0		V
Logic High		2.2		V
Logic Low		−0.3	0.6	V
Input Levels High Trip Option				
Logic High		3.6		V
Logic Low		−0.3	1.2	V
Input Capacitance			7.0	pF
Hi-Z Input Leakage		−2.0	+2.0	μA

Note 1: Duty Cycle = $t_{WI}/(t_{WI} + t_{WO})$.

Note 2: See Figure for additional I/O Characteristics.

Note 3: V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 4: Exercise great care not to exceed maximum device power dissipation limits when direct-driving LEDs (or sourcing similar loads) at high temperature.

Note 5: SO output "0" level must be less than 0.6V for normal operation.

COP340/COP341/COP342

DC Electrical Characteristics

$-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 5.5V$ unless otherwise noted (Continued)

Parameter	Conditions	Min	Max	Units
Output Voltage Levels				
Standard Output				
TTL Operation				
Logic High (V_{OH})	$I_{OH} = -100\ \mu A$	2.4		V
Logic Low (V_{OL})	$I_{OL} = 1.6$ mA		0.4	V
CMOS Operation (Note 1)				
Logic High (V_{OH})	$I_{OH} = -10\ \mu A$	$V_{CC} - 0.5$		V
Logic Low (V_{OL})	$I_{OL} = 10\ \mu A$		0.2	V
Output Current Levels				
Standard Output Source Current	$V_{CC} = 4.5V$, $V_{OH} = 2.4V$	−100	−800	μA
LED Direct Drive Output	$V_{CC} = 5V$ (Note 4)			
Logic High (I_{OH})	$V_{OH} = 2V$	−1.5	−15	mA
TRI-STATE Output Leakage Current		−5.0	+5.0	μA
CKO Output				
Oscillator Output Option				
Logic High	$V_{OH} = 2V$	−0.2		mA
Logic Low	$V_{OL} = 0.4V$	0.4		mA
V_R RAM Power Supply Option				
Supply Current	$V_R = 3.3V$		4.0	mA
CKI Sink Current (RC Option)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2.0		mA
Input Current Levels				
Zero-Crossing Detect Input				
Resistance	$V_{IH} = 1.0V$	0.9	4.6	kΩ
Input Load Source Current	$V_{IH} = 2.0V$, $V_{CC} = 4.5V$	14	280	μA
Total Sink Current Allowed				
All I/O Combined			75	mA
Each L, R Port			20	mA
Each D, G, H Port			10	mA
SO, SK			2.5	mA
Total Source Current Allowed				
All I/O Combined			150	mA
L Port			120	mA
L_7–L_4			70	mA
L_3–L_0			70	mA
Each L Pin			23	mA
All Other Output Pins			1.6	mA

Note 1: TRI-STATE and LED configurations are excluded.

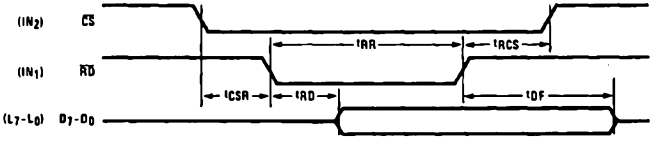
AC Electrical Characteristics

COP440/COP441/COP442: 0°C ≤ T_A ≤ +70°C, 4.5V ≤ V_{CC} ≤ 6.3V unless otherwise noted

COP340/COP341/COP342: − 40°C ≤ T_A ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V unless otherwise noted

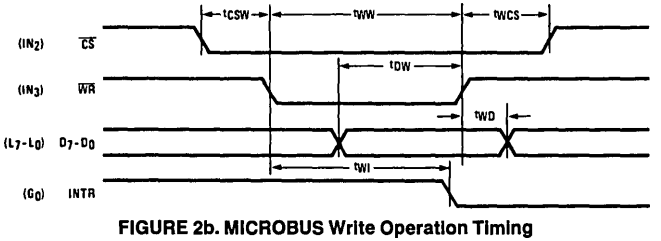
Parameter	Conditions	Min	Max	Units
Instruction Cycle Time-t_E		4.0	10	μs
CKI Frequency	÷16 Mode	1.6	4.0	MHz
	÷8 Mode	0.8	2.0	MHz
	÷4 Mode	0.4	1.0	MHz
Duty Cycle (Note 1)	f_I = 4 MHz	30	60	%
Rise Time	f_I = 4 MHz External Clock		60	ns
Fall Time	f_I = 4 MHz External Clock		40	ns
CKI Using RC *(Figure 9c)*	÷4 Mode			
Frequency	R = 15 kΩ ±5%, C = 100 pF ±10%	0.5	1.0	MHz
Instruction Execution Time-t_E (Note 1)		4.0	8.0	μs
INPUTS: *(Figure 4)*				
SI				
t_{SETUP}		0.3		μs
t_{HOLD}		300		ns
All Other Inputs				
t_{SETUP}		1.7		μs
t_{HOLD}		300		ns
OUTPUT PROPAGATION DELAY	Test Condition: C_L = 50 pF, V_{OUT} = 1.5V			
CKO				
t_{pd1}, t_{pd0}	Crystal Input		0.17	μs
t_{pd1}, t_{pd0}	Schmitt Trigger Input		0.3	μs
SO, SK				
t_{pd1}, t_{pd0}	R_L = 2.4 kΩ		1.0	μs
All Other Outputs	R_L = 5.0 kΩ		1.4	μs
MICROBUS TIMING	C_L = 100 pF, V_{CC} = 5V ±5%			
Read Operation *(Figure 2a)*	TRI-STATE Outputs			
Chip Select Stable Before $\overline{RD}$-t_{CSR}		65		ns
Chip Select Hold Time for $\overline{RD}$-t_{RCS}		20		ns
$\overline{RD}$ Pulse Width-t_{RR}		400		ns
Data Delay from $\overline{RD}$-t_{RD}			375	ns
$\overline{RD}$ to Data Floating-t_{DF}			250	ns
Write Operation *(Figure 2b)*				
Chip Select Stable Before $\overline{WR}$-t_{CSW}		65		ns
Chip Select Hold Time for $\overline{WR}$-t_{WCS}		20		ns
$\overline{WR}$ Pulse Width-t_{WW}		400		ns
Data Set-Up Time for $\overline{WR}$-t_{DW}		320		ns
Data Hold Time for $\overline{WR}$-t_{WD}		100		ns
INTR Transition Time from $\overline{WR}$-t_{WI}			700	ns

Note 1: Variation due to the device included.



TL/DD/6926-2

FIGURE 2a. MICROBUS Read Operation Timing

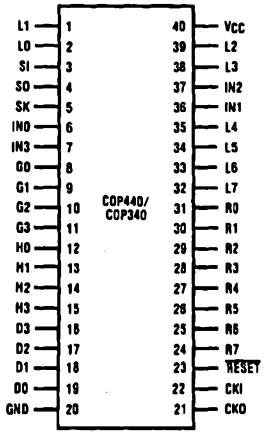


TL/DD/6926-3

FIGURE 2b. MICROBUS Write Operation Timing

Connection Diagrams

Dual-In-Line Package

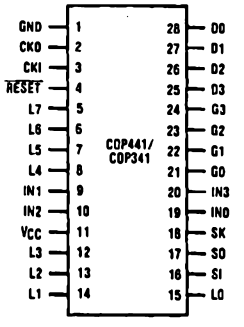


TL/DD/6926-4

Top View

Order Number COP440-XXX/D or COP340-XXX/D
See NS Hermetic Package Number D40C
Order Number COP440-XXX/N or COP340-XXX/N
See NS Molded Package Number N40A

Dual-In-Line Package

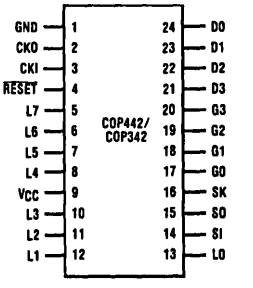


TL/DD/6926-5

Top View

Order Number COP441-XXX/D or COP341-XXX/D
See NS Hermetic Package Number D28C
Order Number COP441-XXX/N or COP341-XXX/N
See NS Molded Package Number N28B

Dual-In-Line Package



TL/DD/6926-6

Top View

Order Number COP442-XXX/D or COP342-XXX/D
See NS Hermetic Package Number D24C
Order Number COP442-XXX/N or COP342-XXX/N
See NS Molded Package Number N24A

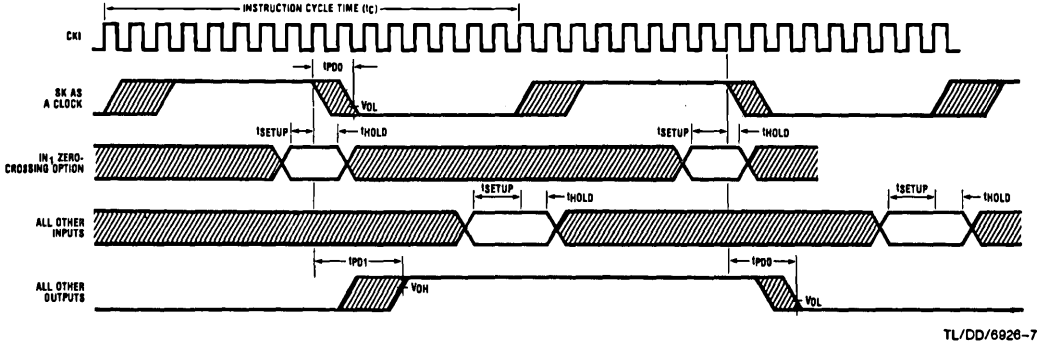
FIGURE 3

Pin Descriptions

Pin	Description
L_7–L_0	8-bit Bidirectional I/O Port with TRI-STATE
G_3–G_0	4-bit Bidirectional I/O Port
D_3–D_0	4-bit General Purpose Output Port
IN_3–IN_0	4-bit General Purpose Input Port (Not Available on COP442/COP342)
SI	Serial Input
SO	Serial Output (or General Purpose Output)
SK	Logic-Controlled Clock (or General Purpose Output)

Pin	Description
CKI	System Oscillator Input
CKO	System Oscillator Output (or General Purpose Input or RAM Power Supply)
$\overline{RESET}$	System Reset Input
V_{CC}	Power Supply
GND	Ground
H_3–H_0	4-bit Bidirectional I/O Port (COP440/COP340 Only)
R_7–R_0	8-Bit Bidirectional I/O Port with TRI-STATE (COP440/COP340 Only)

Timing Diagram



TL/DD/6926-7

FIGURE 4. Input/Output Timing Diagrams (Divide by 16 Mode)

Functional Description

The block diagram of the COP440 is shown in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2.0V). When a bit is reset, it is a logic "0" (less than 0.8V).

PROGRAM MEMORY

Program Memory consists of a 2,048 byte ROM. As can be seen by an examination of the COP440 instruction set, these words may be program instructions, constants, or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, LQID, and LID instructions, ROM must often be thought of as being organized into 32 pages of 64 words each.

ROM addressing is accomplished by an 11-bit PC register. Its binary value selects one of the 2,048 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

DATA MEMORY

Data memory consists of a 640-bit RAM, organized as 10 data registers of 16 4-bit digits. RAM addressing is implemented by an 8-bit B register whose upper 4 bits (Br) select 1 of 10 (0–9) data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into, or from, or exchanged with the A register (accumulator), it may also be loaded into or from the Q latches, L port, R port, EN register, and T counter (internal time base counter). RAM may also be loaded from 4 bits of a ROM word. RAM addressing may also be performed directly to the lower 8 registers by the LDD and XAD instructions based upon the 7-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs. RAM register 8 (Br = 8) also serves as a subroutine stack. Note that it is possible, but not recommended, to alter the contents of the stack by normal data memory access commands.

INTERNAL LOGIC

The 4-bit A register (accumulator) is the source and destination register for most I/O arithmetic, logic, and data memory access operations. It can also be used to load the Br and Bd portions of the B register, N register, to load and input 4 bits of the 8-bit Q latch, EN register, or T counter, to input 4 bits of a ROM word, L or R I/O port data, to input 4-bit G, H, or IN ports, and to perform data exchanges with the SIO register. The accumulator is cleared upon reset.

A 4-bit adder performs the arithmetic and logic functions of the COP440, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below).

The 8-bit T counter is a binary up counter which can be loaded to and from M and A. The input to this counter is software selectable from two sources: the first coming from a divide-by-four prescaler (from instruction cycle frequency) thus providing a 10-bit time base counter; the second coming from IN_2 input, changing the T counter into an 8-bit external event counter (see EN register below). In this mode, a low-going pulse ("1" to "0") of at least 2 instruction cycles wide will increment the counter. When the counter overflows, an overflow flag will be set (see SKT instruction below) and an interrupt signal will be sent to processor X. The T counter is cleared on reset.

Four general-purpose inputs, IN_3–IN_0, are provided; IN_1, IN_2 and IN_3 may be selected, by a mask-programmable option, as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in MICROBUS applications; IN_1, by another mask-programmable option, can be selected as a true zero-crossing detector with the output triggering an interrupt or being interrogated by an instruction. These two mask-programmable options are mutually exclusive.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G_0 may be mask-programmed as an output for MICROBUS applications.

The H register contents are outputs to a 4-bit general-purpose bidirectional I/O port.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control. With the MICROBUS option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU. Note that unlike most other COPS controllers, Q is cleared on reset.

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS option allows L I/O port data to be latched into the Q register. The L I/O port can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa–Sg and decimal point segments of the display.

The R register, when enabled, outputs to an 8-bit general-purpose, bidirectional, I/O port.

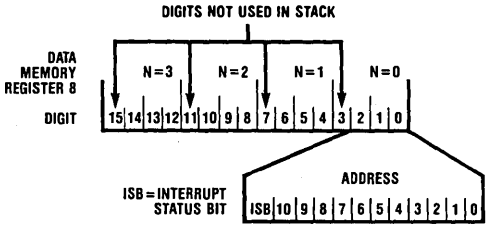
The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and COPS peripherals, or as a binary counter (depending on the contents of the EN register; see EN register description, below). Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream.

The XAS instruction copies the C flag into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the instruction cycle clock.

The 2-bit N register is a stack pointer to the data memory register 8 where the subroutine return address is located. It points to the next location where the address may be stored

Functional Description (Continued)

and increments by 1 after each push of the stack, and decrements by 1 before each pop. The N register can be accessed by exchanging its value with A and is cleared on reset. The stack is 4 addresses deep, 12 bits wide, and does not check for overflow or empty conditions. The RAM digit locations where the addresses are stored are shown in *Figure 5*. The LSBs of the addresses are at digits 0, 4, 8, and 12. The MSBs of digits 2, 6, 10, and 14 contain an interrupt status bit (see Interrupt description, below). The four unused digits (3, 7, 11, and 15) can be used as general data storage. When a subroutine call or interrupt occurs, an 11-bit return address and an interrupt status bit are stored in the stack. The N register is then incremented. When a RET or RETSK instruction is executed, the N register is decremented and then the return address is fetched and loaded into the program counter. The address and interrupt status bits remain in the stack, but will be overwritten when the next subroutine call or interrupt occurs.



TL/DD/6926–8

FIGURE 5. Subroutine Return Address Stack Organization

The EN register in an internal 8-bit register loaded under program control by the LEI instruction (lower 4 bits) or by the CAME instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register.

0. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register left shifting 1 bit each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. The SK output becomes a logic-controlled clock.
1. With EN_1 set, interrupt is enabled with EN_4 and EN_5 selecting the interrupt source. Immediately following an interrupt, EN_1 is reset to disable further interrupts.
2. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O port. Resetting EN_2 disables the L drivers, placing the L I/O port in a high-impedance input state. A special feature of the COP440 and COP441 is that the MICROBUS option will change the function of this bit to disable any writing into G_0 when EN_2 is set.
3. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains set to "0". Table I below provides a summary of the modes associated with EN_3 and EN_0.
4. EN_5 and EN_4 select the source of the interrupt signal.
5. The possible sources are as follows:

EN_5	EN_4	Interrupt Source
0	0	IN_1 (low-going pulse)
0	1	CKO input (if mask-programmed as an input)
1	0	Zero-crossing (or IN_1 level transition)
1	1	T counter overflows

   EN_4 determines the interrupt routine location.
6. With EN_6 set, the internal 8-bit T counter will use IN_2 as its input. With EN_6 reset, the input to the T counter is the output of a divide by four prescaler (from instruction cycle frequency), thus providing a 10-bit time-base counter.
7. With EN_7 set, the R outputs are enabled; if $EN_7 = 0$, the R outputs are disabled.

INTERRUPT

The following features are associated with the interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC+1) together with an interrupt status bit, onto the program counter stack residing in data memory. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset. If EN_4 is reset, the next program address is hex 100; if EN_4 is set, the next program address is hex 300; thus providing a different interrupt location for different interrupt sources.

TABLE I. Enable Register Modes — Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

Functional Description (Continued)

b. An interrupt will be acknowledged only after the following conditions are met:

1. EN_1 has been set.
2. For an external interrupt input, the signal pulse must be at least two instruction cycles wide.
3. A currently executing instruction has been completed.
4. All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. The instruction at hex address 0FF must be a NOP.

d. A CAME or LEI instruction may be put immediately before the RET instruction to re-enable interrupts.

e. If the interrupt signal source is being changed, the interrupt must be disabled prior to, or at, the same time with the change to avoid false interrupts. An interrupt may be enabled only if the interrupt source is not changing. A sample code for changing the interrupt source and enabling the interrupt is as follows:

```
CAME        ; disable interrupt & alter interrupt source
SMB  1      ; set interrupt enable bit
CAME        ; enable interrupt
```

f. An interrupt status bit is stored together with the return address in the stack. The status bit is set if an interrupt occurs at a point in the program where the next instruction is to be skipped; upon returning from the interrupt routine, this set status bit will cause the next instruction to be skipped. Subroutine and interrupt nesting inside interrupt routines are allowed. Note that this differs from the COP420/420C/420L/444L series.

MICROBUS INTERFACE
(not available in COP442, COP342)

The COP440 series has an option which allows them to be used as peripheral microprocessor devices, inputting and outputting data from and to a host microprocessor (μP). IN_1, IN_2 and IN_3 general purpose inputs become MICROBUS-compatible read-strobe, chip-select, and write-strobe lines, respectively. IN_1 becomes $\overline{RD}$—a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μP. IN_2 becomes $\overline{CS}$—a logic "0" on this line selects the COPS processor as the μP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components. IN_3 becomes $\overline{WR}$—a logic "0" on this line will write bus data from the L ports to the Q latches for input to the COPS processor. G_0 becomes INTR, a "ready" output, reset by a write pulse from the μP on the $\overline{WR}$ line, providing the "handshaking" capability necessary for asynchronous data transfer between the host CPU and the COPS processor. G_0 output can be separated from other G outputs by the EN_2 bit (see EN description above).

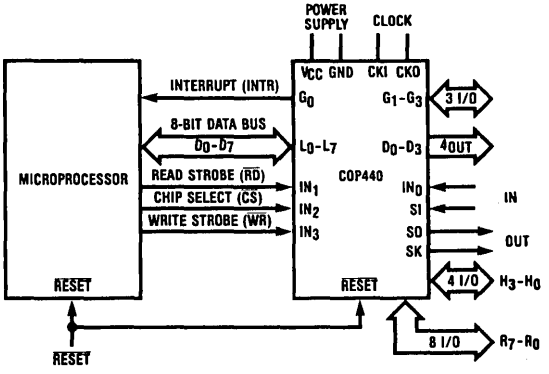
This option has been designed for compatibility with National's MICROBUS—a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS National Publication.) The functional and timing relationships between the COPS processor signal lines affected by this option are as specified for the MICROBUS interface, and are given in the AC electrical characteristics and shown in the timing diagrams *(Figure 2)*. Connection of the COP440 to the MICROBUS is shown in *Figure 6*.

Note: TRI-STATE outputs must be used on L port.

ZERO-CROSSING DETECTION
(not available on the COP442, COP342)

The following features are associated with the IN_1 pin: ININ and INIL instructions input the state of IN_1 to A_1; IN_1 interrupt generates an interrupt pulse when a low-going transition ("1" to "0") occurs on IN_1; zero-crossing interrupt generates an interrupt pulse when an IN_1 transition occurs (both "1" to "0" and "0" to "1").

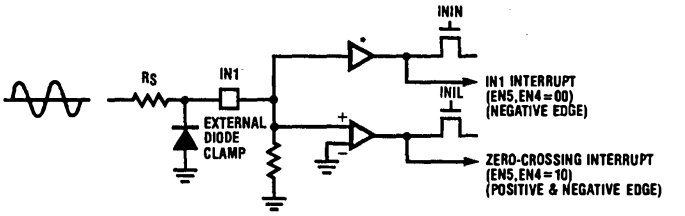
If the zero-crossing detector is mask-programmed in (see *Figure 7a*), the INIL instruction and zero-crossing interrupt will input the state of IN_1 through the true zero-crossing detector ("1" if input > 0V, "0" if input < 0V). The ININ instruction and IN_1 interrupt will then have unique logic HIGH and LOW levels depending on the IN port input level chosen. If normal (TTL) level is chosen, logic HIGH level is 3.0V (3.3V for COP340/341) and logic LOW level is 0.8V



TL/DD/6926-9

FIGURE 6. MICROBUS Option Interconnect

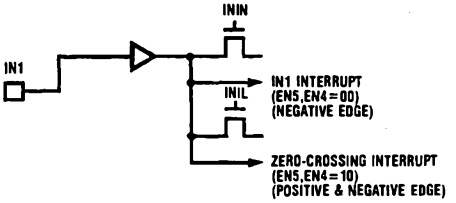
Functional Description (Continued)



TL/DD/6926-10

*Note: This input has a different set of logic HIGH and LOW levels; see above description.

a. Zero-Crossing Detect Logic Option



TL/DD/6926-11

b. IN, without Zero-Crossing Detect Logic

FIGURE 7. IN, Mask-Programmable Options

(0.6V for COP340/341); if high trip level is chosen, logic HIGH level is 5.4V and logic LOW level is 1.2V. If the zero-crossing detector is not mask-programmed in (see *Figure 7b*), IN_1 will have logic HIGH and LOW levels that are defined for the IN port (see option list).

The zero-crossing detector input contains a small hysteresis (50 mV typical) to eliminate signal noise, and is not a high impedance input but contains a resistive load to ground. Since this input can withstand a voltage range of −0.6V to +12V, an external clamping diode is needed for most input signals, as shown in *Figure 7a*, to limit the voltage below ground. An external resistor, R_S may be needed for the following two cases:

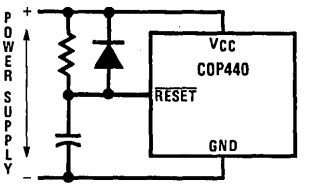
a. Input signal exceeds 12V; R_S and the internal resistor act as a voltage divider to reduce the voltage at the input pin to below 12V.

b. Signal comes from a low impedance source; when the voltage at the pin is clamped to −0.7V by the forward bias voltage of an external diode, R_S limits the current going through the diode.

INITIALIZATION

The $\overline{\text{RESET}}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{\text{RESET}}$ input, provided it stays low for at least three instruction cycle times. The user must provide an external RC network and diode to the $\overline{\text{RESET}}$ pin as in *Figure 8*. The external POR (Power-on-Reset) delay must be greater than the internal POR. The internal POR delay is 2600 internal clock cycles.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, G, H, IL, L, N, Q, R, and T registers are cleared. The SK output is enabled as a SYNC output by setting the SKL latch, thus providing a clock. RAM (data memory and stack) is not cleared. The first instruction at address 0 must be a CLRA.



TL/DD/6926-12

RC ≥ 5 × power supply rise time

FIGURE 8. Power-Up Clear Circuit

OSCILLATOR

There are three basic clock oscillator configurations available, as shown by *Figure 9*.

a. **Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The cycle frequency equals the crystal frequency divided by 16 (optional by 8). Thus a 4 MHz crystal with the divide-by-16 option selected will give a 250 kHz cycle frequency (4 μs instruction cycle time).

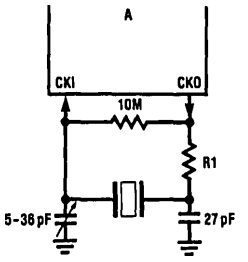
b. **External Oscillator.** CKI is an external clock input signal. The external frequency is divided by 16 (optional by 8 or 4) to give the cycle frequency. If the divide-by-4 option is selected, the CKI input level is the Schmitt-trigger level. CKO is now available to be used as the RAM power supply (V_R) or as a general purpose input.

c. **RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The cycle frequency equals the oscillation frequency divided by 4. CKO is available for non-timing functions.

CKO PIN OPTIONS

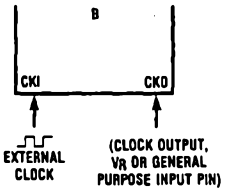
As an option, CKO can be an oscillator output. In a crystal controlled oscillator system, this signal is used as an output to the crystal network. As another option, CKO can be an interrupt input or a general purpose input, reading into bit 2 of A (accumulator) through the INIL instruction. As another option, CKO can be a RAM power supply pin (V_R), allowing

Functional Description (Continued)



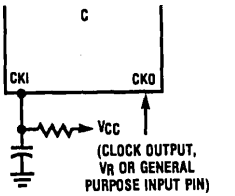
TL/DD/6926-13

a. Crystal Oscillator



TL/DD/6926-14

b. External Oscillator



TL/DD/6926-15

c. RC Controlled Oscillator

Crystal Oscillator

Crystal Value	R_1
4 MHz	1k
3.58 MHz	1k
2.10 MHz	2k

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Execution Time (μs)
13	100	5.0 ±20%
6.8	220	5.3 ±23%
8.2	300	8.0 ±22%
22	100	8.2 ±17%

Note: 5 kΩ ≤ R ≤ 50 kΩ
50 pF ≤ C ≤ 360 pF

FIGURE 9. COP440/441/442 Oscillators

its connection to a standby/backup power supply to maintain the data integrity of RAM registers 0-3 with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either of the two latter options is appropriate in applications where the system configuration does not require use of the CKO pin for timing functions.

RAM KEEP-ALIVE OPTION

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the lower 4 registers of the RAM. To insure that RAM data integrity is maintained, the following conditions must be met:

1. $\overline{\text{RESET}}$ must go low before V_{CC} goes below spec during power-off; V_{CC} must be within spec before $\overline{\text{RESET}}$ goes high on power-up.
2. When V_{CC} is on, V_R must be within the operating voltage range of the chip, and within 1V of V_{CC}.
3. V_R must be ≥ 3.3V with V_{CC} off.

I/O OPTIONS

COP440 inputs have the following optional configurations, illustrated in *Figure 10*.

a. An on-chip depletion load device to V_{CC}.

b. A Hi-Z input which must be driven to a "1" or "0" by external components.

c. A resistive load to GND for the zero-crossing input option (IN_1 only).

COP440 outputs have the following optional configurations:

d. Standard—an enhancement mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with TTL and CMOS input requirements. Available on SO, SK, D, G, and H outputs.

e. Open-Drain—an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, D, G, L, H, and R outputs.

f. Push-Pull—an enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

g. Standard L,R—same as **d.**, but may be disabled. Available on L and R outputs only (disabled on reset).

h. LED Direct Drive—an enhancement-mode device to ground and V_{CC} together with a depletion device to V_{CC} meeting the typical current sourcing requirements of the segments of an LED display. The sourcing devices are clamped to limit current flow. These devices may be turned off under program control (see Functional Description, EN Register), placing the output in a high-impedance state to provide required LED segment blanking for a multiplexed display. Available on L outputs only.

Note 1: When the driver is disabled, the depletion device may cause the output to settle down to an intermediate level between V_{CC} and GND. This voltage cannot be relied upon as a "1" level when reading the L inputs. The external signal must drive it to a "1" level.

Note 2: Much power is dissipated by this driver in driving an LED. Care must be taken to limit the power dissipation of the chip to within the absolute maximum ratings specified.

i. TRI-STATE Push-Pull—an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L and R outputs only (in TRI-STATE mode on reset).

j. Push-Pull R—same as **f.**, but may be disabled. Available on R outputs only.

k. Additional depletion pull-up—a depletion load to V_{CC} with the same current sourcing capability as the input load **a.**, in addition to the output drive chosen. Available on L and R outputs only. *This device cannot be disabled*; therefore, open-drain outputs with "1" output and TRI-STATE outputs do not show high-impedance characteristics. This device is useful in applications where a pull-up with low source current is desired, e.g., reading keyboards and switches.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6 respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figures 11* and *12* for each of these devices to allow the designer to effectively use these I/O configurations in designing a COP440 system.

Functional Description (Continued)

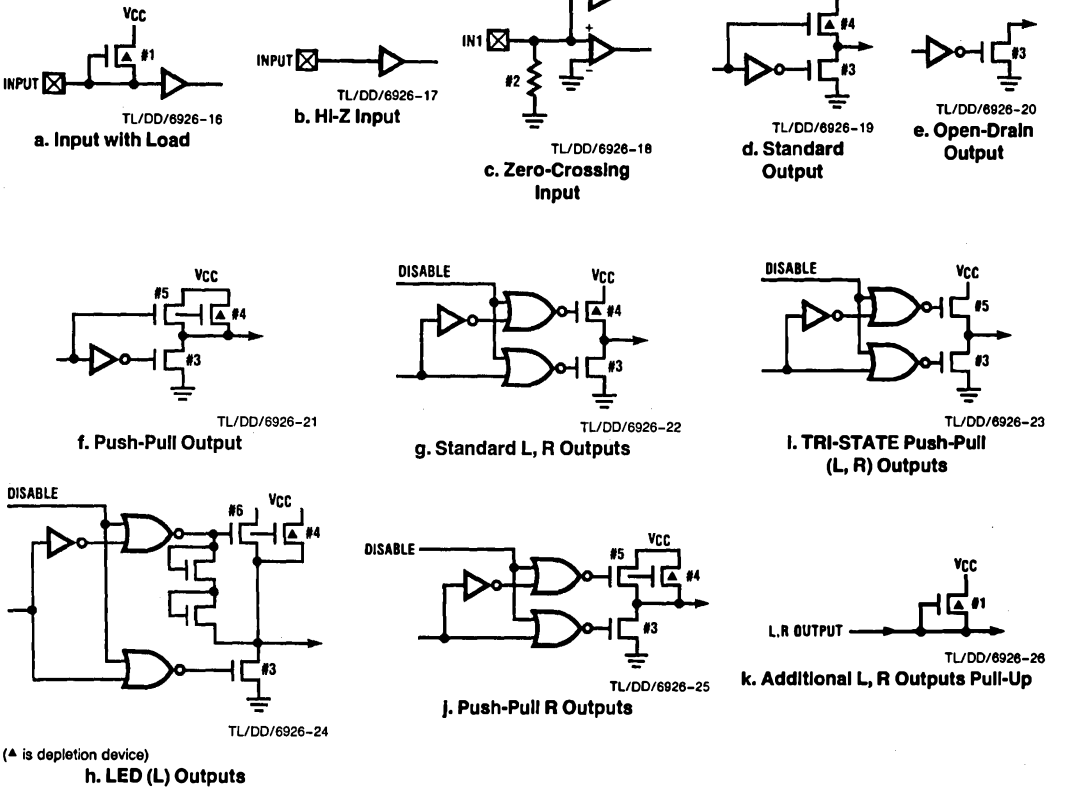


FIGURE 10. Input/Output Configurations

L-BUS CONSIDERATIONS

False states may be generated on L_0–L_7 during the execution of the CAMQ instruction. The L-Ports should not be used as clocks for edge sensitive devices such as flip-flops, counters, shift registers, etc. The following short program illustrates this situation.

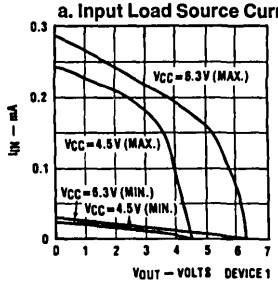
Glitch Test Program

```
START:
        CLRA            ;ENABLE THE Q
        LEI     4       ;REGISTER TO L LINES
        LBI     TEST
        STII    3
        AISC    12
LOOP:
        LBI     TEST    ;LOAD Q WITH X'C3
        CAMQ
        JP      LOOP
```

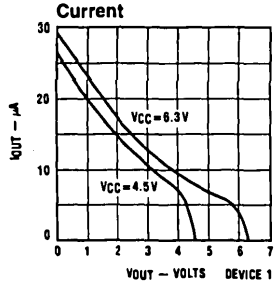
In this program the internal Q register is enabled onto the L lines and a steady bit pattern of logic highs is output on L_0, L_1, L_6, L_7, and logic lows on L_2–L_5 via the two-byte CAMQ instruction. Timing constraints on the device are such that the Q register may be temporarily loaded with the second byte of the CAMQ opcode (X'3C) prior to receiving the valid data pattern. If this occurs, the opcode will ripple onto the L lines and cause negative-going glitches on L_0, L_1, L_6, L_7, and positive glitches on L_2–L_5. Glitch durations are under 2 μs, although the exact value may vary due to data patterns, processing parameters, and L line loading. These false states are peculiar only to the CAMQ instruction and the L lines.

Typical Performance Characteristics

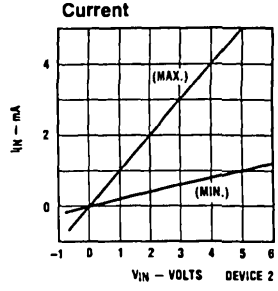
a. Input Load Source Current



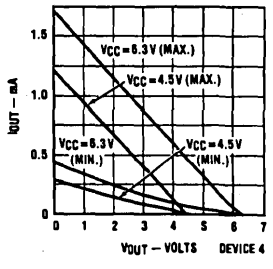
b. Input Load Minimum Source Current



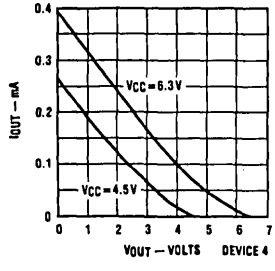
c. Zero-Crossing Detect Input Current



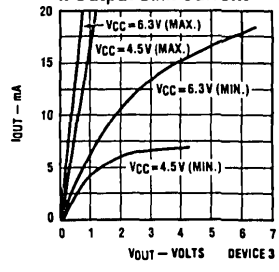
d. Standard Output Source Current



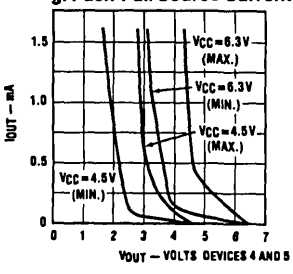
e. Standard Output Minimum Source Current



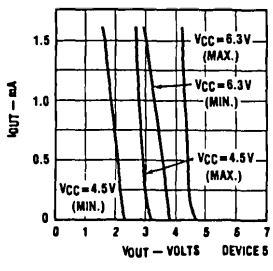
f. Output Sink Current



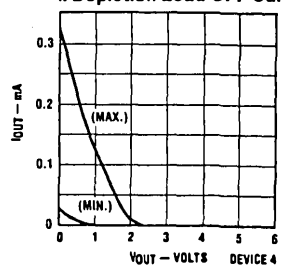
g. Push-Pull Source Current



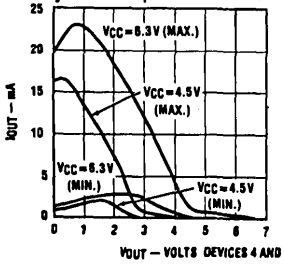
h. TRI-STATE Output Source Current



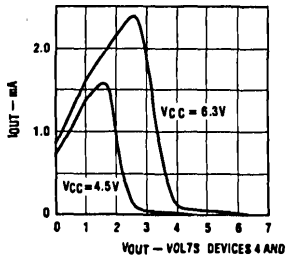
I. Depletion Load OFF Current



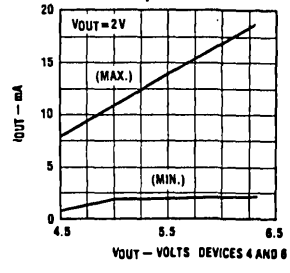
j. LED Output Source Current



k. LED Output Minimum Source Current



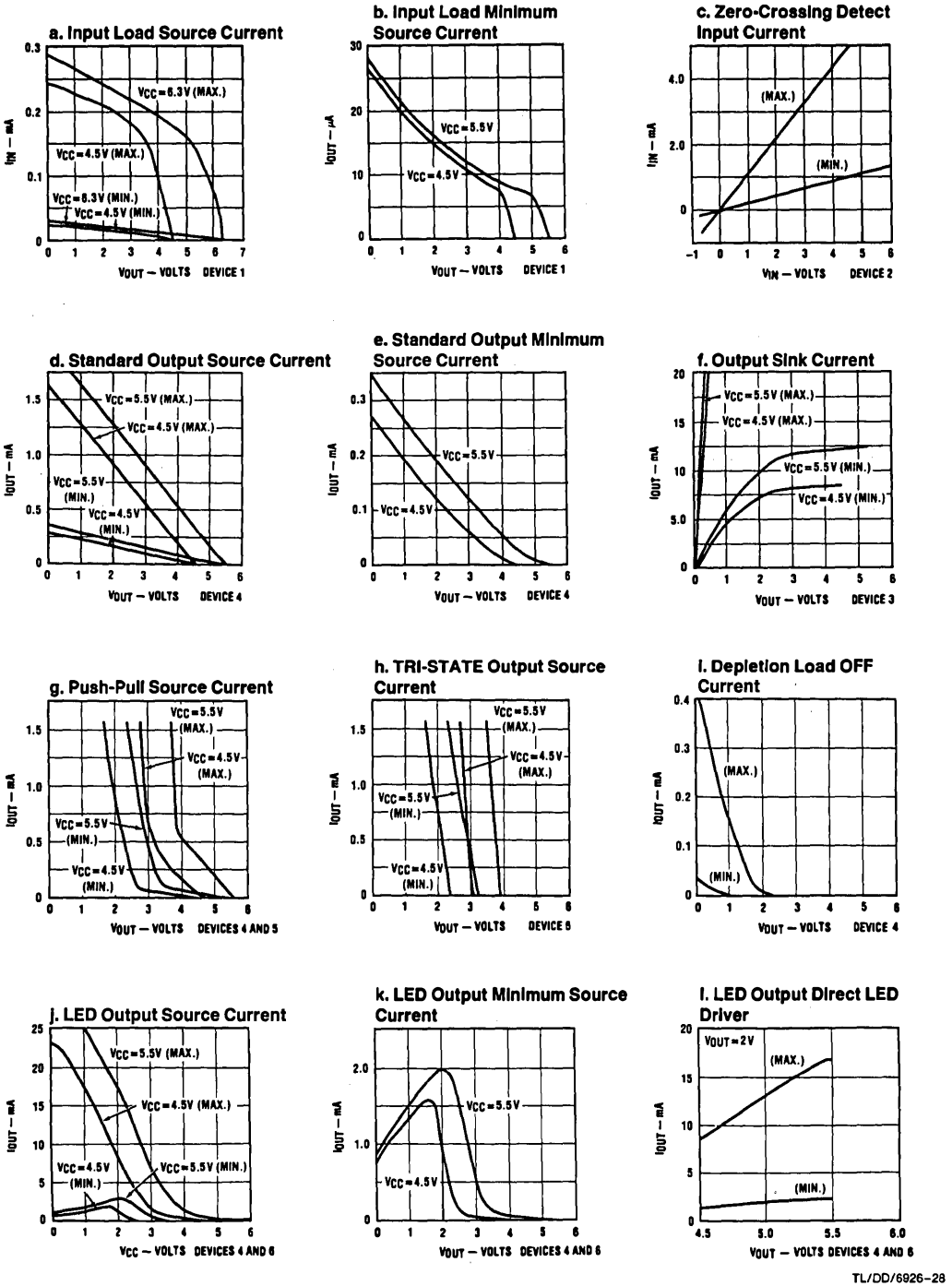
l. LED Output Direct LED Drive



TL/DD/6926-27

FIGURE 11. COP440/441/442 I/O Characteristics

Typical Performance Characteristics (Continued)



TL/DD/6926–28

FIGURE 12. CCOP340/341/342 I/O Characteristics

Power Dissipation

In order not to damage the device by exceeding the absolute maximum power dissipation rating, the amount of power dissipated inside the chip must be carefully controlled. As an example, an application uses a COP440 in room temperature (25°C) environment with a V_{CC} power supply of 6V; IN and SI inputs have internal loads; G and D ports drive loads that may sink up to 2 mA into the chip; H port with standard output option reads switches; L port with the LED option drives a multiplexed seven-segment display; R, SO and SK drive MOS inputs that do not source or sink any current.

a. At 25°C, maximum power dissipation allowed = 750 mW

b. Power dissipation by chip except

$$I/O = I_{CC} \times V_{CC} = 35\ mA \times 6V = 210\ mW$$

c. Maximum power dissipation by IN,

$$SI = 5 \times 0.3\ mA \times 6V = 9\ mW$$

d. G and D ports are sinking current from external loads; maximum output voltage with 2 mA sink current is less than 0.4V. Power dissipation by G and D ports =

$$2\ mA \times 0.4V \times 8 = 6.4\ mW$$

e. Maximum power dissipation by H port =

$$4 \times 1.5\ mA \times 6V = 36\ mW$$

f. When the seven segments of the LED are turned on, the output voltage is about 2V, so that the segment current is 17 mA. Power dissipation by L port =

$$7 \times 17\ mA \times (6V - 2V) = 476\ mW$$

This power dissipation caused by driving LEDs is usually the highest among the various sources.

g. R, SO, and SK do not dissipate any significant amount of power because they do not need to source or sink any current.

Total power dissipation (TPD) inside the device is the sum of items b through g above.

$$TPD = 210 + 9 + 6 + 36 + 476\ mW = 737\ mW$$

This is within the 750 mW limit at room temperature. If this application has to operate at 70°C, then the power dissipation must be reduced to meet the limit at that temperature. Some ways to achieve this would be to limit the LED current or to use an external LED driver.

At 70°C the absolute maximum power dissipation rating drops to 400 mW. The user must be careful not to exceed this value.

COP440 SERIES DEVICES

If the COP440 is bonded as a 28- or 24-pin device, it becomes the COP441 or COP442, respectively, as Illustrated in *Figure 3*. Note that the COP441 and COP442 do not include H and R ports. In addition, the COP442 does not include IN inputs; use of this option precludes the use of the IN options, the interrupt feature with IN as Input, the zero-crossing detect option, IN_2 external event counter input, and the MICROBUS option. All other options are available.

COP340, COP341, and COP342 are extended temperature versions of the COP440, COP441, and COP442, respectively.

COP440 Series Instruction Set

Table II is a symbol table providing internal architecture, instruction operand and operation symbols used in the instruction set table.

Table III provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the COP440 series instruction set.

TABLE II. COP440 Series Instruction Set Symbols

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	8-bit RAM Address Register
Br	Upper 4 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	8-bit Enable Register
G	4-bit Register to latch data for G I/O Port
H	4-bit Register to latch data for H I/O Port
IL	Two 1-bit Latches associated with the IN_3 or IN_0 Inputs
IN	4-bit Input Port
IN_1Z	Zero-Crossing Input
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
N	2-bit subroutine return address stack pointer
PC	11-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
R	8-bit Register to latch data for R TRI-STATE I/O Port
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output
T	8-bit Binary Counter Register

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0–15 binary (RAM Digit Select)
r	4-bit Operand Field, 0–9 binary (RAM Register Select)
a	11-bit Operand Field, 0–2047 binary (ROM Address)
y	4-bit Operand Field, 0–15 binary (Immediate Data)
RAM(s)	Content of RAM location addressed by s
RAM_N	Content of RAM location addressed by stack pointer N
ROM(t)	Content of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
−	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\bar{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values
V	OR

Instruction Set

TABLE III. COP440 Series Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC/LOGIC INSTRUCTIONS						
ASC		30	|0011|0000|	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	|0011|0001|	A + RAM(B) → A	None	Add RAM to A
ADT		4A	|0100|1010|	A + 10_{10} → A	None	Add Ten to A
AISC	y	5–	|0101| y |	A + y → A	Carry	Add immediate, Skip on Carry (y ≠ 0)
CASC		10	|0001|0000|	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	|0000|0000|	0 → A	None	Clear A
COMP		40	|0100|0000|	$\overline{A}$ → A	None	One's complement of A to A
NOP		44	|0100|0100|	None	None	No Operation
OR		33 1A	|0011|0011| |0001|1010|	A ∨ M → A	None	OR RAM with A
RC		32	|0011|0010|	"0" → C	None	Reset C
SC		22	|0010|0010|	"1" → C	None	Set C
XOR		02	|0000|0010|	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	|1111|1111|	ROM ($PC_{10:8}$, A,M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6– – –	|0110|0|$a_{10:8}$| |$a_{7:0}$|	a → PC	None	Jump
JP	a	– –	|1|$a_{6:0}$| (pages 2,3 only) or |11|$a_{5:0}$| (all other pages)	a → $PC_{6:0}$ a → $PC_{5:0}$	None	Jump within Page (Note 4)
JSRP	a	– –	|10|$a_{5:0}$|	PC + 1 → RAM_N N + 1 → N 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6– – –	|0110|1|$a_{10:8}$| |$a_{7:0}$|	PC + 1 → RAM_N N + 1 → N a → PC	None	Jump to Subroutine
RET		48	|0100|1000|	N – 1 → N RAM_N → PC	None	Return from Subroutine
RETSK		49	|0100|1001|	N – 1 → N RAM_N → PC	Always Skip on Return	Return from Subroutine then Skip

Instruction Set (Continued)

TABLE III. COP440 Series Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS						
CAME		33 1F	0011 | 0011 0001 | 1111	$A \rightarrow EN_{7:4}$ $RAM(B) \rightarrow EN_{3:0}$	None	Copy A, RAM to EN
CAMQ		33 3C	0011 | 0011 0011 | 1100	$A \rightarrow Q_{7:4}$ $RAM(B) \rightarrow Q_{3:0}$	None	Copy A, RAM to Q
CAMT		33 3F	0011 | 0011 0011 | 1111	$A \rightarrow T_{7:4}$ $RAM(B) \rightarrow T_{3:0}$	None	Copy A, RAM to T
CEMA		33 0F	0011 | 0011 0000 | 1111	$EN_{7:4} \rightarrow RAM(B)$ $EN_{3:0} \rightarrow A$	None	Copy EN to RAM, A
CQMA		33 2C	0011 | 0011 0010 | 1100	$Q_{7:4} \rightarrow RAM(B)$ $Q_{3:0} \rightarrow A$	None	Copy Q to RAM, A
CTMA		33 2F	0011 | 0011 0010 | 1111	$T_{7:4} \rightarrow RAM(B)$ $T_{3:0} \rightarrow A$	None	Copy T to RAM, A
LD	r	-5	00 | r | 0101 r = 0:3	$RAM(B) \rightarrow A$ $Br \oplus r \rightarrow Br$	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23 --	00 | 10 | 0011 0 | r | d r = 0:7	$RAM(r,d) \rightarrow A$	None	Load A with RAM pointed to directly by r,d
LID		33 19	0011 | 0011 0001 | 1001	$ROM\ (PC_{10:8}, A, M) \rightarrow M, A$	None	Load RAM, A Indirect
LQID		BF	1011 | 1111	$ROM(PC_{10:8},A,M) \rightarrow Q$	None	Load Q Indirect (Note 3)
RMB	0 1 2 3	4C 45 42 43	0100 | 1100 0100 | 0101 0100 | 0010 0100 | 0011	$0 \rightarrow RAM(B)_0$ $0 \rightarrow RAM(B)_1$ $0 \rightarrow RAM(B)_2$ $0 \rightarrow RAM(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0100 | 1101 0100 | 0111 0100 | 0110 0100 | 1011	$1 \rightarrow RAM(B)_0$ $1 \rightarrow RAM(B)_1$ $1 \rightarrow RAM(B)_2$ $1 \rightarrow RAM(B)_3$	None	Set RAM Bit
STII	y	7-	0111 | y	$y \rightarrow RAM(B)$ $Bd + 1 \rightarrow Bd$	None	Store Memory Immediate and Increment Bd
X	r	-6	00 | r | 0110 r = 0:3	$RAM(B) \leftrightarrow A$ $Br \oplus r \rightarrow Br$	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 --	0010 | 0011 1 | r | d r = 0:7	$RAM(r,d) \leftrightarrow A$	None	Exchange A with RAM pointed to directly by r,d
XDS	r	-7	00 | r | 0111 r = 0:3	$RAM(B) \leftrightarrow A$ $Bd - 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	-4	00 | r | 0100 r = 0:3	$RAM(B) \leftrightarrow A$ $Bd + 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

Instruction Set (Continued)

TABLE III. COP440 Series Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 | 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 | 1110	Bd → A	None	Copy Bd to A
LBI	r,d	--	00 | r | (d − 1) r = 0:3, d = 0,9:15	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 6)
			or			
		33	0011 | 0011			
		--	1 | r | d r = 0:7, any d			
LEI	y	33	0011 | 0011	y → $EN_{3:0}$	None	Load lower half of EN Immediate
		6-	0110 | y			
XABR		12	0001 | 0010	A ⟷ Br	None	Exchange A with Br
XAN		33	0011 | 0011	A ⟷ N(0,0 → A_3, A_2)	None	Exchange A with N
		0B	0000 | 1011			
TEST INSTRUCTIONS						
SKC		20	0010 | 0000		C = "1"	Skip if C is True
SKE		21	0010 | 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33	0011 | 0011		$G_{3:0}$ = 0	Skip if G is Zero (all 4 bits)
		21	0010 | 0001			
SKGBZ		33	0011 | 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 | 0001	2nd byte	G_0 = 0	
	1	11	0001 | 0001	2nd byte	G_1 = 0	
	2	03	0000 | 0011	2nd byte	G_2 = 0	
	3	13	0001 | 0011	2nd byte	G_3 = 0	
SKMBZ	0	01	0000 | 0001		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0001 | 0001		$RAM(B)_1$ = 0	
	2	03	0000 | 0011		$RAM(B)_2$ = 0	
	3	13	0001 | 0011		$RAM(B)_3$ = 0	
SKSZ		33	0011 | 0011		SIO = 0	Skip if SIO is Zero
		1C	0001 | 1100			
SKT		41	0100 | 0001		T counter carry has occurred since last test	Skip on Timer (Note 3)

Instruction Set (Continued)

TABLE III. COP440 Series Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
CAMR		33	0011 | 0011	$A \rightarrow R_{7:4}$	None	Output A, RAM to R Port
		3D	0011 | 1101	$RAM(B) \rightarrow R_{3:0}$		
ING		33	0011 | 0011	$G \rightarrow A$	None	Input G Port to A
		2A	0010 | 1010			
INH		33	0011 | 0011	$H \rightarrow A$	None	Input H Port to A
		2B	0010 | 1011			
ININ		33	0011 | 0011	$IN \rightarrow A$	None	Input IN Inputs to A (Note 2)
		28	0010 | 1000			
INIL		33	0011 | 0011	IL_3, CKO, IN_1Z, $IL_0 \rightarrow A$	None	Input IL Latches to A (Note 3)
		29	0010 | 1001			
INL		33	0011 | 0011	$L_{7:4} \rightarrow RAM(B)$	None	Input L Port to RAM, A
		2E	0010 | 1110	$L_{3:0} \rightarrow A$		
INR		33	0011 | 0011	$R_{7:4} \rightarrow RAM(B)$	None	Input R Port to RAM,A
		2D	0010 | 1101	$R_{3:0} \rightarrow A$		
OBD		33	0011 | 0011	$Bd \rightarrow D$	None	Output Bd to D Port
		3E	0011 | 1110			
OGI	y	33	0011 | 0011	$y \rightarrow G$	None	Output to G Port Immediate
		5–	0101 | y			
OMG		33	0011 | 0011	$RAM(B) \rightarrow G$	None	Output RAM to G Port
		3A	0011 | 1010			
OMH		33	0011 | 0011	$RAM(B) \rightarrow H$	None	Output RAM to H Port
		3B	0011 | 1011			
XAS		4F	0100 | 1111	$A \longleftrightarrow SIO, C \rightarrow SKL$	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ instruction is not available on the 24-pin COP442/COP342 since this device does not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (00010 is loaded into the upper 5 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Description of Selected Instructions

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing COP440 programs.

XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

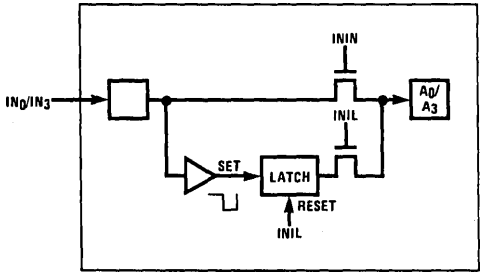
JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 11-bit word, $PC_{10:8}$, A, M. PC_{10}, PC_9 and PC_8 are not affected by this instruction.

Note that JID requires 2 instruction cycles if executed, 1 instruction cycle time if skipped.

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL_3 and IL_0, CKO and IN_1 into A (see *Figure 13*). The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL_3 and IL_0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN_3 and IN_0 lines. If CKO is mask-programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. Unlike the COP420/420C/420L/444L series, INIL will input IN_1 into A1.



TL/DD/6926-29

FIGURE 13. INIL Hardware Implementation

If zero-crossing detect is selected, the IN_1 input will go through the detection logic, thus allowing the user to interrogate the input, sending a "1" if the input is above 0V and a "0" if it is below 0V. INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction. It is also useful in checking the status of the zero-crossing detect input. The general purpose inputs IN_3–IN_0 are input to A upon execution of an ININ instruction, and the IN_1 input does not go through zero-crossing logic so that it has the same logic level as the other IN inputs for the ININ instruction (see *Figure 9*).

Note: IL latches are cleared on reset. This is different from the COP420/420C/420L/444L series.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC_{10}:PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. Note that LQID takes two instruction cycles if executed and one instruction cycle if skipped. Unlike most other COPS processors, this instruction does not push the stack.

LID INSTRUCTION

LID (Load Indirect) loads M and A with the contents of ROM pointed to by the 11-bit word PC_{10}:PC_8, A, M. Note that LID takes three instruction cycles if executed and two if skipped.

SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of the T counter (see internal logic, above) overflow latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

INSTRUCTION SET NOTES

a. The first word of a COP440 program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, they are still fetched from program memory. Thus program paths take the same number of cycle times whether instructions are skipped or executed, except for LID, LQID, and JID.

c. The ROM is organized into 32 pages of 64 words each. The Program Counter is an 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, LQID, or LID instruction is the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11, 15, 19, 23, 27, or 31 will access data in the next group of four pages.

Option List

The COP440 mask-programmable options are assigned numbers which correspond with the COP440 pins.

Option 1: L_1 I/O Port (see note below)
= 0: Standard output
= 1: Open-drain output
= 2: LED direct drive output
= 3: TRI-STATE output
= 4: same as 0 with extra load device to V_{CC}
= 5: same as 1 with extra load device to V_{CC}
= 6: same as 2 with extra load device to V_{CC}
= 7: same as 3 with extra load device to V_{CC}

Option 2: L_0 I/O Port
(same as Option 1)

Option 3: SI Input
= 0: Input with load device to V_{CC}
= 1: Hi-Z Input

Option 4: SO Output
= 0: Standard output
= 1: Open-drain output
= 2: Push-pull output

Option 5: SK Output
(same as Option 4)

Option 6: IN_0 Input
(same as Option 3)

Option 7: IN_3 Input
(same as Option 3)

Option 8: G_0 I/O Port
= 0: Standard output
= 1: Open-drain output

Option 9, G_1 I/O Port
(same as Option 8)

Option 10: G_2 I/O Port
(same as Option 8)

Option 11: G_3 I/O Port
(same as Option 8)

Option 12: H_0 I/O Port
(same as Option 8)

Option 13: H_1 I/O Port
(same as Option 8)

Option 14: H_2 I/O Port
(same as Option 8)

Option 15: H_3 I/O Port
(same as Option 8)

Option 16: D_3 Output
(same as Option 8)

Option 17: D_2 Output
(same as Option 8)

Option 18: D_1 Output
(same as Option 8)

Option 19: D_0 Output
(same as Option 8)

Option 20: GND—No options available

Option 21: CKO Pin
= 0: Oscillator output
= 1: RAM power supply (V_R) input
= 2: General purpose input with load device to V_{CC}
= 3: General purpose Hi-Z input

Option 22: CKI Input
= 0: Crystal input divided by 16
= 1: Crystal input divided by 8
= 2: Single-pin RC controlled oscillator (÷4)
= 3: Schmitt trigger clock input (÷4)

Option 23: $\overline{\text{RESET}}$ Input
(same as Option 3)

Option 24: R_7 I/O Port (see note below)
= 0: Standard output
= 1: Open-drain output
= 2: Push-pull output
= 3: TRI-STATE output
= 4: same as 0 with extra load device to V_{CC}
= 5: same as 1 with extra load device to V_{CC}
= 6: same as 2 with extra load device to V_{CC}
= 7: same as 3 with extra load device to V_{CC}

Option 25: R_6 I/O Port
(same as Option 24)

Option 26: R_5 I/O Port
(same as Option 24)

Option 27: R_4 I/O Port
(same as Option 24)

Option 28: R_3 I/O Port
(same as Option 24)

Option 29: R_2 I/O Port
(same as Option 24)

Option 30: R_1 I/O Port
(same as Option 24)

Option 31: R_0 I/O Port
(same as Option 24)

Option 32: L_7 I/O Port
(same as Option 1)

Option 33: L_6 I/O Port
(same as Option 1)

Option 34: L_5 I/O Port
(same as Option 1)

Option 35: L_4 I/O Port
(same as Option 1)

Option 36: IN_1 Input
= 0: Input with load device to V_{CC}
= 1: Hi-Z Input
= 2: Zero-crossing detect input (Option 41 = 0)

Option 37: IN_2 Input
(same as Option 3)

Option 38: L_3 I/O Port
(same as Option 1)

Option 39: L_2 I/O Port
(same as Option 1)

Option 40: V_{CC}—no options available

Option List (Continued)

Option 41: COP Function
= 0: Normal
= 1: MICROBUS option

Option 42: IN Input Levels
= 0: Standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
= 1: Higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 43: G Input Levels
(same as Option 42)

Option 44: L Input Levels
(same as Option 42)

Option 45: CKO Input Levels
(same as Option 42)

Option 46: SI Input Levels
(same as Option 42)

Option 47: R Input Levels
(same as Option 42)

Option 48: H Input Levels
(same as Option 42)

Option 49: No option available

Option 50: COP Bonding
= 0: COP440 (40-pin device)
= 1: COP441 (28-pin device)
= 2: COP442 (24-pin device)
= 3: COP440 and COP441
= 4: COP440 and COP442
= 5: COP440, COP441, and COP442
= 6: COP441 and COP442

COP440 Option Table

The following options information is to be sent to National along with the EPROM.

OPTION 1 VALUE = _____ IS: L_1 I/O PORT
OPTION 2 VALUE = _____ IS: L_0 I/O PORT
OPTION 3 VALUE = _____ IS: SI INPUT
OPTION 4 VALUE = _____ IS: SO OUTPUT
OPTION 5 VALUE = _____ IS: SK OUTPUT
OPTION 6 VALUE = _____ IS: IN_0 INPUT
OPTION 7 VALUE = _____ IS: IN_3 INPUT
OPTION 8 VALUE = _____ IS: G_0 I/O PORT
OPTION 9 VALUE = _____ IS: G_1 I/O PORT
OPTION 10 VALUE = _____ IS: G_2 I/O PORT
OPTION 11 VALUE = _____ IS: G_3 I/O PORT
OPTION 12 VALUE = _____ IS: H_0 I/O PORT
OPTION 13 VALUE = _____ IS: H_1 I/O PORT
OPTION 14 VALUE = _____ IS: H_2 I/O PORT
OPTION 15 VALUE = _____ IS: H_3 I/O PORT
OPTION 16 VALUE = _____ IS: D_3 OUTPUT
OPTION 17 VALUE = _____ IS: D_2 OUTPUT
OPTION 18 VALUE = _____ IS: D_1 OUTPUT
OPTION 19 VALUE = _____ IS: D_0 OUTPUT
OPTION 20 VALUE = 0 IS: GROUND PIN
OPTION 21 VALUE = _____ IS: CKO PIN
OPTION 22 VALUE = _____ IS: CKI INPUT
OPTION 23 VALUE = _____ IS: RESET INPUT
OPTION 24 VALUE = _____ IS: R_7 I/O PORT
OPTION 25 VALUE = _____ IS: R_6 I/O PORT
OPTION 26 VALUE = _____ IS: R_5 I/O PORT
OPTION 27 VALUE = _____ IS: R_4 I/O PORT
OPTION 28 VALUE = _____ IS: R_3 I/O PORT
OPTION 29 VALUE = _____ IS: R_2 I/O PORT
OPTION 30 VALUE = _____ IS: R_1 I/O PORT
OPTION 31 VALUE = _____ IS: R_0 I/O PORT
OPTION 32 VALUE = _____ IS: L_7 I/O PORT
OPTION 33 VALUE = _____ IS: L_6 I/O PORT
OPTION 34 VALUE = _____ IS: L_5 I/O PORT
OPTION 35 VALUE = _____ IS: L_4 I/O PORT
OPTION 36 VALUE = _____ IS: IN_1 INPUT
OPTION 37 VALUE = _____ IS: IN_2 INPUT
OPTION 38 VALUE = _____ IS: L_3 I/O PORT
OPTION 39 VALUE = _____ IS: L_2 I/O PORT
OPTION 40 VALUE = 0 IS: V_{CC}
OPTION 41 VALUE = _____ IS: COP FUNCTION
OPTION 42 VALUE = _____ IS: IN INPUT LEVELS
OPTION 43 VALUE = _____ IS: G INPUT LEVELS
OPTION 44 VALUE = _____ IS: L INPUT LEVELS
OPTION 45 VALUE = _____ IS: CKO INPUT LEVELS
OPTION 46 VALUE = _____ IS: SI INPUT LEVELS
OPTION 47 VALUE = _____ IS: R INPUT LEVELS
OPTION 48 VALUE = _____ IS: H INPUT LEVELS
OPTION 49 VALUE = _____ IS: NO OPTION
OPTION 50 VALUE = _____ IS: COP BONDING

Note on L and R I/O Port Options

If L and R I/O Ports are used as inputs, the following must be observed:

a. Open-Drain output (selection 1) is allowed only if external pull-up is provided.

b. If L and R output ports are disabled when reading, an external pull-up is required unless selections 4, 5, 6, or 7 are chosen.

c. If L output port is enabled, selections 3 and 7 are not allowed.

d. If R output port is enabled, selections 2, 3, 6, and 7 are not allowed.

Test Mode (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed COP440. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.