CS1089

Vacuum Fluorescent Display Tube Driver

The VFD Driver is a microprocessor interface IC that drives a multiplexed VF (Vacuum Fluorescent) display tube. It consists of a 32–bit shift register, a 32–bit transparent data latch, a metal mask ROM, six 20 mA anode output drivers, twenty–three 2 mA anode output drivers, and three 50 mA grid drivers with output enables.

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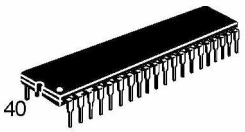
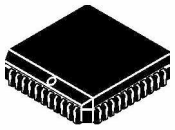
Features

- Power On Reset
- Display Dimming Possible
- Three, 50 mA Grid Drivers
- Anodes:
  - 6 @ 20 mA
  - 23 @ 2 mA



DIP–40
WIDE BODY
N SUFFIX
CASE 711



PLCC–44
FN SUFFIX
CASE 777

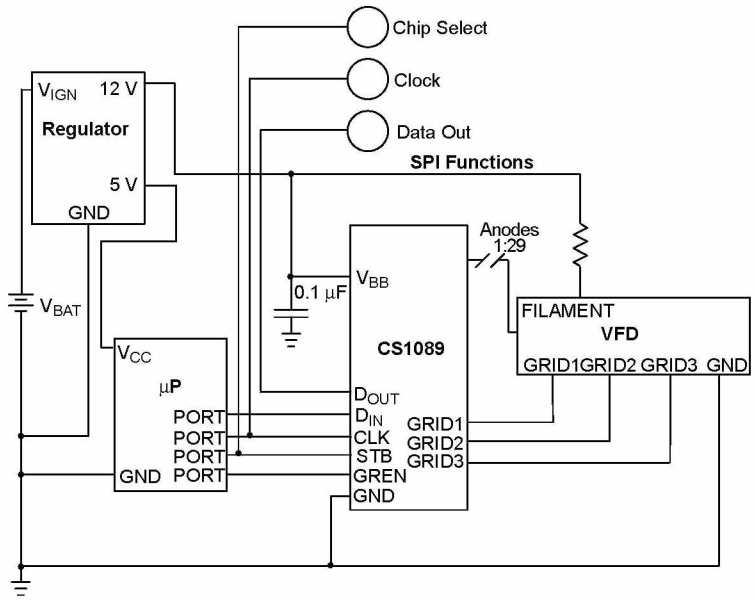


Figure 1. Application Diagram

ORDERING INFORMATION

Device	Package	Shipping
CS1089XN40	DIP–40 WIDE BODY	9 Units/Rail
CS1089XFN44	PLCC–44	23 Units/Rail
CS1089XFNR44	PLCC–44	500 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2877 of this data sheet.

MAXIMUM RATINGS*

Parameter		Value	Unit
Supply Voltage (V_{BB})		–0.6 to +18	V
Input Voltages (D_{IN}, CLK, STB, GREN)		–0.6 to +6.0	V
Junction Temperature Range		–40 to +150	°C
Storage Temperature Range		–55 to +150	°C
ESD Susceptibility (Human Body Model)		2.0	kV
ESD Susceptibility (Machine Model)		200	V
Package Thermal Resistance, DIP–40 Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$		 20 45	 °C/W °C/W
Package Thermal Resistance, PLCC–44 Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$		 16 55	 °C/W °C/W
Lead Temperature Soldering:	Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2	260 Peak 230 Peak	°C

1. 10 second maximum.
2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ($8.0\ V \le V_{BB} \le 16.5\ V$, Gnd = 0 V, $-40°C \le T_J \le 105°C$; unless otherwise stated. Note 3.)

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{BB} Input					
V_{BB} Input Voltage	–	8.0	–	16.5	V
I_{BB0} Current	No outputs active, V_{BB} = 16.5 V	–	2.0	5.0	mA
Reset Mode	All outputs forced low.	–	6.5	7.5	V
D_{IN}, CLK, STB Inputs					
V_{IL1}, Input Low Voltage	–	–	–	1.6	V
V_{IH}, Input High Voltage	–	3.3	–	–	V
I_{IL}, Input Current	$V_{IN} = V_{IH}$	–	7.5	20.0	μA
GREN Input					
V_{IL}, Input Low Voltage	–	–	–	1.6	V
V_{IH}, Input High Voltage	–	3.3	–	–	V
I_{IH}, Input Pull–down Current	V_{IN} = 3.325 V	–	30	60	μA
GRID1, GRID2, GRID3 Outputs					
I_{OL}	Sink Current	1.0	–	–	mA
I_{OH}	Source Current	50	–	–	mA
V_{OL}	I_{OUT} = 1.0 mA	–	–	0.5	V
V_{OH}	I_{OUT} = –50 mA, V_{BB} = 12 V	V_{BB} – 0.75	–	V_{BB}	V
AN24 – AN29 Outputs					
I_{OL}	Sink Current	400	–	–	μA
I_{OH}	Source Current	20	–	–	mA
V_{OL}	I_{OUT} = 400 μA	–	–	0.5	V
V_{OH}	I_{OUT} = –20 mA	V_{BB} – 0.5	–	V_{BB}	V

3. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be 100% parametrically tested in production.

ELECTRICAL CHARACTERISTICS (continued) (8.0 V ≤ V_{BB} ≤ 16.5 V, Gnd = 0 V, –40°C ≤ T_J ≤ 105°C; unless otherwise stated. Note 4.)

Parameter	Test Conditions	Min	Typ	Max	Unit
AN1 – AN23 Outputs					
I_{OL}	Sink Current	100	–	–	μA
I_{OH}	Source Current	2.0	–	–	mA
V_{OL}	I_{OUT} = 100 μA	–	–	0.5	V
V_{OG}	I_{OUT} = –2.0 mA	V_{BB} – 0.5	–	V_{BB}	V
D_{OUT} Output					
I_{OL}	Sink Current	1.0	–	–	mA
I_{OH}	Source Current	1.0	–	–	mA
V_{OL}	I_{OUT} = 1.0 mA	–	–	0.5	V
V_{OH}	I_{OUT} = –1.0 mA	3.9	–	5.1	V
AC Characteristics: Input and Output Timing					
F_C, CLK Frequency	–	0	–	1.0	MHz
T_{CL}, CLK Low Time	–	200	–	–	ns
T_{CH}, CLK High Time	–	200	–	–	ns
T_{CR}, CLK Rise Time	–	–	–	100	ns
T_{CF}, CLK Fall Time	–	–	–	100	ns
T_{CD}, CLK Low to D_{OUT} Propagation Delay	–	–	–	200	ns
T_{SC}, STB Low to CLK High Time	–	50	–	–	ns
T_{ST}, STB High Time	–	500	–	–	ns
T_{AN}, STB High to Anode Output Propagation Delay	–	–	–	5.0	μs
T_{GL}, Grid Turn On Propagation Delay	V_{BB} = 12 V	–	–	2.0	μs
T_{G0}, Grid Turn Off Propagation Delay	V_{BB} = 12 V	–	–	5.0	μs
T_{GR}, Grid Rise Time	At rated load. Note 5.	0.50	–	2.00	μs
T_{GF}, Grid Fall Time	At rated load. Note 5.	0.35	–	2.00	μs
T_{AR}, Anode Rise Time	At rated load. Note 5.	0.40	–	2.00	μs
T_{AF}, Anode Fall Time	At rated load. Note 5.	0.40	–	2.50	μs

4. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be 100% parametrically tested in production.
5. Grid and anode rise / fall times are measured from 10% and 90% points. Output currents are at the maximum rated currents for the respective stages.

PACKAGE LEAD DESCRIPTION

Package Lead Number		Lead Symbol	Function
40L DIP	44L PLCC	(29 Anode Configuration)	
1	14	GRID1	50 mA grid output.
2	15	GRID2	50 mA grid output.
3	16	GRID3	50 mA grid output.
4	17	AN1	2.0 mA anode output.
5	18	AN2	2.0 mA anode output.
6	19	AN3	2.0 mA anode output.
7	20	AN4	2.0 mA anode output.
8	21	AN5	2.0 mA anode output.
9	22	AN6	2.0 mA anode output.
10	24	AN7	2.0 mA anode output.
11	25	AN8	2.0 mA anode output.
12	26	AN9	2.0 mA anode output.
13	27	AN10	2.0 mA anode output.
14	28	AN11	2.0 mA anode output.
15	29	AN12	2.0 mA anode output.
16	30	AN13	2.0 mA anode output.
17	31	AN14	2.0 mA anode output.
18	32	AN15	2.0 mA anode output.
19	33	AN16	2.0 mA anode output.
20	35	GND	Ground connection.
21	36	AN17	2.0 mA anode output.
22	37	AN18	2.0 mA anode output.
23	38	AN19	2.0 mA anode output.
24	39	AN20	2.0 mA anode output.
25	40	AN21	2.0 mA anode output.
26	41	AN22	2.0 mA anode output.
27	42	AN23	2.0 mA anode output.
28	43	AN24	20 mA anode output.
29	44	AN25	20 mA anode output.
30	2	AN26	20 mA anode output.
31	3	AN27	20 mA anode output.
32	4	AN28	20 mA anode output.
33	5	AN29	20 mA anode output.
34	6	D_{OUT}	Shift register data output.
35	7	D_{IN}	Shift register data input.
36	8	CLK	Shift register clock input.
37	9	STB	Transfer contents of shift registers to output stages.
38	10	GREN	Grid outputs enable.
39	1, 11, 12, 23, 34	NC	No connection.
40	13	V_{BB}	Supply voltage input.

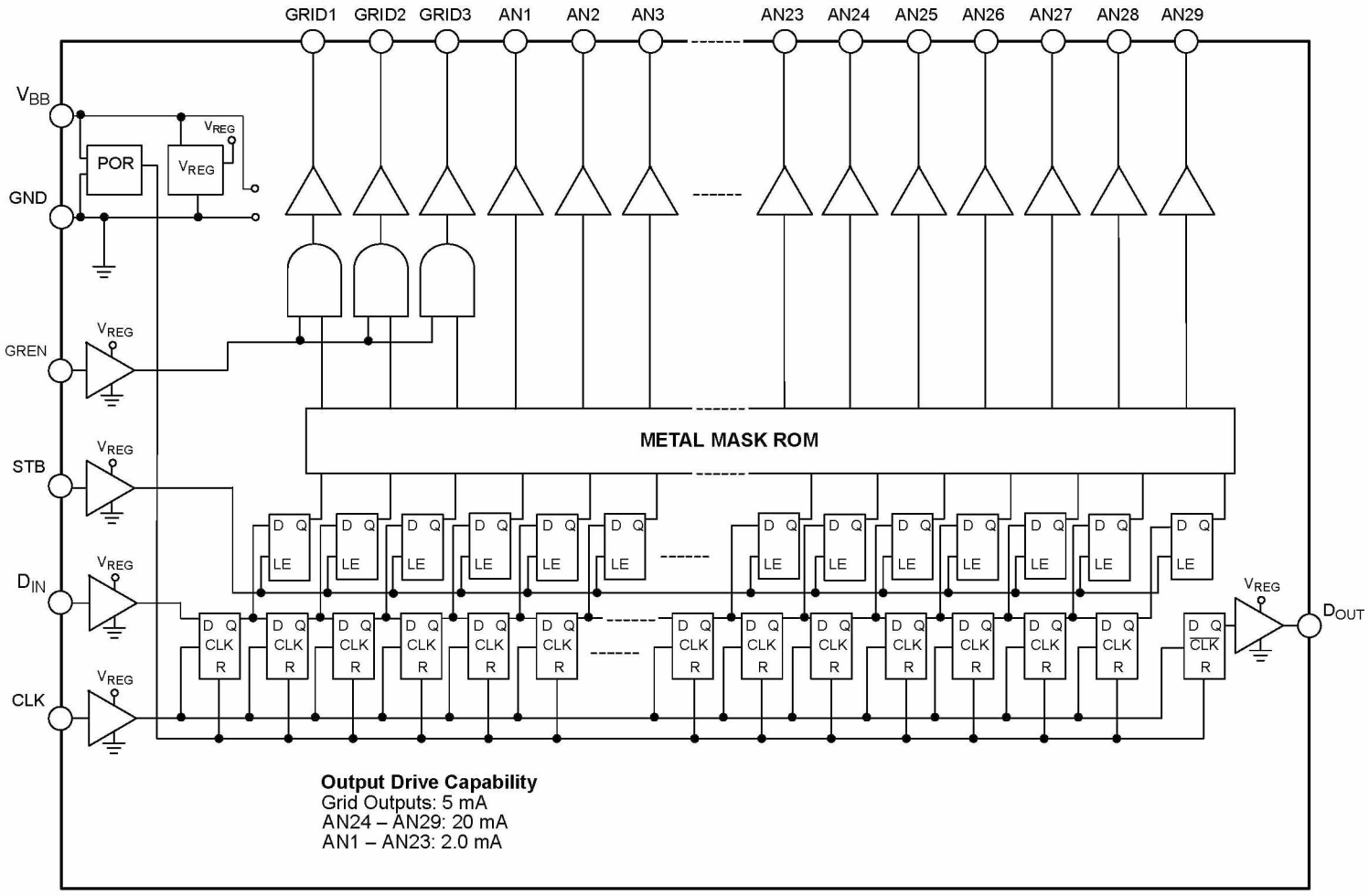


Figure 2. Block Diagram

OPERATION DESCRIPTION

Upon the initial application of power, the power on reset function will cause all of the anode and grid driver outputs to be off and all shift register outputs to be set low. Data is fed into the shift register through the D_{IN} pin at the rising edge of the CLK input. Thirty two bits of data are capable of being stored by the shift register. Once the desired pattern is stored in the shift register, it can be transferred to the latch by setting the STB input high. The output of each latch drives its corresponding output stage. A logic high input to the shift register/latch will cause the corresponding output to turn on. A logic low input to the shift register/latch will cause the corresponding output to turn off. Please note that if the STB is held high, the outputs of the latch reflect the outputs of the corresponding shift register bits and will change if data is shifted in.

The three GRID outputs are gated by the GREN input. When GREN is low, the GRID outputs are forced low regardless of the state of the corresponding latch output. When GREN is high, the GRID outputs correspond to the state of their respective latch outputs. The anode outputs, AN1 to AN29 are always enabled.

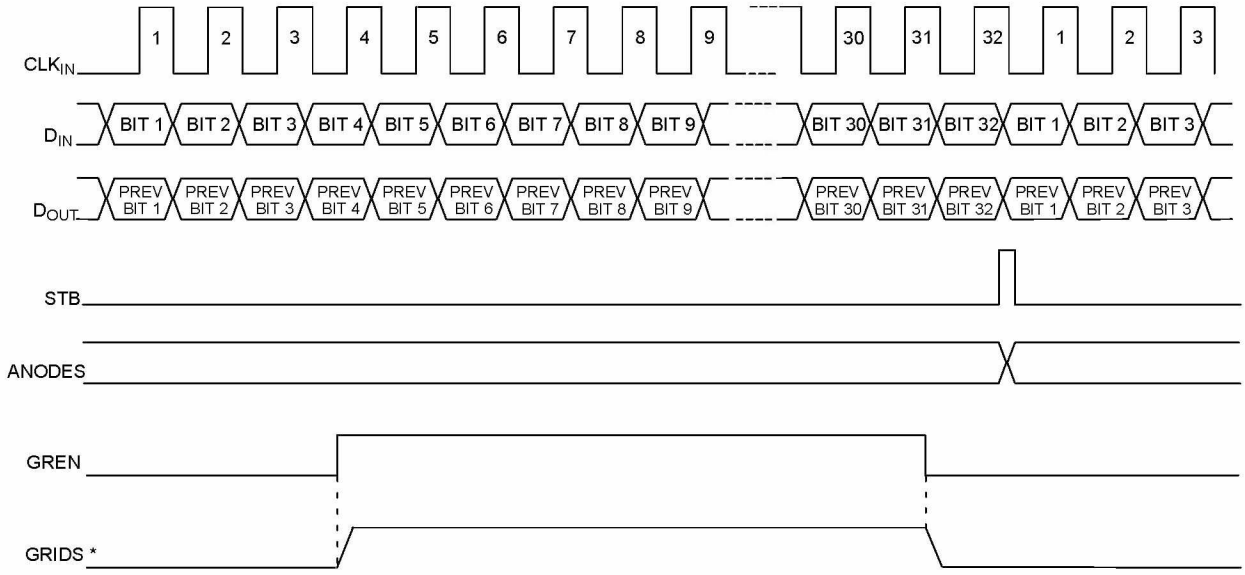
The D_{OUT} pin is the output of the last stage of the shift register to allow serial cascading of this IC with other devices. Data from the last stage of the shift register is supplied to the D_{OUT} pin delayed by 1/2 CLK cycle. Data on the D_{OUT} output changes with the falling edges of the CLK to prevent logic race conditions between the CLK and the D_{IN} of the next IC in the serial chain.

APPLICATION INFORMATION

Table 1. Bit Pattern, G = Grid, A = Anode.

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A1	A2	A3	A4	A5	A6	A7	A8	A16	A15	A14	A13	A12	A11	A10	A9

Bit #	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A23	A22	A21	A20	A19	A18	A17	G3	A24	A25	A26	A27	A28	A29	G1	G2



* Selected grid goes high only if input bit pattern from shift register to grid is high.

Figure 3. Typical Operation

Unused grid and anode drivers should have their respective bits set to logic low in the data stream.

Multiple grid or anode drivers may be connected together, but must be programmed to the same logic state for proper device operation. Maximum package power must be observed and care must be taken to maintian junction temperature below +150°C.

Care must be taken when interfacing this part to a microprocessor. The D_{OUT} output V_{OH} is specified at 3.9 V to 5.1 V at an I_{OUT} of –1.0 mA. Lower current loads will result in a higher output voltage. V_{OH} = 5.2 V (typ) with no load. V_{OH} = 5.7 V (max) with no load. Protection or workarounds for the device may be needed at the application level. No protection is needed when interfacing with other parts in this family (CS1087, CS1088, or CS1089).

MARKING DIAGRAMS

DIP–40
WIDE BODY
N SUFFIX
CASE 711

PLCC–44
FN SUFFIX
CASE 777

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS