# SONY

# CXA1744AR

## IF Amplifier for Digital Cordless Telephone

### Description

The CXA1744AR is an IF amplifier IC designed for digital cordless telephone of Europe, CT-2.

### Features

- Mixer, RSSI, detector, and various other functions required of a digital cordless phone IF amplifier.
- Local oscillator and multiplier for the mixer.
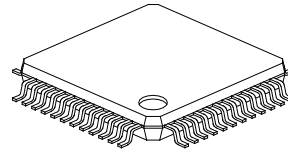- Low power consumption (8.4mA at 3.0V)
- Small package (48-pin LQFP).

### Absolute Maximum Ratings (Ta=25°C)

- Supply voltage                $V_{CC}$        14        V
- Operating temperature    Topr    –20 to +75    °C
- Storage temperature       Tstg    –65 to +150   °C
- Allowable power dissipation  $P_D$        500        mW

### Recommended Operating Condition

- Supply voltage                $V_{CC}$    2.7 to 5.5     V
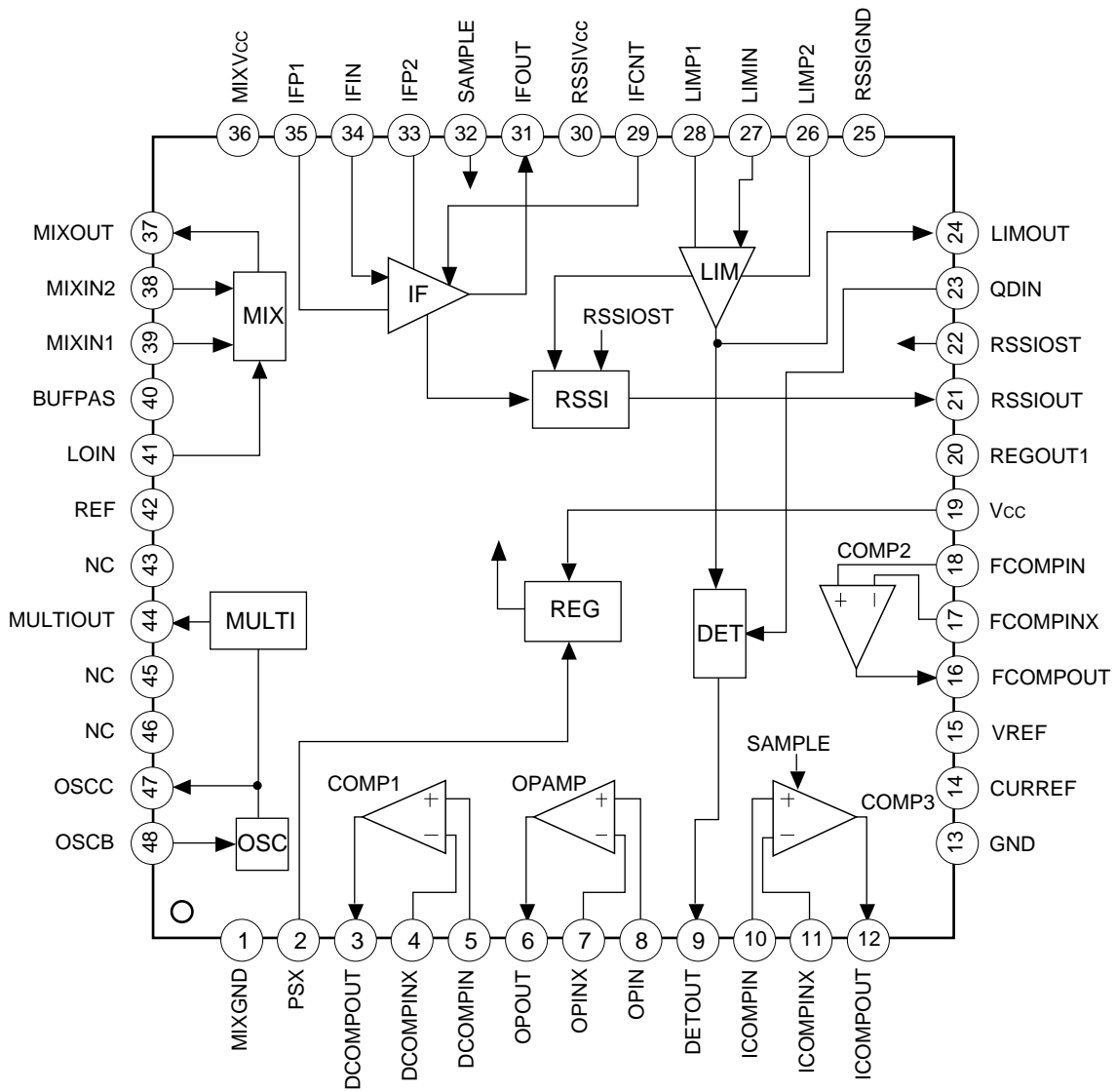
48  pin  LQFP  (Plastic)

### Structure

Bipolar silicon monolithic IC

### Applications

Digital cordless telephone of Europe (CT-2)

E93Z33-TE

**Block Diagram and Pin Configuration**

**Pin Description**

| Pin No. | Symbol | Typical pin voltage | Equivalent circuit | Description |
|---|---|---|---|---|
| 1 | MIXGND | 0V | | GND for the MIX, OSC, and MULTI circuits. |
| 2 | PSX | 0V |  | Power save control.<br>Power save mode for Low; power save function executes on all circuits except the OSC circuit and a part of the REG circuit. |
| 3 | DCOMPOUT | — |  | Data slicer comparator output. |
| 4 | DCOMPINX | — |  | Data slicer comparator input.<br>DCOMPINX is for out-of-phase input. |
| 5 | DCOMPIN | | | DCOMPIN is for in-phase input. |
| 6 | OPOUT | — |  | Operational amplifier output. |
| 7 | OPINX | — |  | Operational amplifier input.<br>OPINX is for out-of-phase input. |
| 8 | OPIN | | | OPIN is for in-phase input. |
| 9 | DETOUT | 1.25V |  | Detector output. |

| Pin No. | Symbol | Typical pin voltage | Equivalent circuit | Description |
|---|---|---|---|---|
| 10 | ICOMPIN | — |  | Sample-and-hold circuit input. ICOMPIN is for in-phase input. ICOMPINX is for out-of-phase input. |
| 11 | ICOMPINX | | | |
| 12 | ICOMPOUT | — |  | Sample-and-hold circuit output. |
| 13 | GND | 0V | | GND for circuits other than the MIX, OSC, MULTI, and RSSI circuits. |
| 14 | CURREF | 1.25V |  | Adjustment for RSSI output current. Connects a resistor between this pin and GND. |
| 15 | VREF | 1.9V |  | Reference voltage. Leave this pin open normally. |
| 16 | FCOMPOUT | — |  | Comparator output for free-channel detection. |
| 17 | FCOMPINX | — |  | Comparator input for free-channel detection. FCOMPINX is for out-of-phase input. FCOMPIN is for in-phase input. |
| 18 | FCOMPIN | | | |

| Pin No. | Symbol | Typical pin voltage | Equivalent circuit | Description |
|---------|--------|---------------------|--------------------|-------------|
| 19 | Vcc | 3.0V | | Power supply for circuits other than the MIX, OSC, MULTI, and RSSI circuits. |
| 20 | REGOUT1 | 1.25V |  | Internal bias regulator output. A stabilized bias voltage can be obtained. |
| 21 | RSSIOUT | — |  | RSSI current output. A voltage output is obtained when a resistor is connected between this pin and GND. |
| 22 | RSSIOST | 1.25V |  | RSSI offset adjustment. The offset amount of RSSI output current can be adjusted by connecting a resistor between this pin and GND. |
| 23 | QDIN | 2.45V |  | Detector input. Connect a detection discriminator. |
| 24 | LIMOUT | 1.55V |  | Limiter output. |
| 25 | RSSIGND | 0V | | GND for the IF amplifier, limiter and RSSI circuits. |

| Pin No. | Symbol | Typical pin voltage | Equivalent circuit | Description |
|---------|--------|---------------------|--------------------|-------------|
| 26 | LIMP2 | 1.5V |  | Limiter input. Input the signal from IF amplifier to LIMIN. Connect a decoupling capacitor to LIMP1 and LIMP2. |
| 27 | LIMIN | | | |
| 28 | LIMP1 | | | |
| 29 | IFCNT | 0.6V |  | IF amplifier gain adjustment. Connect a resistor between this pin and GND to compensate for the interstage filter insertion loss between the IF amplifier and limiter. |
| 30 | RSSIVcc | 2.45V |  | Power supply for the IF amplifier, limiter and RSSI circuits. Connected to the regulator output internally. Connect a decoupling capacitor. |
| 31 | IFOUT | 1.55V |  | IF amplifier output. |
| 32 | SAMPLE | 3.0V |  | Sample-and-hold circuit control input. Sample mode for open or High; hold mode for Low. |
| 33 | IFP2 | 1.55V |  | IF amplifier input. Input the signal from MIX to IFIN. Connect a decoupling capacitor to IFP1 and IFP2. |
| 34 | IFIN | | | |
| 35 | IFP1 | | | |
| 36 | MIXVcc | 3.0V | | Power supply for the MIX, OSC, and MULTI circuits. |

| Pin No. | Symbol | Typical pin voltage | Equivalent circuit | Description |
|---|---|---|---|---|
| 37 | MIXOUT | 1.4V |  | Mixer output. |
| 38 | MIXIN2 | 1.2V |  | Mixer RF signal differential input and bias. Connect a decoupling capacitor to REF. |
| 39 | MIXIN1 | | | |
| 42 | REF | | | |
| 40 | BUFPAS | 1.75V |  | Mixer local signal input. Connect a decoupling capacitor to BUFPAS. Input the local signal to LOIN. |
| 41 | LOIN | | | |
| 44 | MULTIOUT | — |  | Multiplier current output. Connect a tank circuit between this pin and power supply. |
| 47 | OSCC | — |  | The Colpitts-type oscillation circuit is composed by connecting a crystal oscillator. Input to the OSCC pin when using an external oscillator. |
| 48 | OSCB | 2.75V | | |

## Electrical Characteristics   (VCC=3.0V, Ta=25°C, refer to the Electrical Characteristics Measurement Circuit)

| Item | Symbol | SW set to ON | Measurement conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Current consumption 1 | ICC | | For operating $V_{IN}7$=10MHz, 0dBm | I7 | 6.4 | 8.4 | 11.2 | mA |
| Current consumption 2 | ICC | S1 | For power saving $V_{IN}7$=10MHz, 0dBm | I7 | — | 0.2 | 0.5 | mA |
| Mixer conversion gain | GVMIX | | $V_{IN}5$=150.05MHz, -40dBm $V_{IN}6$=139.35MHz, -10dBm RL=330Ω | V3 | 15.5 | 18 | 20.5 | dB |
| Mixer output resistance | ROMIX | | | | 240 | 330 | 420 | Ω |
| IF AMP voltage gain | GIF | S10 | $V_{IN}4$=10.7MHz, -60dBm RL=470Ω | V2 | 31 | 33.5 | 36 | dB |
| IF AMP input resistance | RIIF | | | | 240 | 330 | 420 | Ω |
| IF AMP output resistance | ROIF | | | | 320 | 440 | 560 | Ω |
| Limiter voltage gain | GLIM | | $V_{IN}3$=10.7MHz, -80dBm | 24pin | 64 | 66.5 | 69 | dB |
| Limiter input resistance | RILIM | | | | 340 | 460 | 580 | Ω |
| Limiter output voltage amplitude | VLIM | | $V_{IN}3$=10.7MHz, -20dBm | 24pin | 320 | 400 | 480 | mVP-P |
| RSSI output current inclination (IF) | | | $V_{IN}4$=10.7MHz, -30~0dBm | I8 | 0.32 | 0.4 | 0.54 | µA/dB |
| RSSI output current inclination (LIM) | | | $V_{IN}3$=10.7MHz, -45~-15dBm | I8 | 0.32 | 0.4 | 0.54 | µA/dB |
| RSSI dynamic range | DRSSI | | For MIXIN input | | 75 | 80 | — | dB |
| RSSI relative precision | | | | | — | — | ±3 | dB |
| RSSI output voltage range | | | | | 0.2 | — | 1.3 | V |
| Detector output voltage | VDET | | $V_{IN}3$=10.7MHz, -20dBm | V1 | 160 | 200 | 240 | mVrms |
| Detector total harmonic distortion | THD | | $F_{MOD}$=36kHz, $f_{DEV}$=±25kHz | V1 | — | — | 3.0 | % |
| Detector maximum output voltage | | | | | 1.2 | — | — | VP-P |
| Detector output voltage High level | | | | | Vcc -1.1 | — | — | V |
| Detector output voltage Low level | | | | | — | — | 0.5 | V |
| REG1 output voltage | VREG1 | S9 | IL=300µA | 20pin | 1.07 | 1.17 | 1.27 | V |
| COMP1 output saturation voltage | ISAT1 | S2 | $V_{IN}1$=1.1V, Isink=5mA | 3pin | — | 0.35 | 0.5 | V |
| COMP1 output leak current | ILEAK1 | | | I1 | — | — | 1.0 | µA |
| COMP1 input bias current | IB1 | S3 S4 | Measured value/2 | I2 | -200 | -70 | — | nA |
| COMP1 rise time | tr1 | | $V_{IN}1$=DC level 1.3V | | — | 70 | 200 | nsec |
| COMP1 fall time | tf1 | | Rectangular wave of 100kHz, 0.5VP-P | 3pin | — | 40 | 200 | nsec |
| COMP1 rise propagation delay time | tpdr1 | | RL=1KΩ, CL=20PF | | — | 130 | 500 | nsec |
| COMP1 fall propagation delay time | tpdf1 | | | | — | 160 | 500 | nsec |
| COMP1 input dynamic range | | | For Vref=1.3V | | 0.3 | — | Vcc | V |

| Item | Symbol | SW set to ON | Measurement conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| COMP2 output saturation voltage | $I_{SAT2}$ | S6 | $V_{IN2}$=1.1V, Isink=1mA | 16pin | — | 0.2 | 0.4 | V |
| COMP2 output leak current | $I_{LEAK2}$ | | | I5 | — | — | 1.0 | µA |
| COMP2 input bias current | IB2 | S7 S8 | Measured value/2 | I6 | -200 | -70 | — | nA |
| COMP2 rise time | tr2 | | $V_{IN2}$=DC level 1.3V | 16pin | — | 300 | 500 | nsec |
| COMP2 fall time | tf2 | | Rectangular wave of 100kHz, 0.5$V_{P-P}$ | | — | 30 | 500 | nsec |
| COMP2 rise propagation delay time | tpdr2 | | RL=4.7kΩ, CL=20pF | | — | 200 | 500 | nsec |
| COMP2 fall propagation delay time | tpdf2 | | | | — | 170 | 500 | nsec |
| COMP2 input dynamic range | | | For Vref=1.3V | | 0 | — | Vcc | V |
| OPAMP input bias range | IB | | Measured value/2 | I3 | -200 | -70 | — | nA |
| OPAMP in-phase input voltage range | $V_{ICM}$ | | | | 0.4 | — | Vcc -1.1 | V |
| OPAMP output voltage range | | | | | 0.4 | — | Vcc -1.1 | V |
| Sample-and-hold circuit High leak current | $I_{LEAKH}$ | S5 S11 | For hold | I4 | — | — | 100 | nA |
| Sample-and-hold circuit Low leak current | $I_{LEAKL}$ | S11 | | | -100 | — | — | nA |
| Sample-and-hold circuit control voltage High | | | | | 0.8 X Vcc | — | — | V |
| Sample-and-hold circuit control voltage Low | | | | | — | — | 0.13 X Vcc | V |
| Sample-and-hold circuit OFF current time for High output | | | Sample→Hold (For S11 OFF→ON) | 12pin | — | 1.2 | 3.0 | µsec |
| Sample-and-hold circuit OFF current time for Low output | | S5 | Sample→Hold (For S11 OFF→ON), VS=1.1V | 12pin | — | 1.2 | 3.0 | µsec |

**Design Reference Values**                                              (V<sub>CC</sub>=3.0V, Ta=25°C)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|------|--------|-----------|------|------|------|------|
| Multiplier output amplitude | V<sub>MLT</sub> | fin=27.87MHz, -10dBm | — | 200 | — | mV<sub>P-P</sub> |
| 3rd order intercepting point | IP3 | | — | -8 | — | dBM |
| RF input impedance S11 real component | | fin=150.05MHz | — | 145 | — | Ω |
| RF input impedance S11 imaginary component | | fin=150.05MHz | — | -380 | — | Ω |
| Mixer noise figure | | SBB conversion | — | 11 | — | dB |
| IF amplifier voltage gain difference (for adjustment) | | RL=470Ω, difference to Pin 29 open | — | 3 | — | dB |
| RSSI rise time | | For input signal OFF/ON | — | 30 | — | μsec |
| RSSI fall time | | For input signal ON/OFF | — | 50 | — | μsec |
| RSSI rise time | | For burst operation | — | 40 | — | μsec |
| RSSI fall time | | For burst operation | — | 40 | — | μsec |
| Input sensitivity (12 dB SINAD value) | | For MIXIN input (50Ω LC matching) (50Ω LC matching) | — | 4.5 | — | μV |

## Electrical Characteristics Measurement Circuit



*1   303AC-1941NK (Toko)

**Application Circuit**



*1 MF XTal 27.87MHz (Asahi)
*2 LQN1 84nH (Murata)
*3 SFE10.7MHYK (Murata)
*4 SFECA10.7MA5 (Murata)
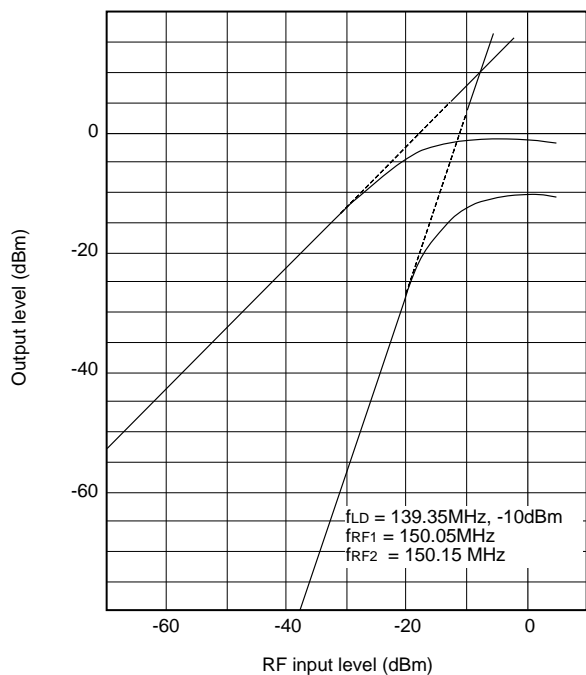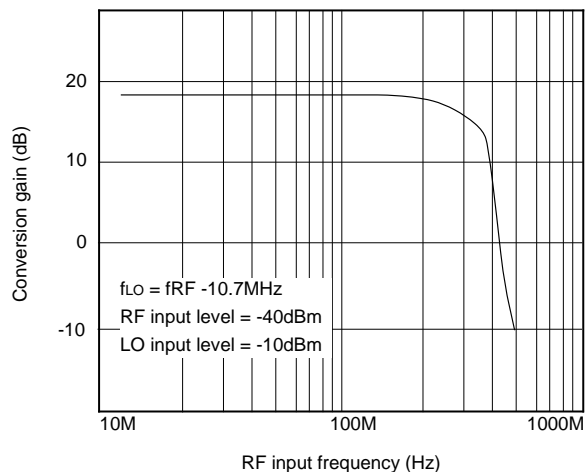*5 303AC - 1941NK (Toko)
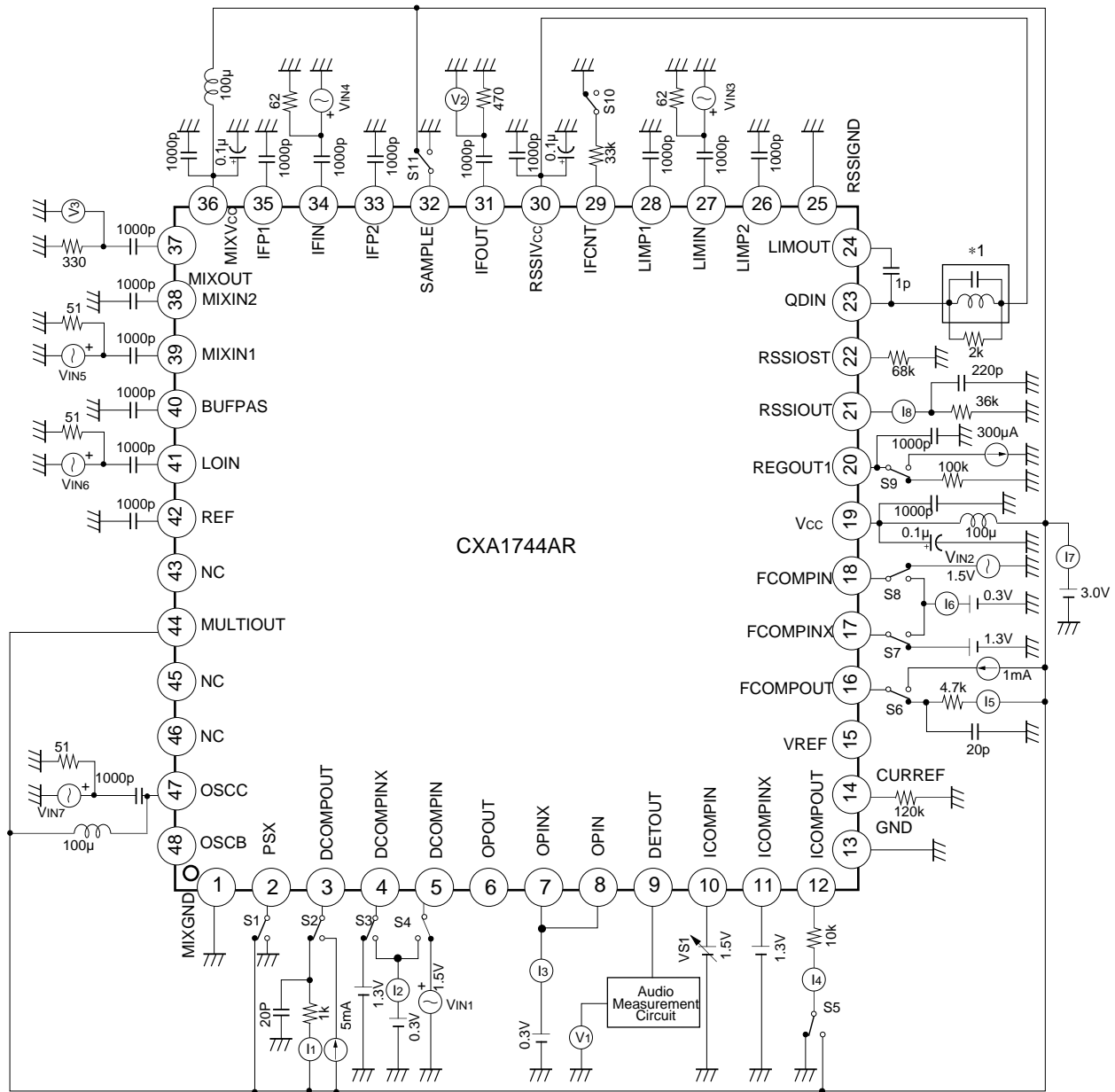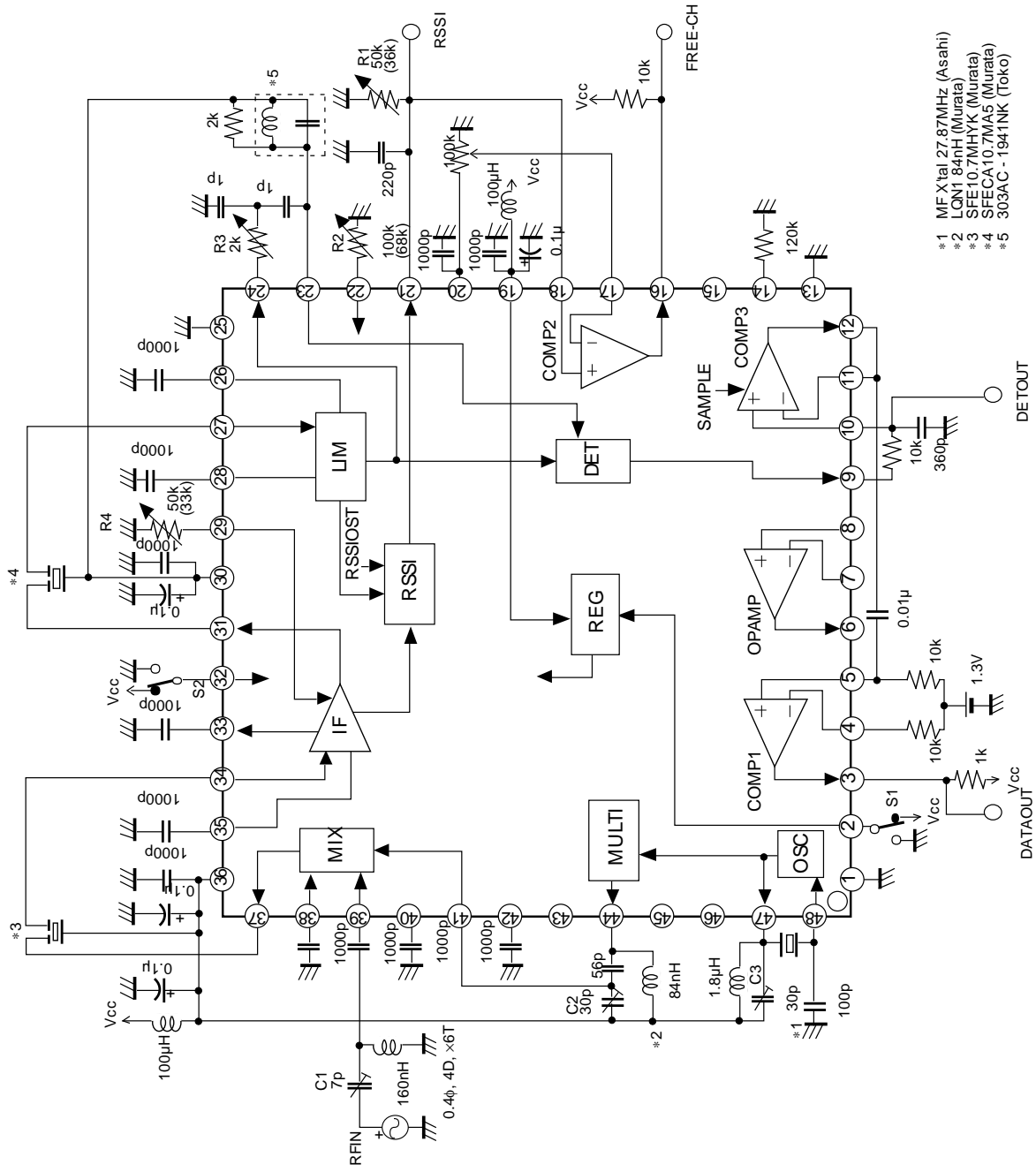
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.
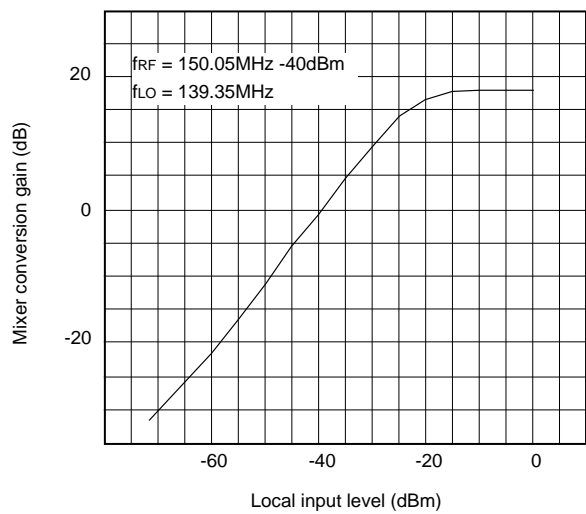
### Mixer input characteristics and 3rd order intercept point

Output level (dBm) vs RF input level (dBm)

$f_{LD} = 139.35MHz, -10dBm$
$f_{RF1} = 150.05MHz$
$f_{RF2} = 150.15 MHz$

### Mixer conversion gain frequency characteristics

Conversion gain (dB) vs RF input frequency (Hz)

$f_{LO} = f_{RF} -10.7MHz$
RF input level = -40dBm
LO input level = -10dBm

### Local input level vs. Mixer conversion gain

Mixer conversion gain (dB) vs Local input level (dBm)

$f_{RF} = 150.05MHz -40dBm$
$f_{LO} = 139.35MHz$

### IF amplifier voltage gain frequency characteristics

Voltage gain (dB) vs IF amplifier input frequency (Hz)

IF amplifier input level = -60dBm

### Limiter voltage gain frequency characteristics

Voltage gain (dB) vs Limiter input frequency (Hz)

Limiter input level = -80dBm
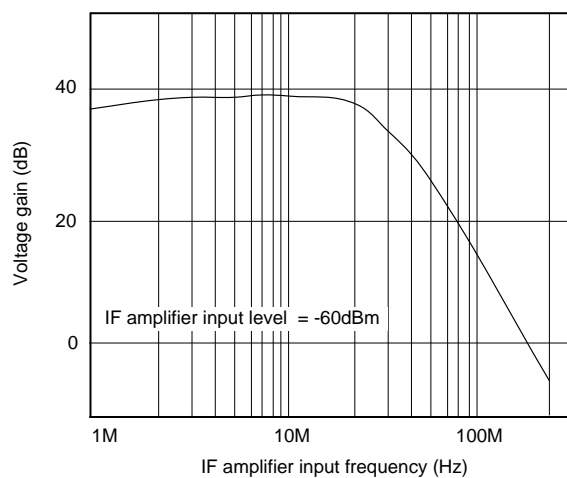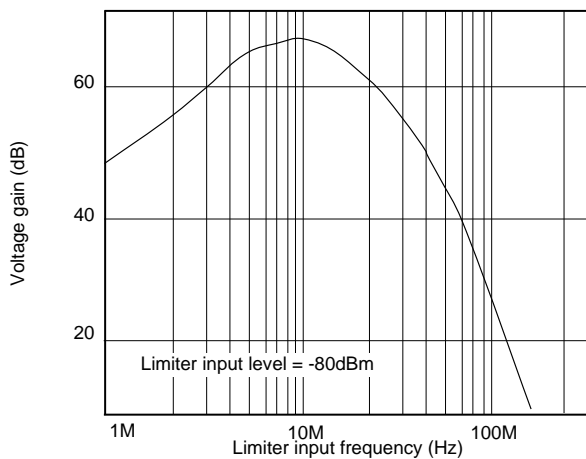
### Detector output frequency characteristics

Output level (dB) vs Audio frequency (Hz)

$f_{LIM} = 10.7MHz, -10dBm$
$f_{DEV} = \pm25.4kHz$

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## RSSI characteristics



RSSI output voltage (V) vs. RF input level (dBm)

$f_{RF} = 150.05\text{MHz}$
$f_{LO}$:Built-in OSC used

+25°C
−20°C
+75°C

## DET output characteristics



Output level (dB) vs. RF input level (dBm)

$f_{RF} = 150.05\text{MHz}$
$f_{DEV} = \pm25.4\text{kHz}$
$f_{MOD} = 36\text{kHz}$
$f_{LO}$: Built-in OSC used

S+D+N

$\dfrac{D+N}{S+D+N}$

N
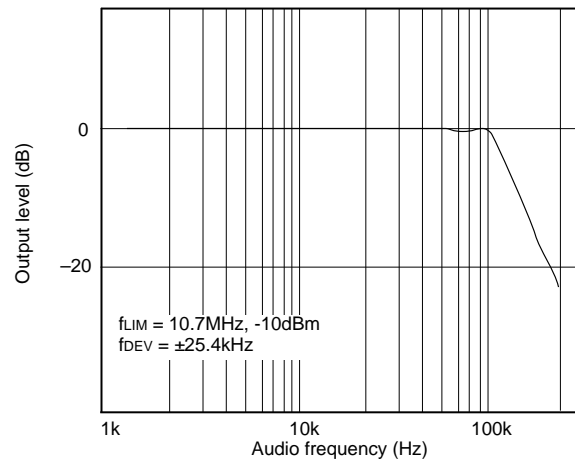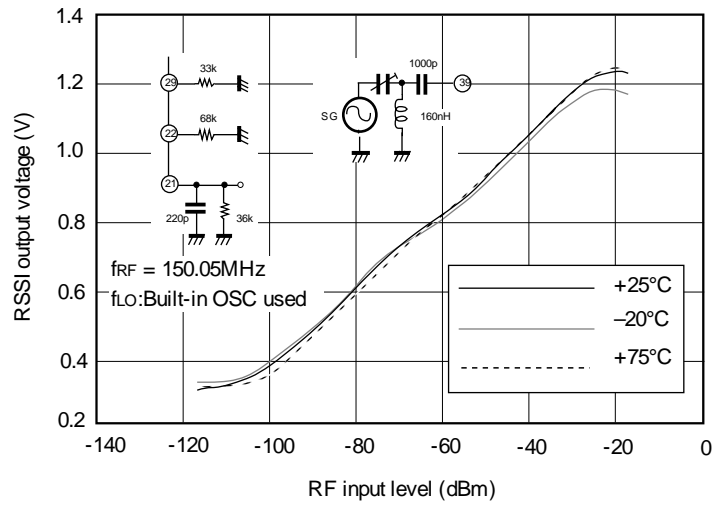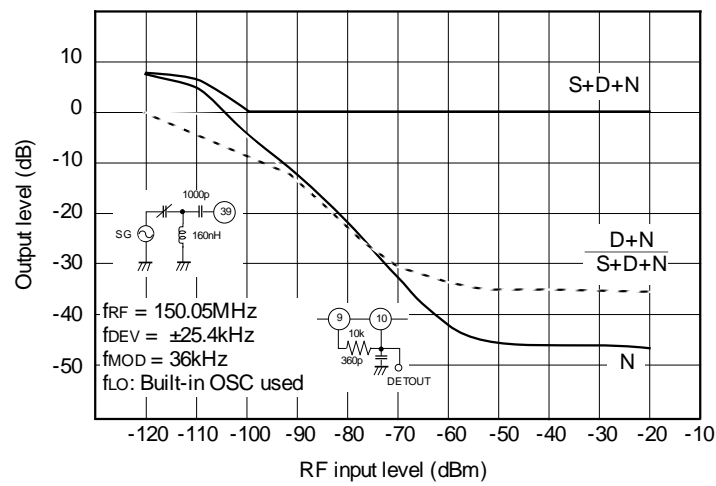
## Supply voltage vs. Current consumption



Current consumption (mA) vs. Supply voltage (V)

For operating

For power saving
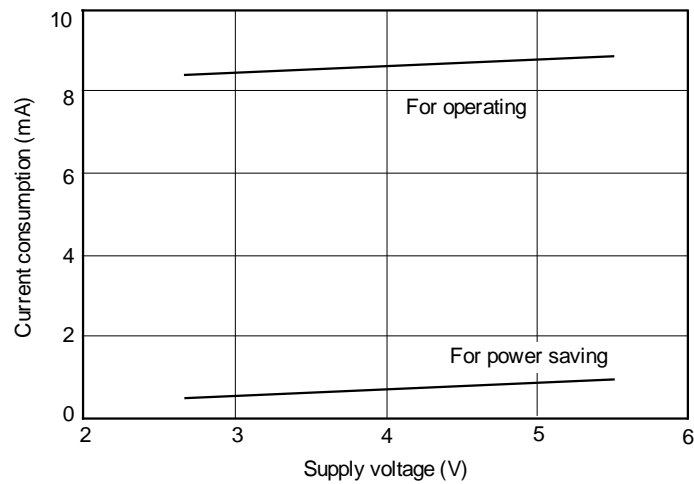
**Description of Operation**

• The signals which have been input from Pins 38 and 39 are mixed with the local oscillation signal from the oscillator and multiplier at the mixer, and the frequency-converted signal is output from Pin 37.  The oscillator can be self-oscillated by composing the Colpitts-type crystal oscillation circuit between Pins 47 and 48. Also, the external local oscillation signal can be directly input to Pin 47.

• After the bandwidth is limited by filter, the mixer output signal is amplified by the IF amplifier and output from Pin 31. The IF amplifier output signal is limited its bandwidth again,  and the amplitude is limited by the limiter amplifier and output from Pin 24. The limiter amplifier output signal is phase-shifted by LC resonance circuit and the signal is output from Pin 9 after being quadrature-detected.

• The RSSI output is the currents corresponding to the input level at the IF amplifier and limiter amplifier. The current signal can be converted into a voltage signal by connecting a proper I-V conversion circuit to Pin 21.

Notes of Operation

Take care of the followings because the CXA1744AR has the IF amplifier voltage gain of approximately 34 dB and limiter amplifier voltage gain of approximately 67 dB and uses high frequency.

1.  Use as wide pattern as possible for the power supply line and GND, and insert a by-pass capacitor as close to them as possible.

2.  Separate the input line from the output line as far as possible and make the wiring short.

3.  Ground the decoupling capacitors of mixer (Pins 38, 40 and 42), IF amplifier (Pins 33 and 35) and limiter amplifier (Pins 26 and 28) as close to each pin as possible.

Notes on Application

1)  Power supply

This IC has a built-in voltage regulator so that the supply voltage range is wide (2.7 to 5.5 V) and stable. There are three power supply pins and GND pins (Pins 19, 13 and 36, 1  and 30, 25).

Ground a decoupling capacitor as close to each power supply pin as possible.

2)  Oscillator

The oscillator in this IC varies its current consumption according to the oscillation level.

The figures below show how to use the CXA1744AR oscillator.

(a)  Configuring a Colpitts oscillation circuit.

(b)  Inputting a local oscillation signal from an external circuit.

Input a signal of approximately 0 dBm to stabilize the oscillator operation and reduce the current consumption.
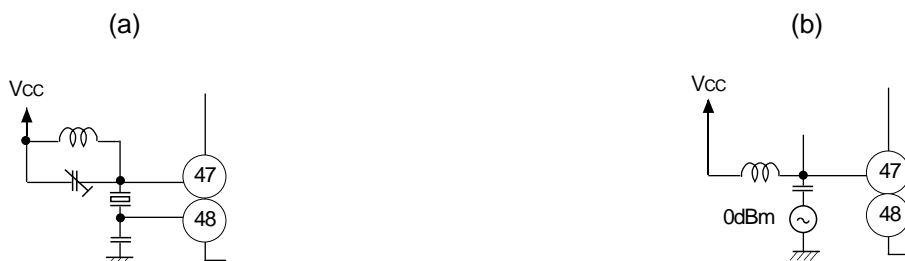
3) Multiplier

The ×5 multiplier is provided in this IC for mixer local signal. The fifth-order component of the input signal is extracted by the resonance circuit connected to Pin 44 externally. Wire the resonance circuit as close to Pin 44 as possible.

4) Mixer

The CXA1744AR mixer is of double balanced type. Its input is at Pins 38 and 39; when input from Pin 39, Pin 38 should be grounded with a capacitor.

5) 10.7 MHz filter

The mixer output impedance and IF amplifier input impedance are approximately 330 Ω. The IF amplifier output impedance and limiter amplifier input impedance are approximately 460 Ω. Use the 10.7 MHz filter with matching.

6) Detector

For quadrature FM detection, the phase of the limiter output (Pin 24) is shifted 90° by the RLC parallel resonance circuit or discriminator as the output is input to pin 23.

The phase shifter by RLC parallel resonance circuit is shown below. In this case, values of L and C are determined so that the center frequency of the second IF signal and the parallel resonance frequency are equal. As the value of R sets the detector output level, select this value so as to obtain the required output level.

With regards to the detector input, the center frequency of the second IF signal and the frequency for the minimum value of the detector distortion does not match because the internal delay is more than the external one. Add the delay circuit as shown below to match the center frequency of the second IF signal and the frequency for the minimum value of the detector distortion.

[____] Delay circuit



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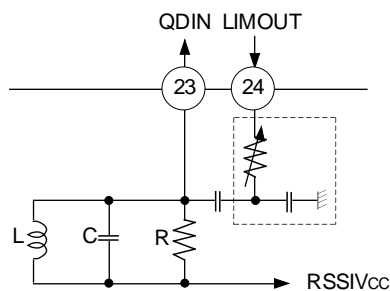
7)  RSSI

RSSI detects the input signal level, and the current is output in this IC. If the voltage output is necessary, I-V conversion should be made by use of a resistor, etc.

This IC can compensate for the unevenness of the filter connected between the IF amplifier and limiter amplifier. Pin 29 is used to perform the adjustment so that the line of the RSSI output characteristics is as straight as possible.

Also, RSSI offset adjustment pin (Pin 22) is provided in this IC. For example, the RSSI offset amount is adjusted to match the dynamic range used in the next-stage IC.

8)  Comparator

This IC has three comparators and they are designed according to the following applications.

COMP1 performs the waveform shaping of the demodulated audio signal and outputs the resulting signal as a rectangular wave.

COMP2 is used to detect the free channel or the signal strength after the RSSI output voltage is input.

COMP3 is the current output-type comparator. The COMP3 output can be turned ON/OFF by setting Pin 32 High/Low and this comparator can form a part of a sample-and-hold circuit. The rise time of the demodulated signal during burst operating can be shortened.

9)  PSX

This is the power save control pin (Pin 2). The power save function is performed by setting this pin Low; the functional blocks except OSC are in the power save mode.

**Package Outline**    Unit : mm

48PIN LQFP (PLASTIC)



NOTE: "∗" Dimensions do not include mold protrusion.

DETAIL **A**

PACKAGE STRUCTURE
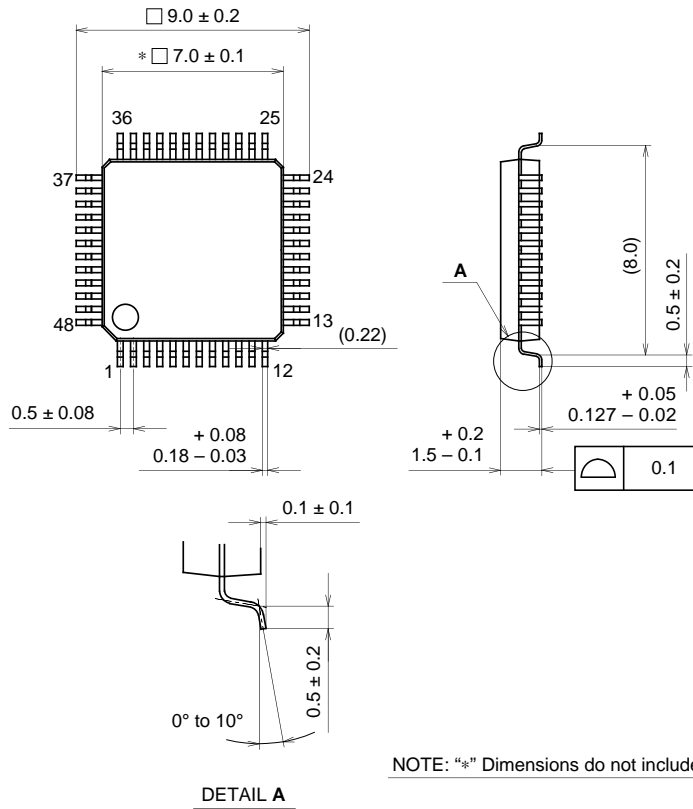
| PACKAGE MATERIAL | EPOXY / PHENOL RESIN |
|---|---|
| LEAD TREATMENT | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE WEIGHT | 0.2g |

| SONY CODE | LQFP-48P-L01 |
|---|---|
| EIAJ CODE | QFP048-P-0707 |
| JEDEC CODE | ———— |