

## 6-bit 140 MSPS Flash A/D Converter

**Description**

The CXA1826Q is a 6-bit high-speed flash A/D converter IC capable of digitizing analog signals at the maximum rate of 140 MSPS. The digital input/output level is compatible with the ECL 100K/10KH/10K.

**Features**

- Ultra-high speed operation with maximum conversion rate of 140 MSPS
- Low input capacitance
- Wide analog input bandwidth
- Low power consumption
- Low error rate

**Function**

6-bit 140 MSPS flash AD converter

32 pin QFP (Plastic)

**Structure**

Bipolar silicon monolithic IC

**Applications**

CRT PRML QAM

**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

|                           |                 |              |    |
|---------------------------|-----------------|--------------|----|
| • Supply voltage          | AVEE, DVEE      | -7 to +0.5   | V  |
| • Analog input voltage    | VIN             | -2.7 to +0.5 | V  |
| • Reference input voltage | VRT, VRB        | -1.5 to +0.5 | V  |
|                           | VRT-VRB         | 2.5          | V  |
| • Digital input voltage   | CLKP, CLKN, INV | -4 to +0.5   | V  |
|                           | CLKP-CLKN       | 2.7          | V  |
| • Digital output current  | ID0 to ID5      | -30 to 0     | mA |
| • Storage temperature     | Tstg            | -65 to +150  | °C |

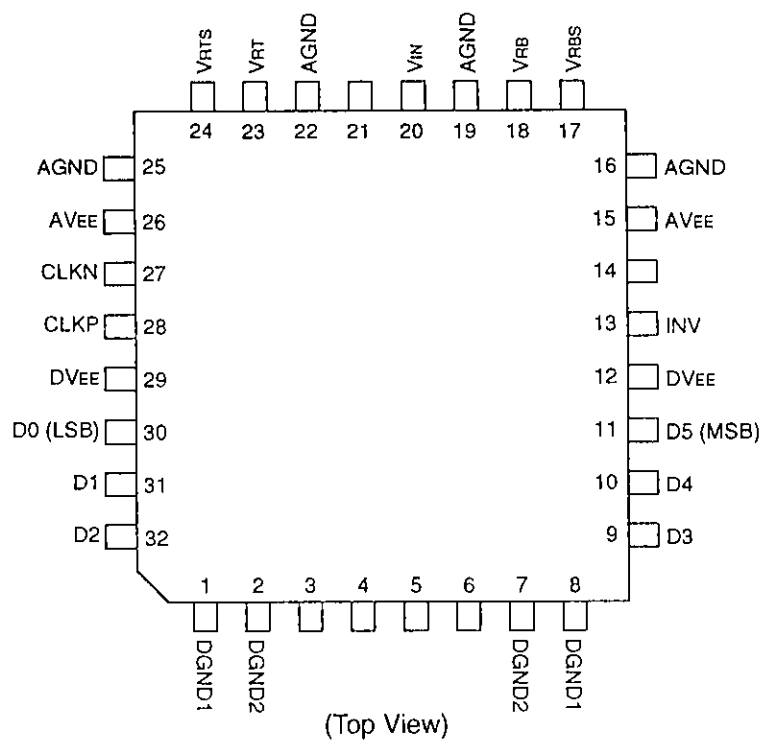
**Recommended Operating Conditions**

|                           |            | Min.  | Typ. | Max.  |    |
|---------------------------|------------|-------|------|-------|----|
| • Supply voltage          | AVEE, DVEE | -5.5  | -5.2 | -4.95 | V  |
|                           | AVEE-DVEE  | -0.05 | 0    | 0.05  | V  |
|                           | AGND-DGND  | -0.05 | 0    | 0.05  | V  |
| • Reference input voltage | VRT        | -0.1  | 0    | 0.1   | V  |
|                           | VRB        | -2.2  | -2.0 | -1.8  | V  |
| • Analog input voltage    | VIN        | VRB   |      | VRT   |    |
| • Pulse width of clock    | TPW1       | 3.0   |      |       | ns |
|                           | TPW0       | 3.0   |      |       | ns |
| • Operating temperature   | Ta         | -20   |      | 75    | °C |

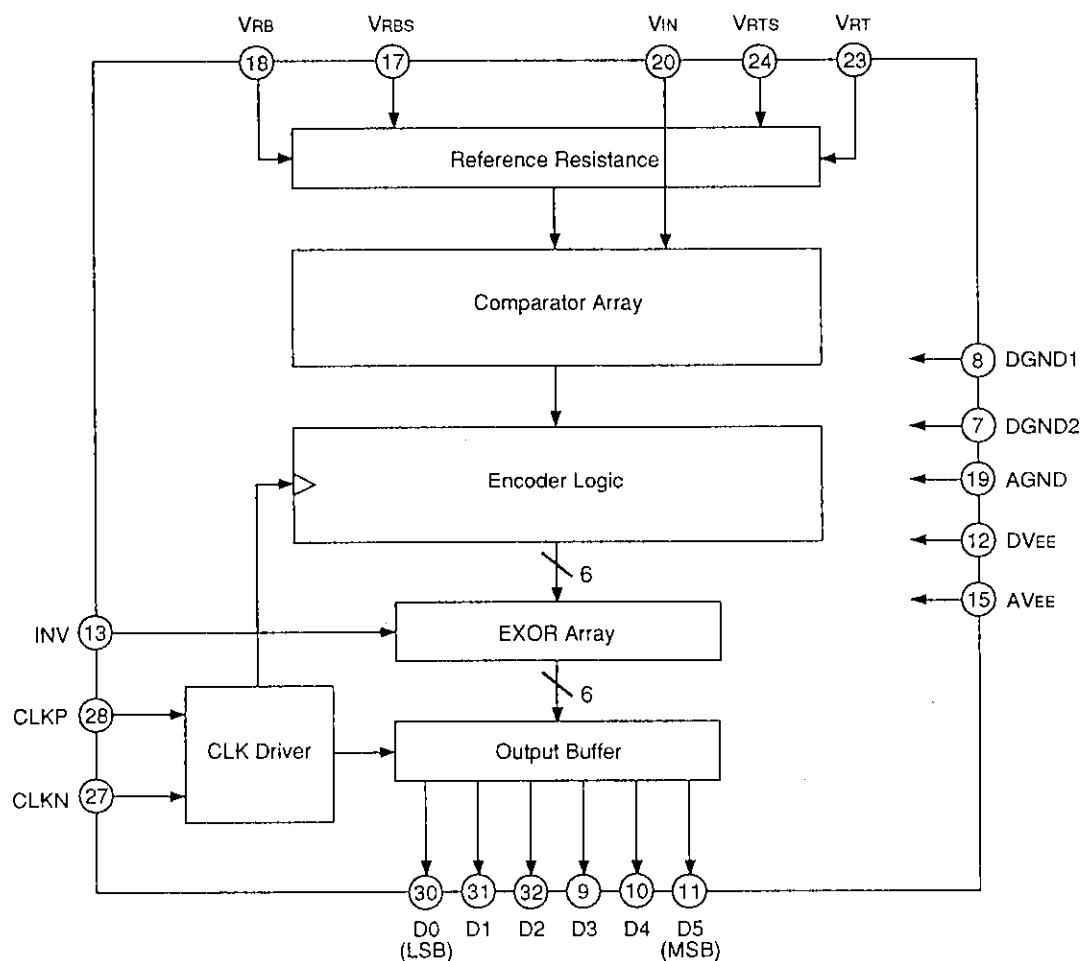
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## Pin Configuration

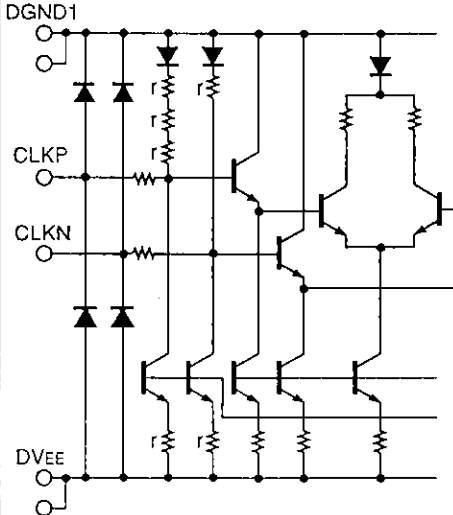
Pins without name are NC pins (not connected).

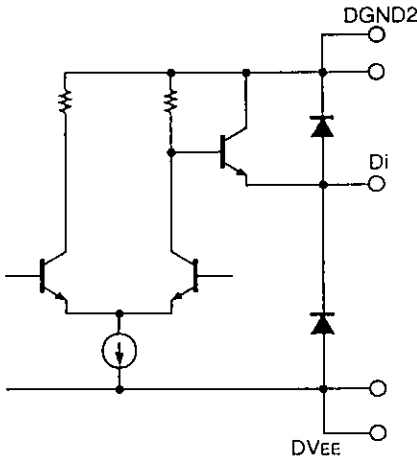
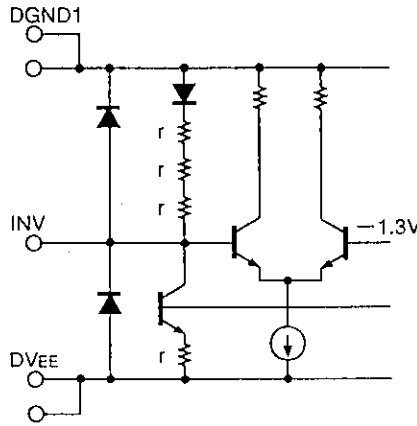
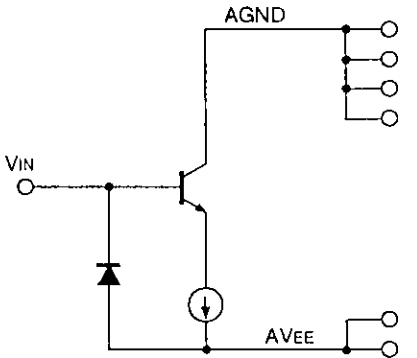


## Block Diagram



## Pin Description and I/O Pin Equivalent Circuit

| Pin No.        | Symbol | I/O | Typical voltage level | Equivalent circuit                                                                  | Description                                                                                                                                                                                                                                                  |
|----------------|--------|-----|-----------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16, 19, 22, 25 | AGND   | —   | 0V                    |                                                                                     | Analog GND.<br>Used as GND for input buffers and latches of comparators. Separated from DGND1 and DGND2.                                                                                                                                                     |
| 15, 26         | AVEE   | —   | −5.2V                 |                                                                                     | Analog VEE.<br>Typical voltage is −5.2V.<br>Connected internally with DVEE.<br>(Resistance is 4 to 6 $\Omega$ .)<br>Connect to AGND through a ceramic chip capacitor of 0.1 $\mu$ F or more just near the pin.                                               |
| 28             | CLKP   | I   | ECL                   |  | CLK input.                                                                                                                                                                                                                                                   |
| 27             | CLKN   |     |                       |                                                                                     | CLK complementary input.<br>When left open, voltage goes to ECL threshold potential (−1.3V). Although only CLKP input can be used for operation with CLKN input open, complementary input is recommended in order to attain high speed and stable operation. |
| 1, 8           | DGND1  | —   | 0V                    |                                                                                     | Digital GND for internal circuits.                                                                                                                                                                                                                           |
| 2, 7           | DGND2  | —   | 0V                    |                                                                                     | Digital GND for output transistors.                                                                                                                                                                                                                          |
| 12, 29         | DVEE   | —   | −5.2V                 |                                                                                     | Digital VEE.<br>Connected internally with AVEE. (Resistance is 4 to 6 $\Omega$ .) Connect to DGND through a ceramic chip capacitor of 0.1 $\mu$ F or more just near the pin.                                                                                 |

| Pin No. | Symbol | I/O | Typical voltage level | Equivalent circuit                                                                   | Description                                                                                                                             |
|---------|--------|-----|-----------------------|--------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 30      | D0     | O   | ECL                   |    | LSB of data output.<br>External pull-down resistor is required.                                                                         |
| 31      | D1     |     |                       |                                                                                      | Data output.<br>External pull-down resistors are required.                                                                              |
| 32      | D2     |     |                       |                                                                                      |                                                                                                                                         |
| 9       | D3     |     |                       |                                                                                      |                                                                                                                                         |
| 10      | D4     |     |                       |                                                                                      | MSB of data output.<br>External pull-down resistor is required.                                                                         |
| 11      | D5     |     |                       |                                                                                      |                                                                                                                                         |
| 13      | INV    | I   | ECL                   |   | Output polarity inversion input for D0 (LSB) to D5 (MSB). (Refer to the output code table.)<br>When left open, Low level is maintained. |
| 20      | VIN    | I   | VRT to VRB            |  | Analog input.                                                                                                                           |

| Pin No.                | Symbol | I/O | Typical voltage level | Equivalent circuit                                                                                                                                                                                                                                                                                                                                                                                                      | Description                                                                                                                                                                                                                                          |
|------------------------|--------|-----|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18                     | VRB    | I   | -2V                   | <p>The diagram shows a vertical chain of resistors labeled 'r'. At the top, a network of inputs VRT and VRTS is connected to the chain through resistor r1. The chain passes through several comparators: Comparator 1, Comparator 2, Comparator 30, Comparator 31, Comparator 32, Comparator 33, and Comparator 63. At the bottom, a network of inputs VRBS and VRB is connected to the chain through resistor r3.</p> | Reference voltage (bottom) force; typical voltage is -2V. Connect to AGND through a ceramic chip capacitor of 0.1 $\mu$ F or more and a tantalum capacitor of 10 $\mu$ F or more just near the pin.                                                  |
| 17                     | VRBS   |     |                       |                                                                                                                                                                                                                                                                                                                                                                                                                         | Reference voltage (bottom) sense.                                                                                                                                                                                                                    |
| 23                     | VRT    | I   | 0V                    |                                                                                                                                                                                                                                                                                                                                                                                                                         | Reference voltage (top) force; typical voltage is 0V. When applying a voltage other than AGND to this pin, connect to AGND through a ceramic chip capacitor of 0.1 $\mu$ F or more and a tantalum capacitor of 10 $\mu$ F or more just near the pin. |
| 24                     | VRTS   |     |                       |                                                                                                                                                                                                                                                                                                                                                                                                                         | Reference voltage (top) sense.                                                                                                                                                                                                                       |
| 3, 4<br>5, 6<br>14, 21 | NC     | —   | —                     |                                                                                                                                                                                                                                                                                                                                                                                                                         | Not connected. Although not connected in the IC, it is recommended that these pins should be connected to AGND or DGND on printed circuit board.                                                                                                     |

## Electrical Characteristics

(Ta=25°C, AV<sub>EE</sub>=DV<sub>EE</sub>=-5.2V, V<sub>RT</sub>=0V, V<sub>RB</sub>=-2V)

| Item                           | Symbol           | Conditions                                                                                          | Min.  | Typ.     | Max.  | Unit     |
|--------------------------------|------------------|-----------------------------------------------------------------------------------------------------|-------|----------|-------|----------|
| Resolution                     | n                |                                                                                                     | 6     | 6        | 6     | bits     |
| DC characteristics             |                  |                                                                                                     |       |          |       |          |
| Integral linearity error       | EIL              | F <sub>C</sub> =140MHz                                                                              | -0.25 |          | +0.25 | LSB      |
| Differential linearity error   | EDL              | F <sub>C</sub> =140MHz                                                                              | -0.25 |          | +0.25 | LSB      |
| Analog input                   |                  |                                                                                                     |       |          |       |          |
| Analog input capacitance       | C <sub>IN</sub>  | V <sub>IN</sub> =-1V+0.07V <sub>ms</sub>                                                            |       | 7        | 18    | pF       |
| Analog input resistance        | R <sub>IN</sub>  |                                                                                                     | 300   |          |       | KΩ       |
| Input bias current             | I <sub>IN</sub>  | V <sub>IN</sub> =-1V                                                                                |       |          | 400   | μA       |
| Reference input                |                  |                                                                                                     |       |          |       |          |
| Reference resistance           | R <sub>REF</sub> |                                                                                                     |       | 200      |       | Ω        |
| Offset voltage V <sub>RT</sub> | E <sub>OT</sub>  |                                                                                                     |       |          | 20    | mV       |
| VRB                            | E <sub>OB</sub>  |                                                                                                     |       |          | 20    | mV       |
| Digital input                  |                  |                                                                                                     |       |          |       |          |
| Logic high level               | V <sub>IH</sub>  |                                                                                                     | -1.13 |          | -0.65 | V        |
| Logic low level                | V <sub>IL</sub>  |                                                                                                     | -2.1  |          | -1.50 | V        |
| Logic high current             | I <sub>IH</sub>  | Apply -0.8V to input                                                                                | 0     |          | 50    | μA       |
| Logic low current              | I <sub>IL</sub>  | Apply -1.6V to input                                                                                | -50   |          | 50    | μA       |
| Input capacitance              |                  |                                                                                                     |       | 7        |       | pF       |
| Switching characteristics      |                  |                                                                                                     |       |          |       |          |
| Maximum conversion frequency   | F <sub>C</sub>   | Error rate 1E-9 TPS*1                                                                               | 140   |          |       | MSPS     |
| Aperture jitter                | T <sub>aj</sub>  |                                                                                                     |       | 10       |       | ps       |
| Sampling delay                 | T <sub>ds</sub>  |                                                                                                     |       | 1.5      |       | ns       |
| High pulse width of clock      | TPW <sub>1</sub> |                                                                                                     | 3.0   |          |       | ns       |
| Low pulse width of clock       | TPW <sub>0</sub> |                                                                                                     | 3.0   |          |       | ns       |
| Digital output                 |                  |                                                                                                     |       |          |       |          |
| Logic high level               | V <sub>OH</sub>  | R <sub>L</sub> =100Ω to -2V                                                                         | -1.10 |          | -0.65 | V        |
| Logic low level                | V <sub>OL</sub>  | R <sub>L</sub> =100Ω to -2V                                                                         | -2.1  |          | -1.6  | V        |
| Output delay                   | T <sub>do</sub>  | R <sub>L</sub> =100Ω to -2V                                                                         | 3.0   | 3.6      | 4.2   | ns       |
| Output rise time               | T <sub>r</sub>   | R <sub>L</sub> =100Ω to -2V, 20% to 80%                                                             |       | 0.8      |       | ns       |
| Output fall time               | T <sub>f</sub>   | R <sub>L</sub> =100Ω to -2V, 20% to 80%                                                             |       | 1.0      |       | ns       |
| Dynamic characteristics        |                  |                                                                                                     |       |          |       |          |
| Amplitude input bandwidth      |                  | f <sub>CLK</sub> =140MHz, f <sub>IN</sub> =69.999MHz                                                | 200   |          |       | MHz      |
| Error rate                     |                  | Error Amplitude ≥ 4LSB<br>3dB down of fullscale input                                               |       |          | 1E-09 | TPS*1    |
| S/N ratio                      | SNR              | f <sub>CLK</sub> =140MHz, f <sub>IN</sub> =1MHz<br>f <sub>CLK</sub> =140MHz, f <sub>IN</sub> =35MHz |       | 36<br>34 |       | dB<br>dB |
| Power supply                   |                  |                                                                                                     |       |          |       |          |
| Supply current                 | I <sub>EE</sub>  | AV <sub>EE</sub> =DV <sub>EE</sub> =-5.2V                                                           | -60   | -40      | -25   | mA       |
| Power consumption              | P <sub>d</sub>   |                                                                                                     |       | 225      |       | mW       |

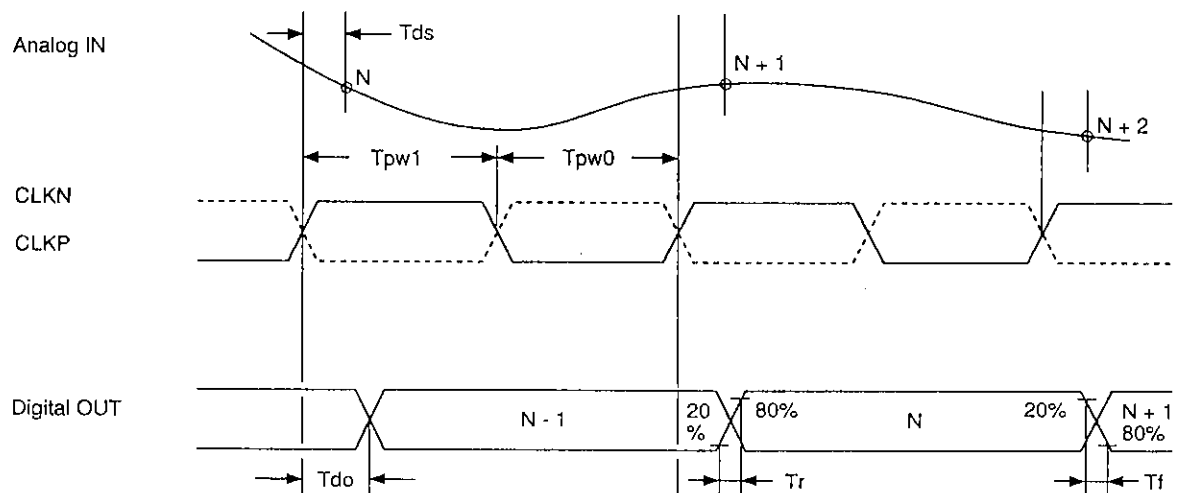
\*1 TPS: Times Per Sample

## Output Code Table

| VIN*  | Step | INV: 1 |        | INV: 0 |    |
|-------|------|--------|--------|--------|----|
|       |      | D5     | D0     | D5     | D0 |
| 0V    | 0    | 000000 | 111111 |        |    |
|       | 1    | 000001 | 111110 |        |    |
|       |      | ⋮      | ⋮      |        |    |
| -1.0V | 31   | 011111 | 100000 |        |    |
|       | 32   | 100000 | 011111 |        |    |
|       |      | ⋮      | ⋮      |        |    |
| -2.0V | 62   | 111110 | 000001 |        |    |
|       | 63   | 111111 | 000000 |        |    |

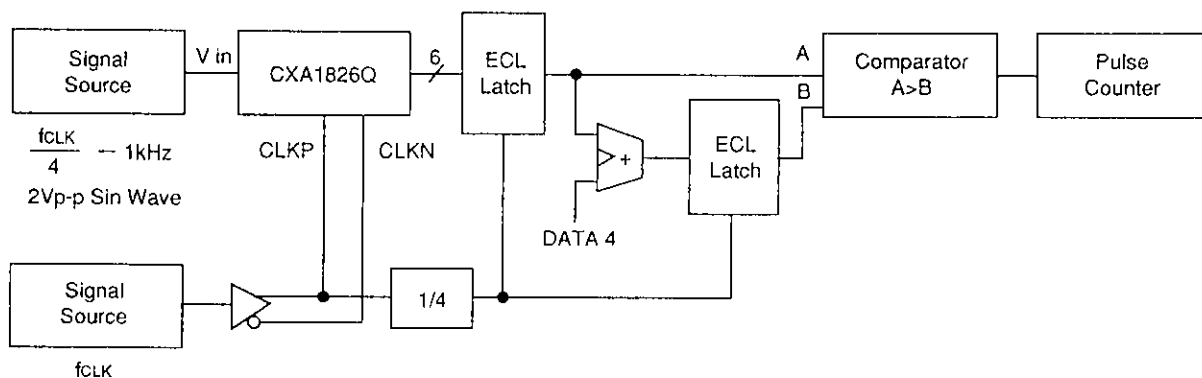
V<sub>RT</sub>=0V, V<sub>RB</sub>=-2V

## Timing Diagram

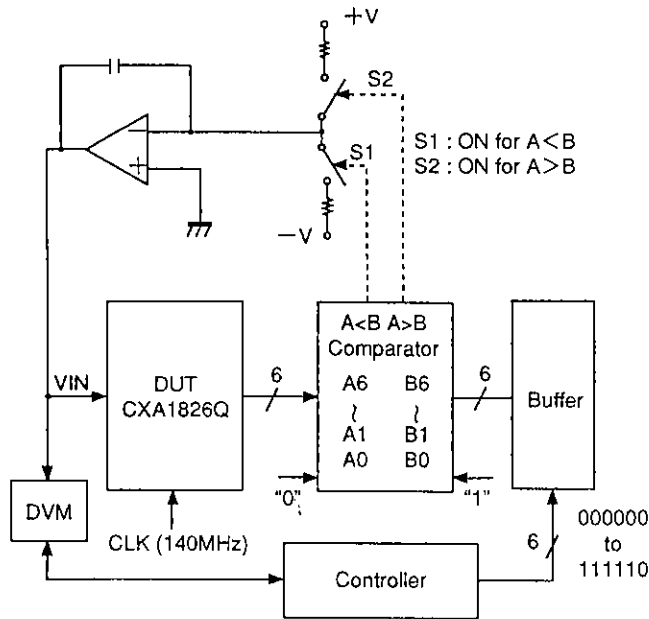


## Electrical Characteristics Measurement Circuit

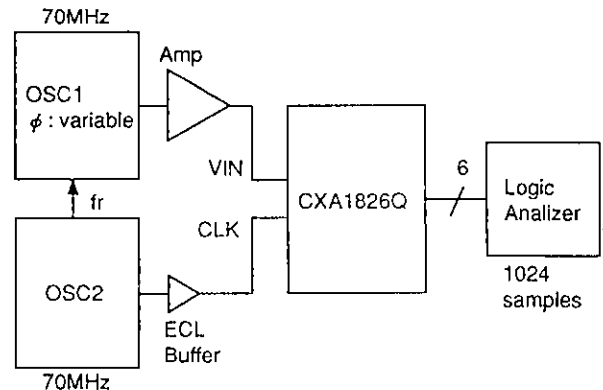
## Maximum conversion rate measurement circuit



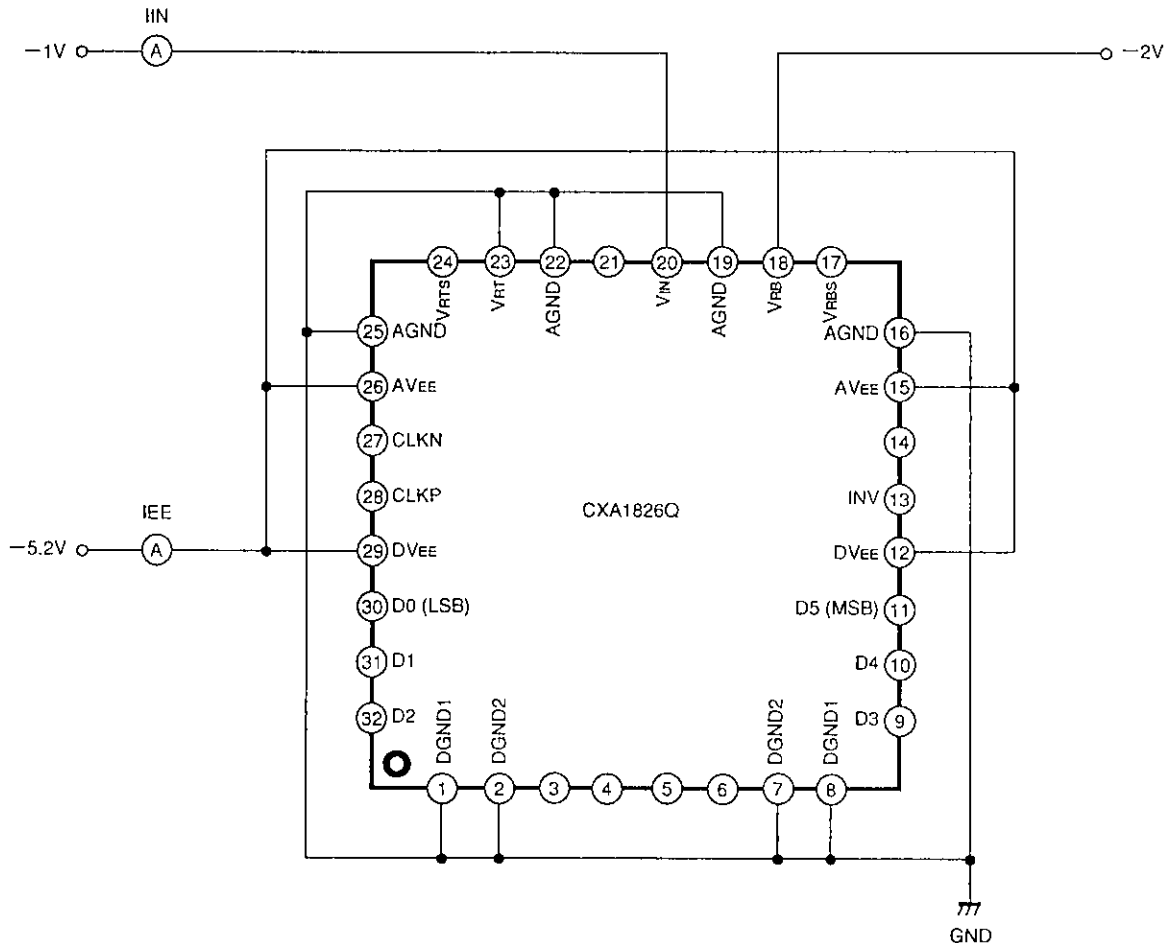
**Integral linearity error measurement circuit**  
**Differential linearity error measurement circuit**



**Sampling delay measurement circuit**  
**Aperture jitter measurement circuit**



**Supply current measurement circuit**  
**Analog input bias current measurement circuit**



## 6bit, 140MHz ADC Evaluation board

### Description

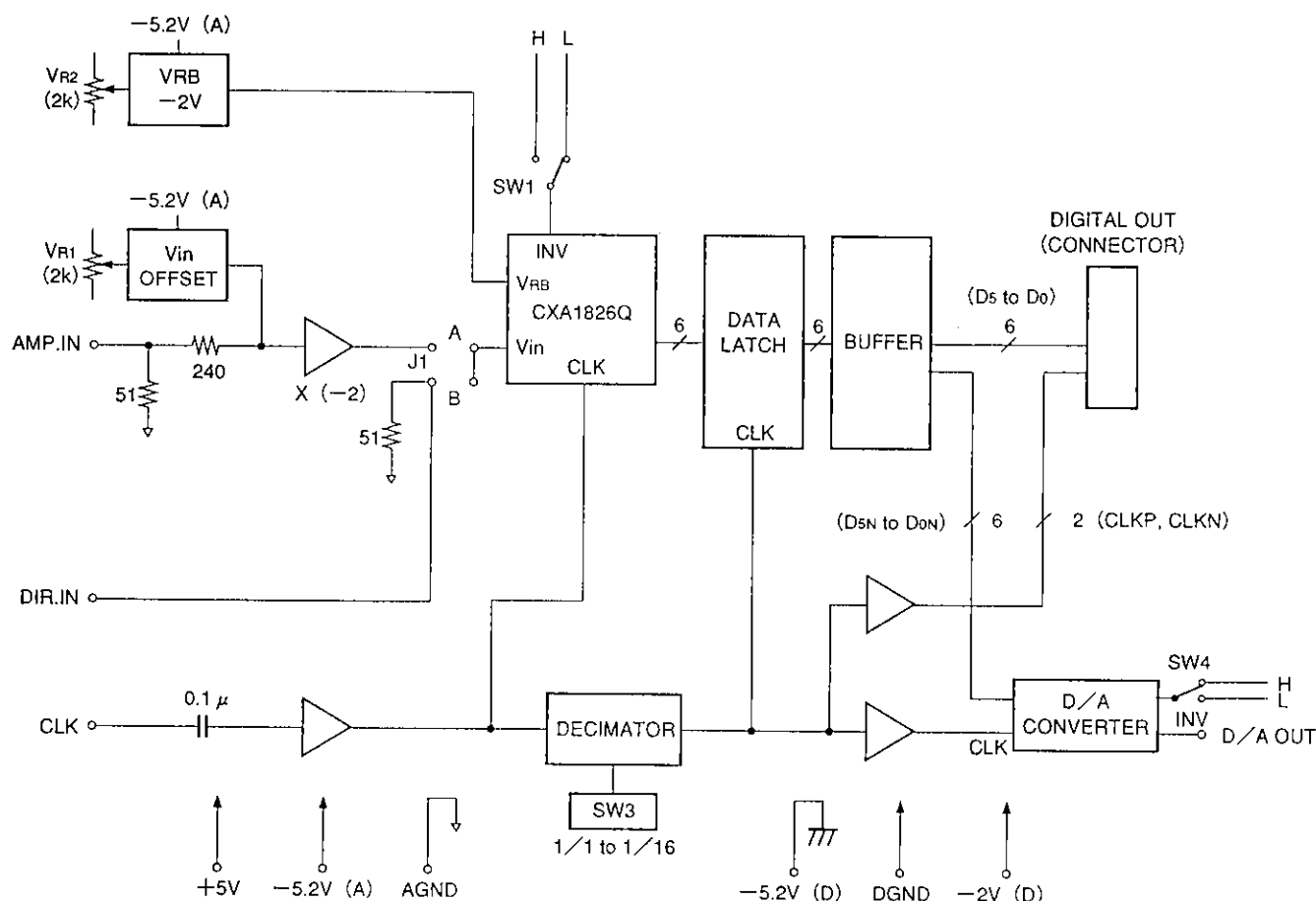
The CXA1826Q EVALUATION BOARD WITH DAC is a tool for customers to evaluate the performance of the CXA1826Q (6bit, 140MHz, high-speed A/D converter). In addition to indispensable features such as the reference voltage generator, this tool equips two sets of analog inputs (the AC coupled input and the operation amplifier input), the input voltage offset generator, the clock decimator, the output data latches, the 10-bit high-speed DAC, and the 20-pin cable connector for digital outputs.

This evaluation board provides full performance of the CXA1826Q and it is designed to facilitate evaluation.

### Features

- Resolution: 6bits
- Maximum conversion rate: 140MHz
- Supply voltage: +5.0V, -5.2V, -2.0V
- Two analog inputs (AC coupled input, operation amplifier input)
- Clock level converter: Sine wave to ECL level signal
- Reference voltage adjustment circuit for the A/D converter
- Built-in clock frequency decimation circuit: (1/1 to 1/16)

### Block Diagram



**Supply Current**

| Item  | Min. | Typ. | Max. | Unit |
|-------|------|------|------|------|
| -5.2V |      | 0.65 | 0.8  | A    |
| +5.0V |      | 15   | 30   | mA   |
| -2.0V |      | 0.35 | 0.5  | A    |

(Note: Supply current -2.0V is the value when Rn10, Rn11 and Rn12 are not mounted.)

**Analog Input (DIR. IN, AMP. IN)**

| Item                    | Min. | Typ. | Max. | Unit     |
|-------------------------|------|------|------|----------|
| Input voltage (DIR. IN) | -2.0 |      | 0    | V        |
| (AMP. IN) *1            | -0.5 |      | +0.5 | V        |
| Input impedance         |      | 50   |      | $\Omega$ |

(\*1: Adjustable by VR1)

**Clock Input (CLK)**

| Item                         | Min. | Typ. | Max. | Unit     |
|------------------------------|------|------|------|----------|
| Input voltage (Peak to Peak) |      | 1.0  |      | Vp-p     |
| Input impedance              |      | 50   |      | $\Omega$ |

**Digital Output (D0 to D5)**

ECL 10kH level

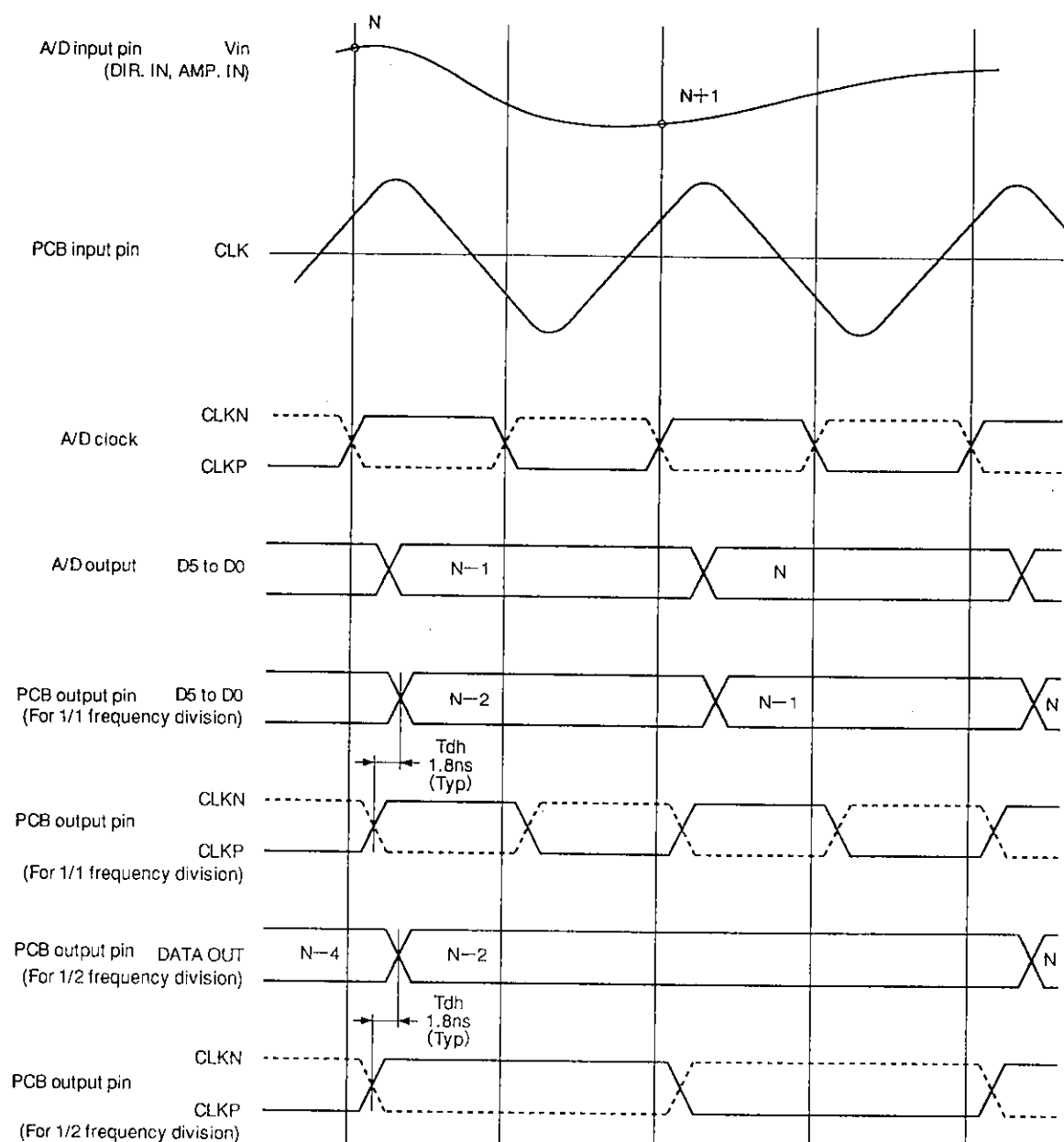
**Clock Output**

ECL 10kH level, complementary output

**Digital Out of Connector Pin Assignment**

| Pin | Assignment | Pin | Assignment |
|-----|------------|-----|------------|
| 1   | D0 (LSB)   | 2   | DGND       |
| 3   | D1         | 4   | DGND       |
| 5   | D2         | 6   | DGND       |
| 7   | D3         | 8   | DGND       |
| 9   | D4         | 10  | DGND       |
| 11  | D5 (MSB)   | 12  | DGND       |
| 13  | NC         | 14  | DGND       |
| 15  | NC         | 16  | DGND       |
| 17  | CLKP       | 18  | DGND       |
| 19  | CLKN       | 20  | DGND       |

## Timing Chart



## Adjustment Methods and Notes on Operation

1)  $V_{in}$  Offset (VR1)

The volume to adjust the signal range (0V center assumed) with the A/D converter input range when a waveform is input through AMP. IN.

## 2) A/D Full Scale (VR2)

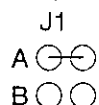
The volume to adjust A/D converter VRB voltage.

- 3) D/A Full Scale (VR4)  
The volume to adjust D/A output full scale (−1V)

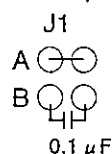
- 4) J1 (Input selection)  
A: Shorts to select AMP.IN input.  
B: Shorts to select DIR.IN input.

[Jumper Position at shipment]

When Op. Amp input is used



When AC coupled input is used



- 5) SW1  
The switch for INV High/Low
- 6) SW3 (Decimation)  
The switch to select clock frequency decimation.  
Switch position : decimation ratio  
0 : 1/1  
1 : 1/2  
2 : 1/4  
3 : 1/8  
4 : 1/16
- 7) SW4 (D/A INV)  
The switch for D/A converter output inversion.
- 8) Rn10, Rn11 and Rn12 are not mounted at shipment. They are not required during evaluation.
- 9) Waveform probe pins P5 and P8 through P28 are devised to facilitate GND connection in order to reduce the distortion. As shown in the diagram below, the distance between the probe point and the GND is 300 mils, and there is  $\phi$  1.2mm throughhole at each. The signal and GND locations are suit for a Tektronix GND tip (part number 013-1185-00).

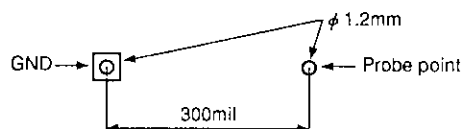
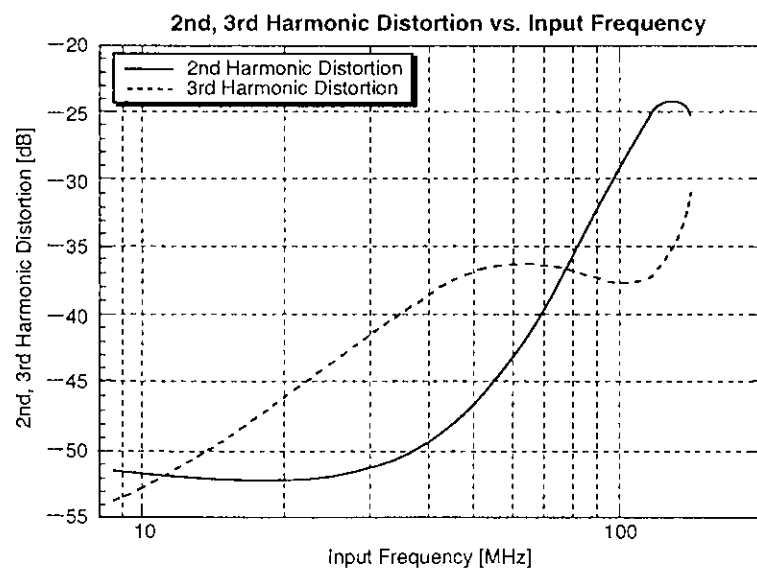
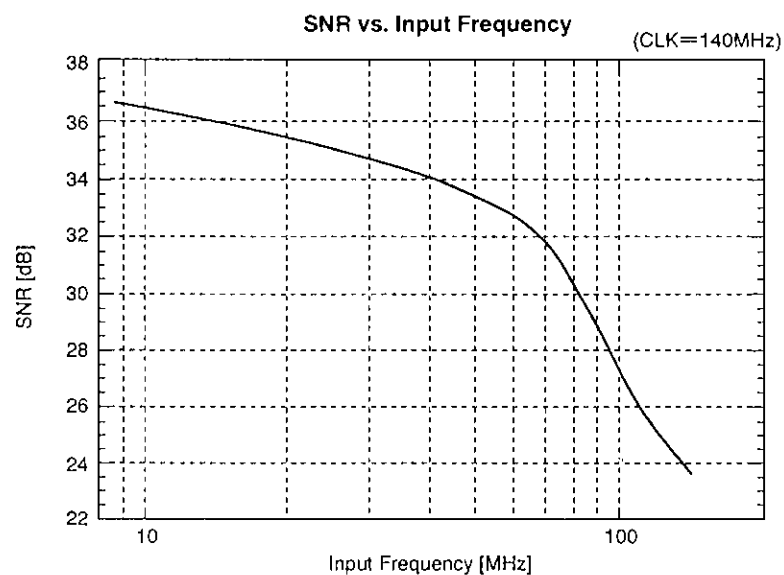
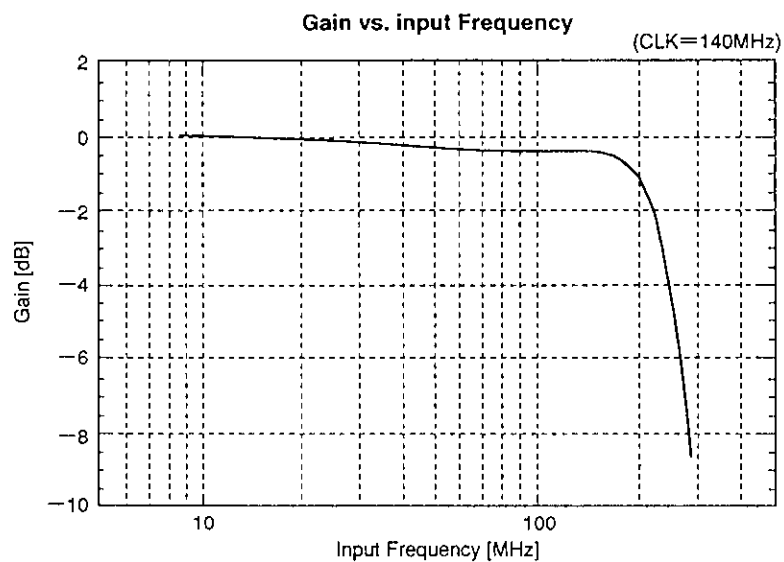


Fig. 3

- 10) D/A converter (IC13) input data (waveform probe pins P21 through P28) are the complementary signals of the decimated A/D converter outputs. Those are inverted again in the D/A converter so that the direction of reproduced waveform can agree with the A/D input signal converter.

## Characteristics



# Part List

## RESISTOR:

|                     |                             |
|---------------------|-----------------------------|
| R1, R14, R18 to R20 | 51 $\Omega$                 |
| R2, R6              | 240 $\Omega$                |
| R4                  | 22K $\Omega$                |
| R5                  | 11K $\Omega$                |
| R7, R21             | 1K $\Omega$                 |
| R8, R10             | 510 $\Omega$                |
| R9                  | 1.3K $\Omega$               |
| R11                 | 43 $\Omega$                 |
| R15, R23            | 330 $\Omega$                |
| R16, R17            | 51 $\Omega$ (CHIP RESISTOR) |
| R22                 | 270 $\Omega$                |

## NETWORK RESISTOR:

|               |              |
|---------------|--------------|
| Rn1, Rn2, Rn7 | 51 $\Omega$  |
| Rn5 to Rn9    | 75 $\Omega$  |
| Rn3, Rn4      | 100 $\Omega$ |

## VARIABLE RESISTOR:

|           |             |
|-----------|-------------|
| VR1, 2, 4 | 2K $\Omega$ |
|-----------|-------------|

## CAPACITOR

|                  |                              |
|------------------|------------------------------|
| C1               | 0.1 $\mu$ F (CERAMIC)        |
| C4, C50          | 3.3 $\mu$ F (TANTALUM)       |
| C6, C7, C15, C26 | 1 $\mu$ F (TANTALUM)         |
| C20              | 10 $\mu$ F (TANTALUM)        |
| C54 to C57       | 33 $\mu$ F (TANTALUM)        |
| OTHERS           | 0.1 $\mu$ F (CHIP CAPACITOR) |

## TRANSISTOR:

|            |            |
|------------|------------|
| Q1         | 2SA970     |
| IC:        |            |
| IC1        | TL4558P    |
| IC2, IC8   | 10H116     |
| IC3, IC14  | TL431CLP   |
| IC4        | CLC404AJP  |
| IC5        | 10H136     |
| IC7        | 10H164     |
| IC9, IC10  | 10H176     |
| IC11, IC12 | 10H101     |
| IC13       | CX20202A-1 |

## DIODE:

|          |         |
|----------|---------|
| D1 to D6 | 1S2076A |
|----------|---------|

## FERRITE BEAD:

|          |            |
|----------|------------|
| LB1, LB2 | ZBF253D-00 |
|----------|------------|

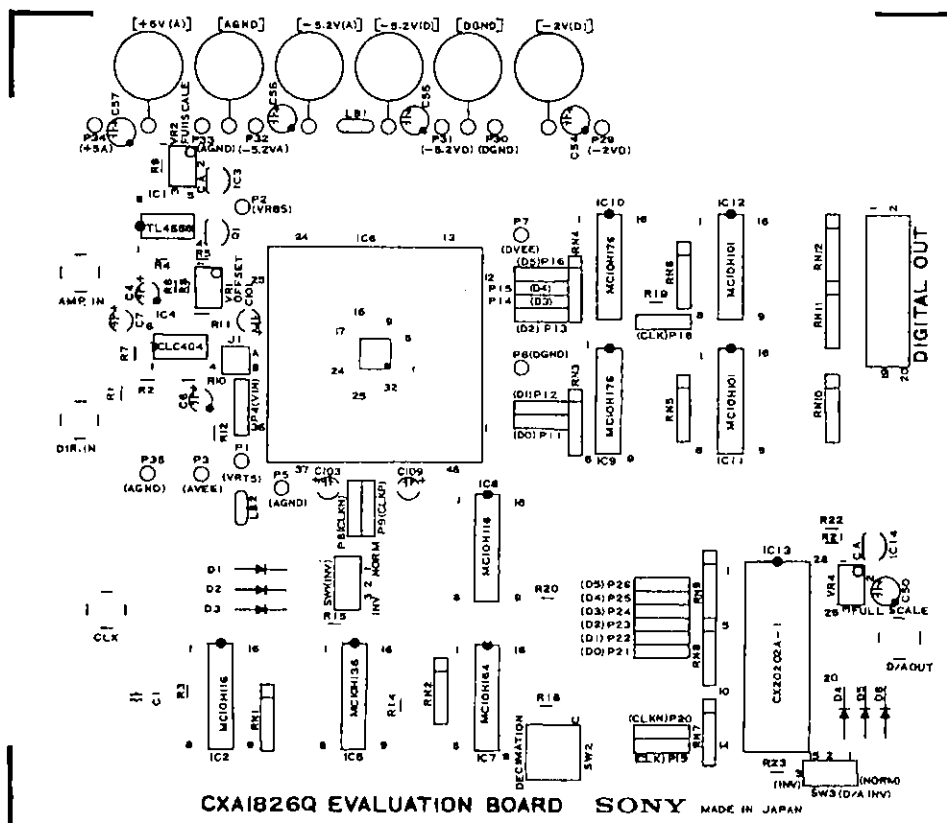
## SWITCH:

|          |              |
|----------|--------------|
| SW1, SW3 | ATE1D-2M3-10 |
| SW2      | S-1010A      |

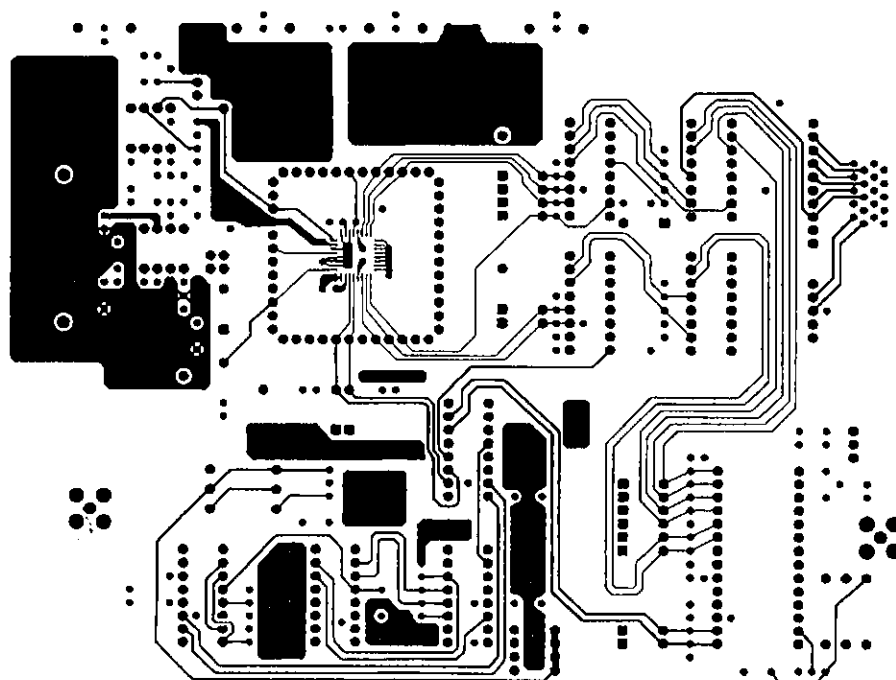
## OTHERS

|                |                |
|----------------|----------------|
| SMA CONNECTOR  | TMA5502-10     |
| Dout CONNECTOR | 8830E-020-170S |
| JUMPER LINE    | JX-1           |

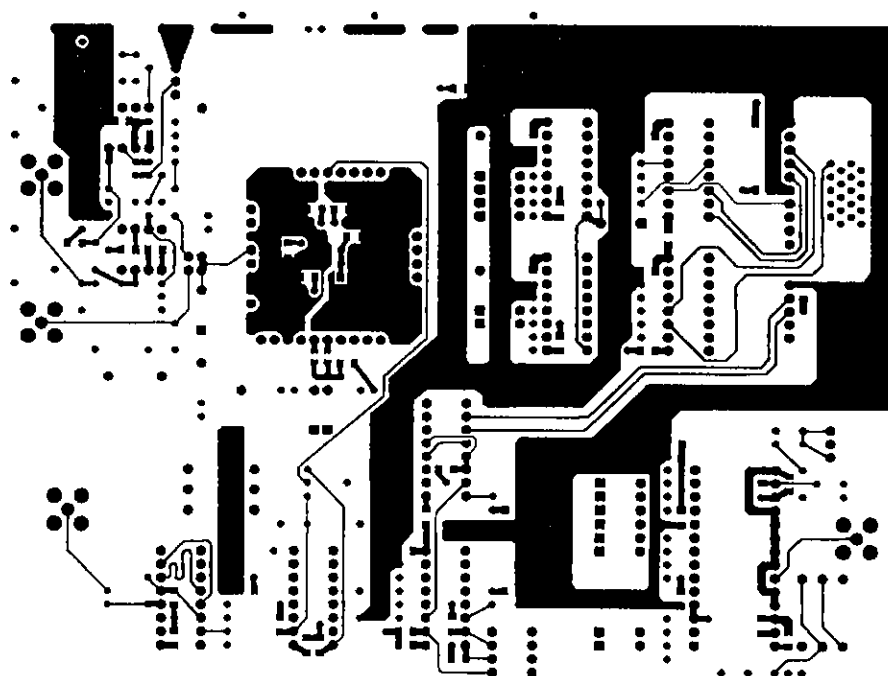
# Parts Layout



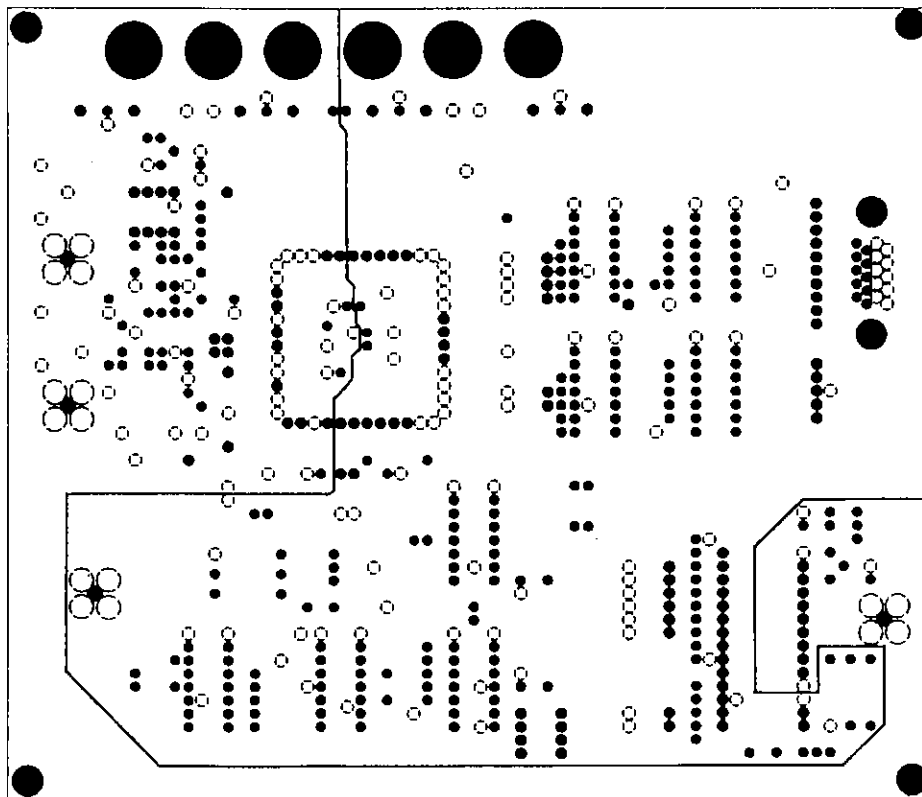
## Printed Pattern



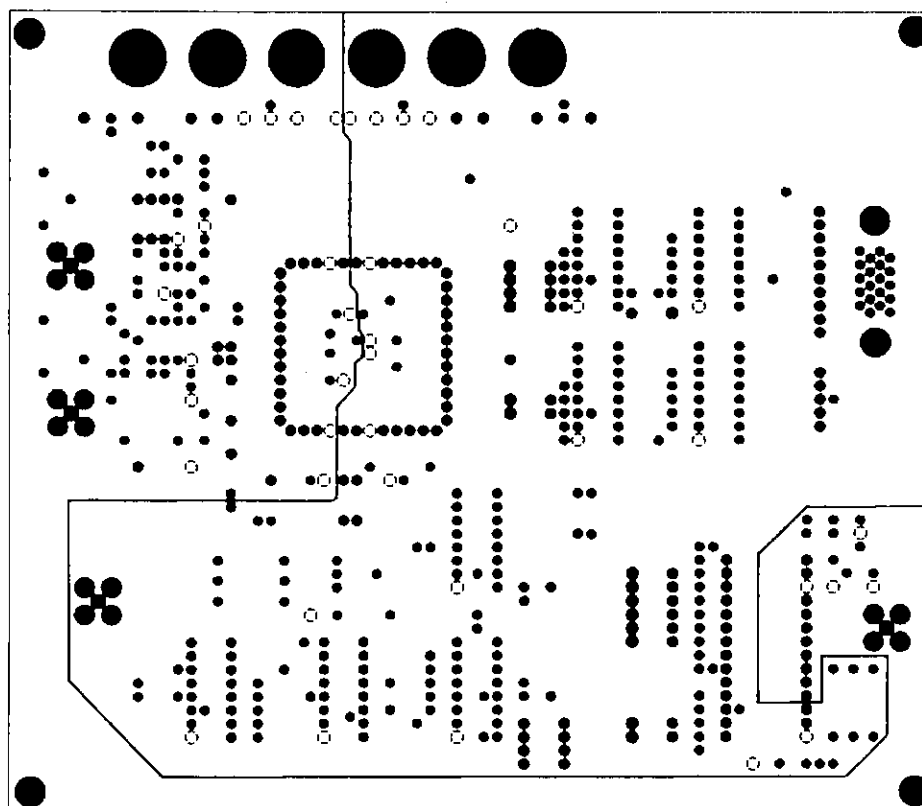
1st layer Component plane (Top View)



4th layer Solder plane (Top View)

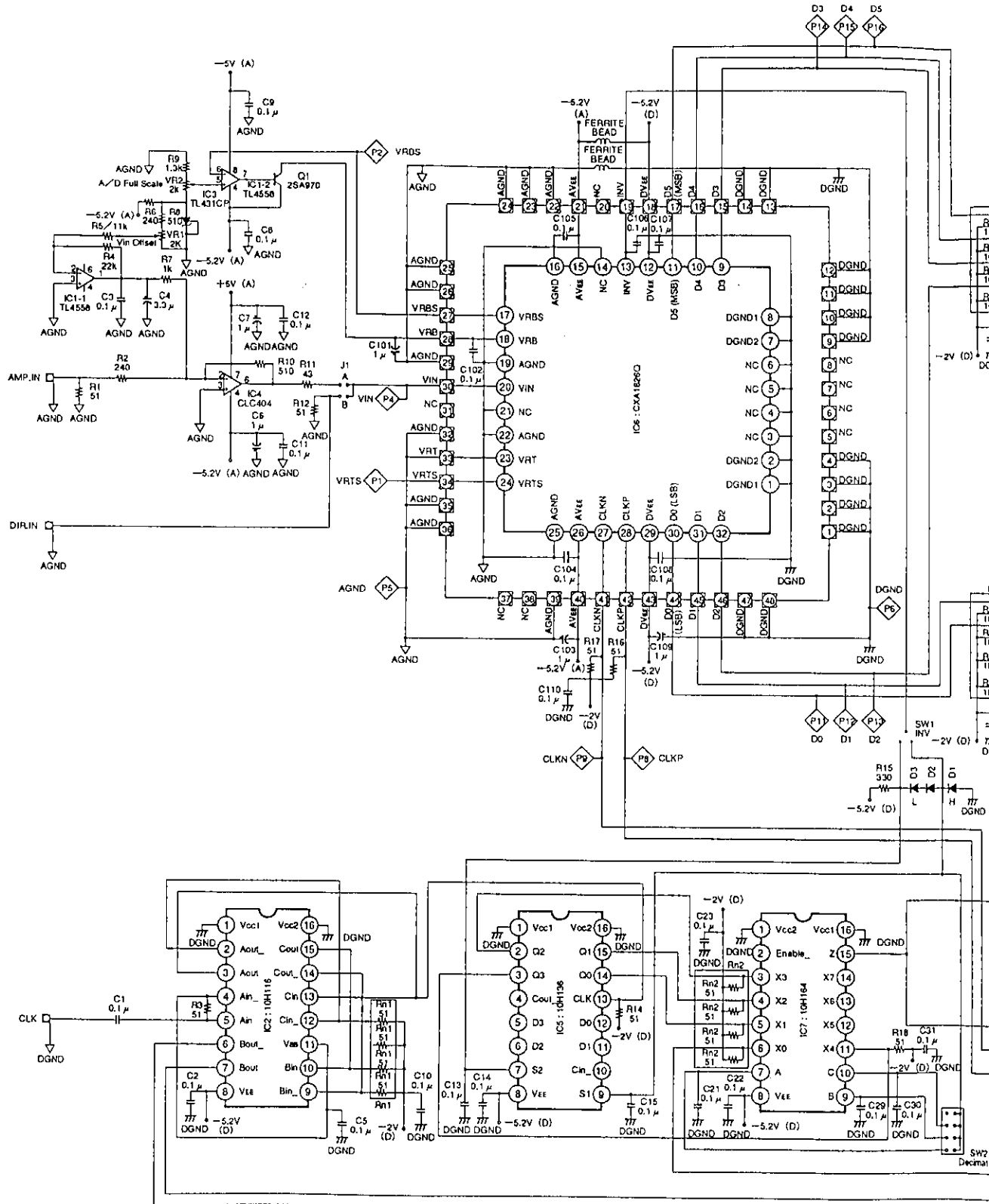


2nd layer GND plane (Top View)

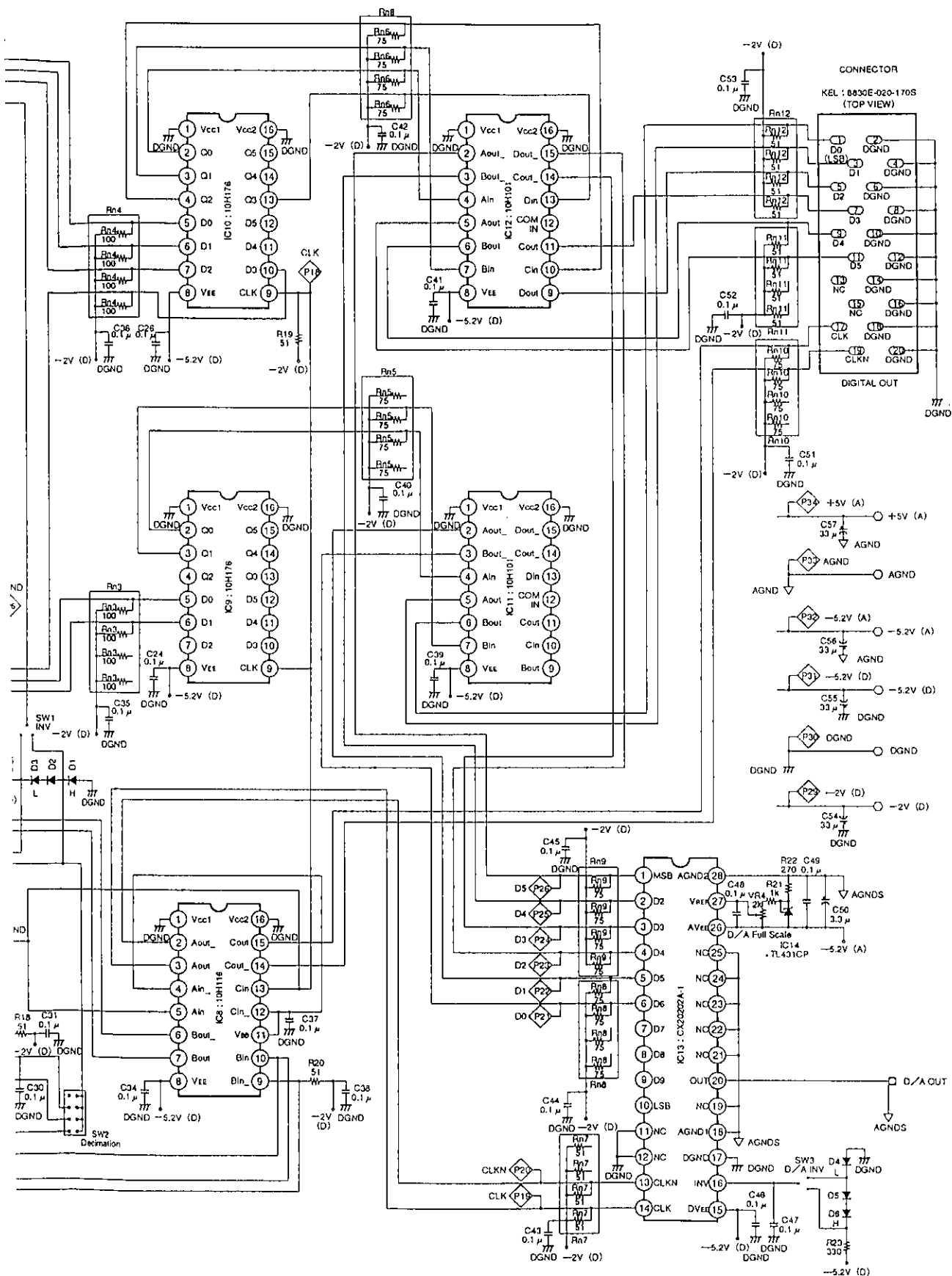


3rd layer Power supply plane (Top View)

# PCB Circuit Diagram

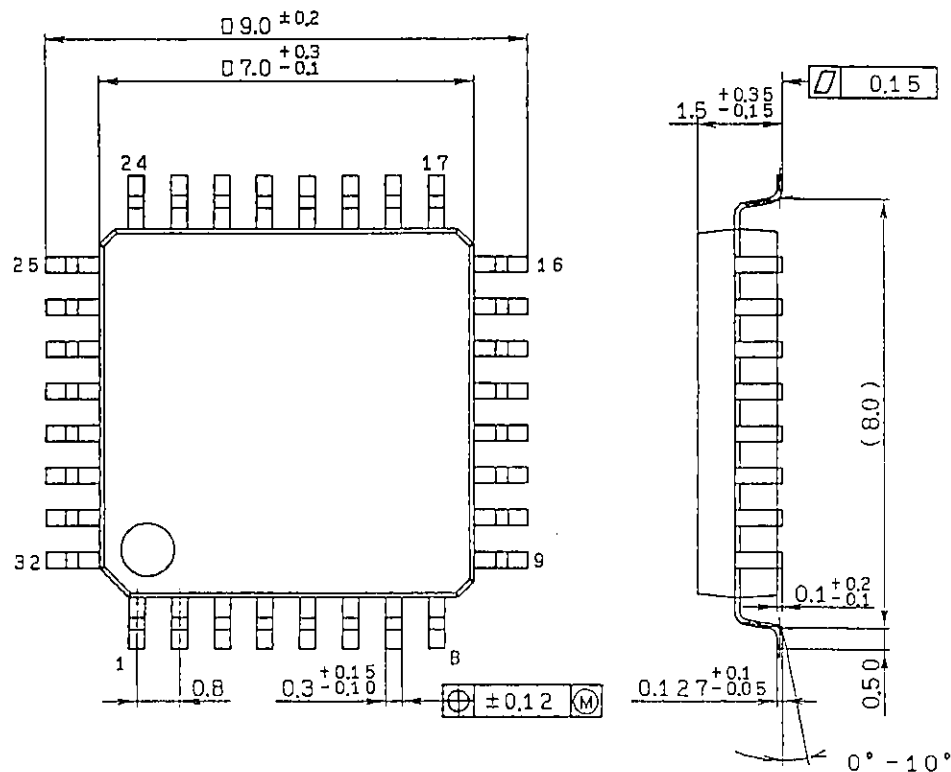


PCB Circuit Diagram shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.



Package Outline      Unit : mm

32pin QFP (Plastic) 0.2g



|            |                  |
|------------|------------------|
| SONY NAME  | QFP-32P-L01      |
| EIAJ NAME  | *QFP032-P-0707-A |
| JEDEC CODE |                  |