SONY

CXA2075M

RGB Encoder

Description

The CXA2075M is an encoder IC that converts analog RGB signals to a composite video signal. This IC has various pulse generators necessary for encoding. Composite video outputs and Y/C outputs for the S terminal are obtained just by inputting composite sync, subcarrier and analog RGB signals.

It is best suited to image processing of personal computers and video games.

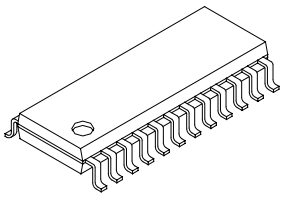
Compared to the CXA1645M, the CXA2075M has superior points as follows:

1. The number of parts reduced (5 parts)
   Clamp capacitor
   Regulator capacitor resistor
   Resistor for filter
2. External parts reduced by the internal TRAP
   (External TRAP can be also selected)
3. Higher band of R, G, B OUT

Features

- Single 5V power supply
- Compatible with both NTSC and PAL systems
- Built-in 75Ω drivers
  (RGB output, composite video output, Y output, C output)
- Both sine wave and pulse can be input as a subcarrier.
- Built-in band-pass filter for the C signal and delay line for the Y signal
- Built-in R-Y and B-Y modulator circuits
- Built-in PAL alternate circuit
- Burst flag generator circuit
- Half H killer circuit

24 pin SOP (Plastic)



Applications

Video games and personal computers

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

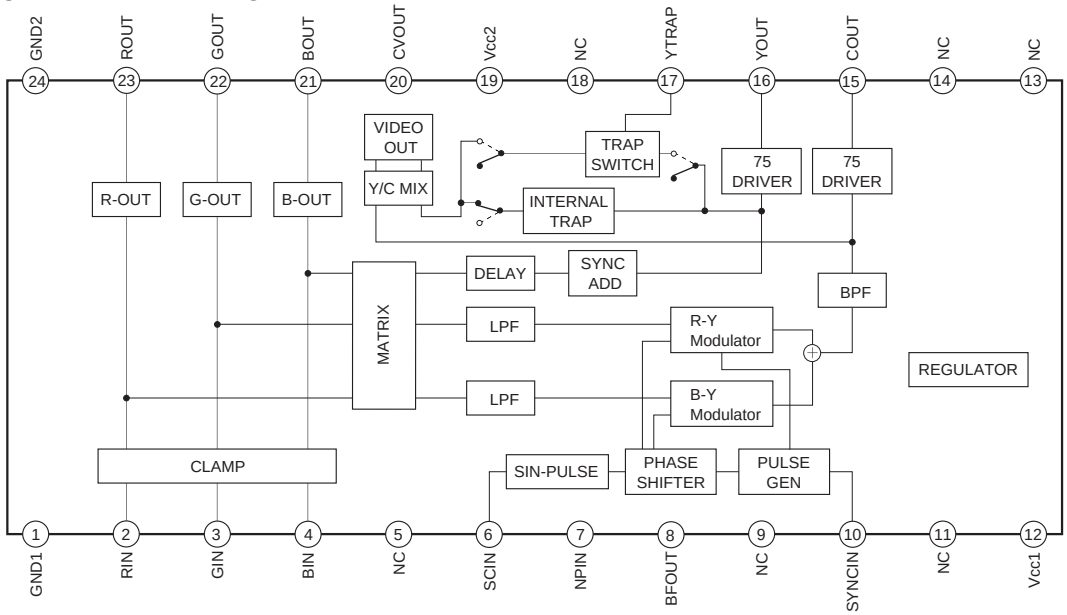
• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	780	mW

- Input pin applied voltage
  RIN, GIN, BIN, SCIN, NPIN, SYNCIN and Vcc pins voltage or below, GND pin voltage or above

Recommended Operating Condition

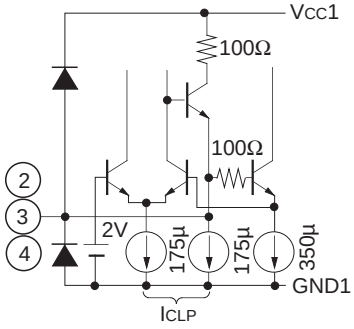
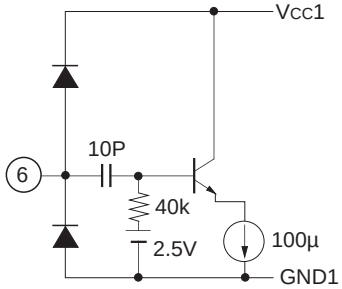
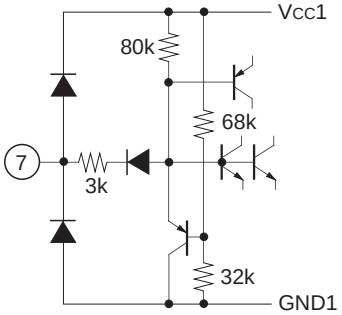
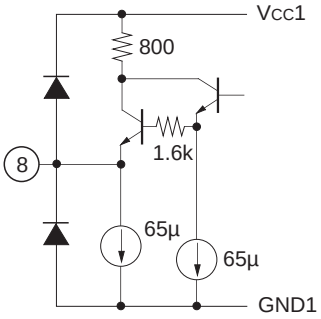
Supply voltage	V_{CC}1, 2	5.0 ± 0.25 V

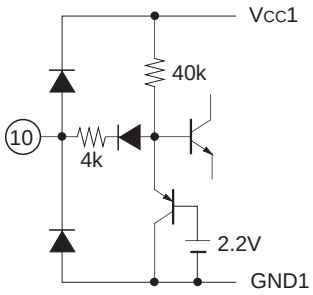
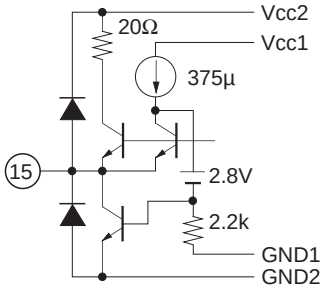
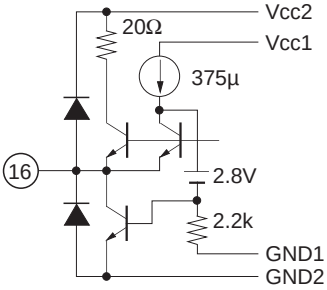
Block Diagram and Pin Configuration

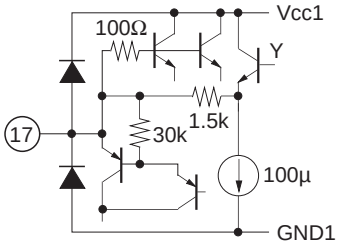
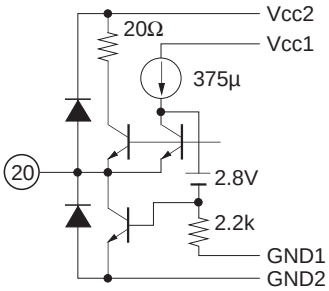
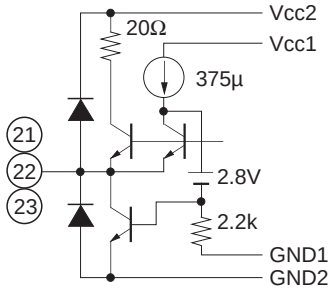


E96X23

Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	GND1	0V	—	Ground for all circuits other than RGB, composite video and Y/C output circuits. The leads to GND2 should be as short and wide as possible.
2 3 4	RIN GIN BIN	Black level when clamped		Analog RGB signal inputs. Input at 100% = 1Vp-p (max.). To minimize clamp error, input at as low impedance as possible. ICLP turns ON only in the burst flag period.
5	NC			NO CONNECTION
6	SCIN	—		Subcarrier input. Input 0.4 to 5.0Vp-p sine wave or pulse. Refer to Notes on Operation, Nos. 2 and 4.
7	NPIN	1.7V when open		Pin for switching between NTSC and PAL modes. NTSC: Vcc, PAL: GND
8	BFOUT	H : 3.6V L : 3.2V		BF pulse monitoring output. Incapable of driving a 75Ω load.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	NC			NO CONNECTION
10	SYNCIN	2.2V		Composite sync signal input. Input TTL-level voltages. L (≤ 0.8V): SYNC period H (≥ 2.0V)
11	NC			NO CONNECTION
12	Vcc1	5.0V	—	Power supply for all circuits other than RGB, composite video and Y/C output circuits. Refer to Notes on Operation, Nos. 3 and 8.
13	NC			NO CONNECTION
14	NC			NO CONNECTION
15	COUT	1.6V		Chroma signal output. Capable of driving a 75Ω load. Refer to Notes on Operation, Nos. 5 and 7.
16	YOUT	Black level 1.35V		Y signal output. Capable of driving a 75Ω load. Refer to Notes on Operation, Nos. 5 and 7.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
17	YTRAP	Black level 2.13V		Pin for reducing cross color caused by the subcarrier frequency component of the Y signal. When the CVOUT pin is in use, connect a capacitor or a capacitor and an inductor in series between YTRAP and GND. Decide capacitance and inductance, giving consideration to cross color and the required resolution. No influence on the YOUT pin. Internal TRAP can be also used. Refer to Notes on Operation, No. 6.
18	NC			NO CONNECTION
19	Vcc2	5.0V	—	Power supply for RGB, composite video and Y/C output circuits. Decouple this pin with a large capacitor of 10µF or above as a high current flows. Refer to Notes on Operation, Nos. 3 and 8.
20	CVOUT	Black level 0.97V		Composite video signal output. Capable of driving a 75Ω load. Refer to Notes on Operation, Nos. 5 and 7.
21 22 23	BOUT GOUT ROUT	Black level 1.2V		Analog RGB signal outputs. Capable of driving a 75Ω load. Refer to Notes on Operation, Nos. 5 and 7.
24	GND2	0V	—	Ground for RGB, composite video and Y/C output circuits. The leads to GND1 should be as short and wide as possible.

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V, See the Electrical Characteristics Measurement Circuit.)

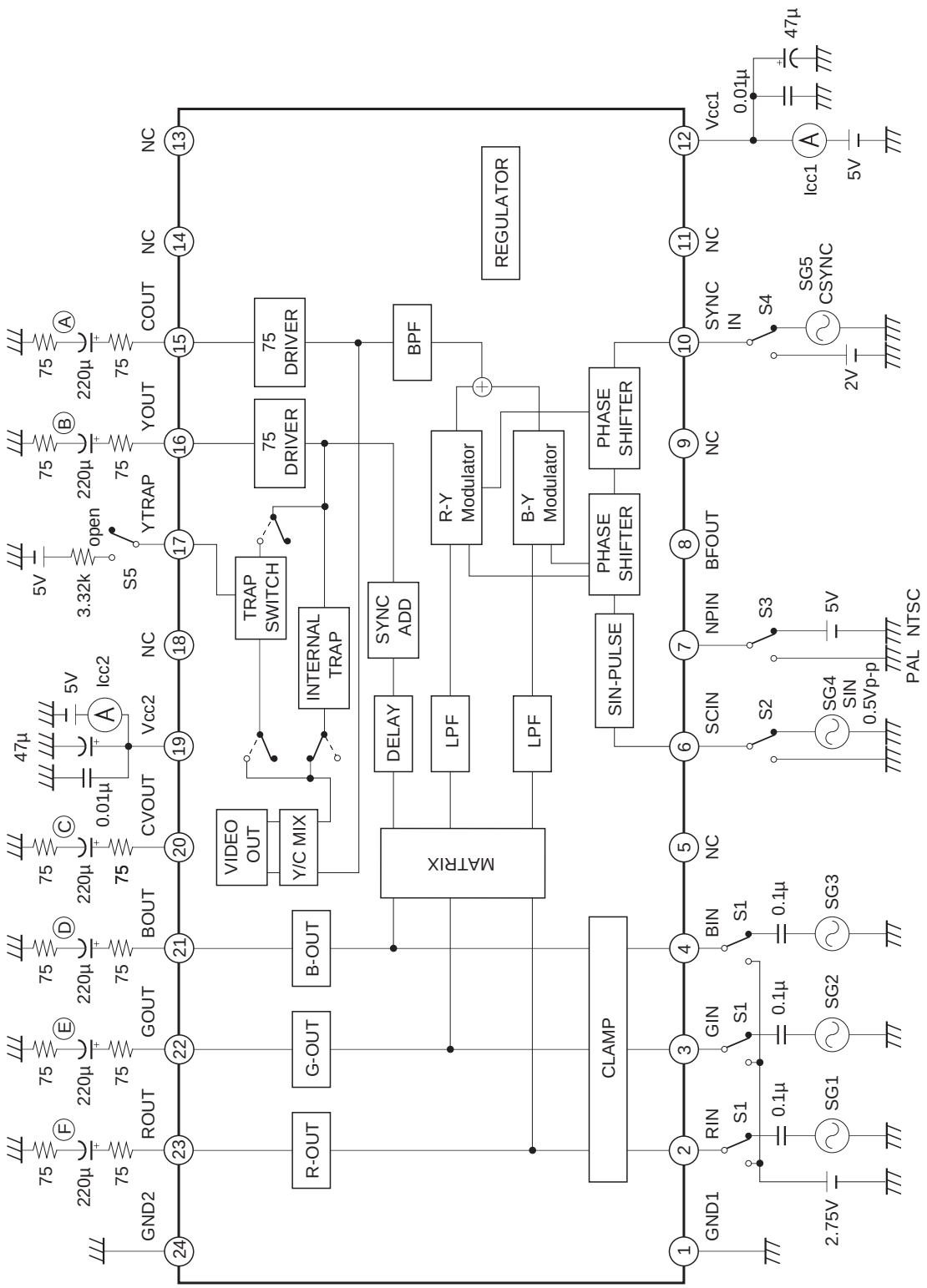
Item	Symbol	S1 RIN GIN BIN	S2 SCIN	S3 NPIN	S4 SYNC IN	Measurement pin	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption 1	$I_{CC}1$	2.75V	SG4	5V	SG5	$I_{CC}1$	No input signal, SG5: CSYNC TTL level, SG4: SIN wave 3.58MHz 0.5Vp-p Fig. 1	—	67	—	mA
Current consumption 2	$I_{CC}2$					$I_{CC}2$		—	40	—	
(R, G, BOUT)											
RGB output voltage	V_O (R)	SG1			2V	D	SG1 to SG3: DC direct coupling 3.2V_{DC}, 1.0Vp-p f = 200kHz Pin 9 = Clamp voltage* Fig. 2	0.64	0.69	0.72	V
	V_O (G)	SG2				E					
	V_O (B)	SG3				F					
RGB output frequency characteristics	f_C (R)	SG1			2V	D	SG1 to SG3: DC direct coupling 3.2V_{DC}, 1.0Vp-p f = 27MHz/200kHz Pin 9 = Clamp voltage Fig. 3	–5	–3.2	—	dB
	f_C (G)	SG2				E		–5	–3.4	—	dB
	f_C (B)	SG3				F		–5	–3.8	—	dB
(YOUT)											
Output sync level	V_O (YS1/2)	SG1 to SG3	0V	5V	SG5	B	SG1 to SG3: 100% color bar input, 1.0Vp-p (Max.) SG5: CSYNC TTL level Fig. 4	0.24	0.27	0.31	Vp-p
R100%: Y level	V_O (YR1/2)							0.19	0.215	0.24	
G100%: Y level	V_O (YG1/2)							0.38	0.405	0.43	
B100%: Y level	V_O (YB1/2)							0.06	0.076	0.09	
White 100%: Y level	V_O (YW1/2)							0.63	0.682	0.79	
Output frequency characteristics	f_C (Y1/2)	SG1 to SG3	0V	5V	2V		SG1 to SG3: DC direct coupling 3.2V_{DC}, 1.0Vp-p f = 5MHz/200kHz Pin 9 = Clamp voltage	–1	–0.13	—	dB
(CVOUT)											
Output sync level	V_O (YS1/2)	SG1 to SG3	0V	5V	SG5	C	SG1 to SG3: 100% color bar input, 1.0Vp-p (Max.) SG5: CSYNC TTL level Fig. 4	0.22	0.24	0.27	Vp-p
R100%: Y level	V_O (YR1/2)							0.18	0.208	0.23	V
G100%: Y level	V_O (YG1/2)							0.35	0.376	0.41	V
B100%: Y level	V_O (YB1/2)							0.055	0.071	0.085	V
White 100%: Y level	V_O (YW1/2)							0.61	0.66	0.75	V
Output frequency characteristics	f_C (Y1/2)	SG1 to SG3	0V	5V	2V		SG1 to SG3: DC direct coupling 3.2V_{DC}, 1.0Vp-p f = 5MHz/200kHz Pin 9 = Clamp voltage	–3.3	–1.53	—	dB

* Clamp voltage: voltage appearing at Pin 9 when CSYNC is input.

Item	Symbol	S1	S2	S3	S4	Measure-ment pin	Measurement conditions	Min.	Typ.	Max.	Unit
		RIN GIN BIN	SCIN	NPIN	SYNC IN						
(COUT)											
Burst level	VO (BN1/2)	SG1 to SG3	SG4	5V	SG5	A	SG1 to SG3: 100% color bar input, 1.0Vp-p (Max.) SG4: SIN wave, 3.58MHz 0.5Vp-p SG5: CSYNC TTL level Fig. 5	0.24	0.282	0.34	Vp-p
R chroma ratio	R/BN1/2							2.8	3.17	3.6	
R phase	θR1/2							99	104	111	deg
G chroma ratio	G/BN1/2							2.7	3.06	3.8	
G phase	θG1/2							232	238	246	deg
B chroma ratio	B/BN1/2							1.8	2.1	2.35	
B phase	θB1/2							341	348	356	deg
Burst width	tW (B) 1/2							2.35	2.6	2.8	µs
Burst position	tD (B) 1/2							0.35	0.68	0.95	µs
Carrier leak	VL1/2	SG1 to SG3	SG4	5V	SG5		SG1 to SG3: No signal, SG4: SIN wave, 3.58MHz 0.5Vp-p SG5: CSYNC TTL level 3.58MHz component measured. Fig. 6	—	6	29	mVp-p

Item	Symbol	S1 RIN GIN BIN	S2 SCIN	S3 NPIN	S4 SYNC IN	Measure-ment pin	Measurement conditions	Min.	Typ.	Max.	Unit
(CVOUT)											
Burst level	V_O (BN1/2)	SG1 to SG3	SG4	5V	SG5	C	SG1 to SG3: 100% color bar input, 1.0Vp-p (Max.) SG4: SIN wave, 3.58MHz 0.5Vp-p SG5: CSYNC TTL level Fig. 5	0.22	0.264	0.32	Vp-p
R chroma ratio	R/BN1/2							2.95	3.3	3.7	
R phase	θR1/2							99	105	111	deg
G chroma ratio	G/BN1/2							2.9	3.23	3.5	
G phase	θG1/2							233	239	247	deg
B chroma ratio	B/BN1/2							1.8	2.02	2.3	
B phase	θB1/2							342	349	357	deg
Burst width	t_W (B) 1/2							2.35	2.52	2.8	µs
Burst position	t_D (B) 1/2							0.35	0.66	0.95	µs
Carrier leak	VL1/2	SG1 to SG3	SG4	5V	SG5		SG1 to SG3: No signal, SG4: SIN wave, 3.58MHz 0.5Vp-p SG5: CSYNC TTL level 3.58MHz component measured. Fig. 6	—	6	29	mVp-p
PAL burst level ratio	K (BP1/2)	SG1 to SG3	SG4	GND	SG5		SG1 to SG3: No signal, SG4: SIN wave, 4.43MHz 0.5Vp-p SG5: CSYNC TTL level Fig. 6	0.9	1.0	1.1	
PAL burst phase	θPAL1/2							129	138	146	deg
	θXPAL1/2							214	221	228	deg
Internal TRAP attenuation frequency	fTRAP	SG1 to SG3	0V	5V	2V	C	SG1 to SG3: DC direct coupling 3.2V_{DC} 1.0Vp-p f = 3.58MHz/200kHz YTRAP = 3.32k	–30	–21.6	–4	dB

Electrical Characteristics Measurement Circuit



Measuring Signals and Output Waveforms

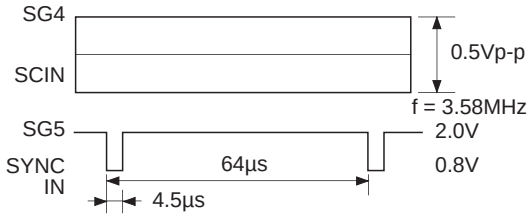


Fig. 1

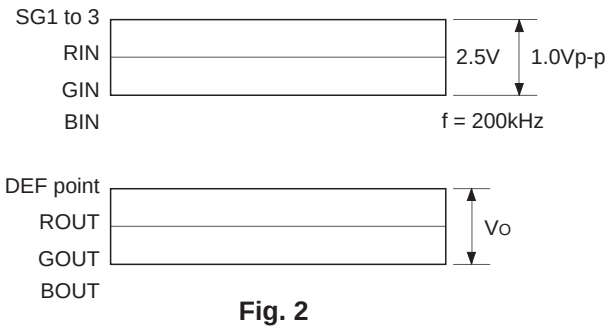


Fig. 2

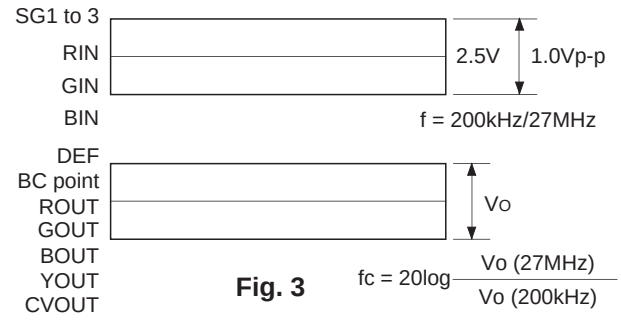


Fig. 3

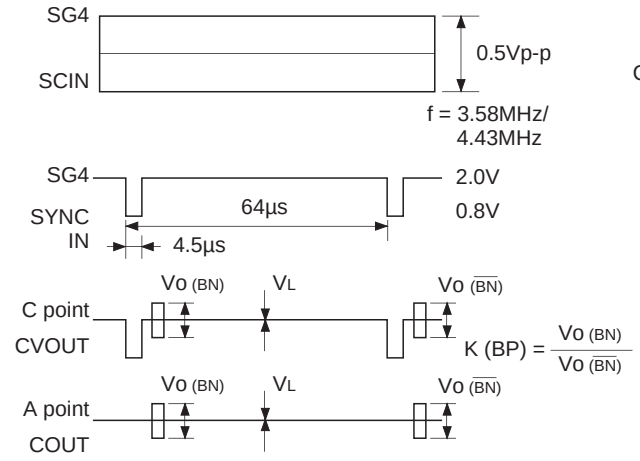


Fig. 6

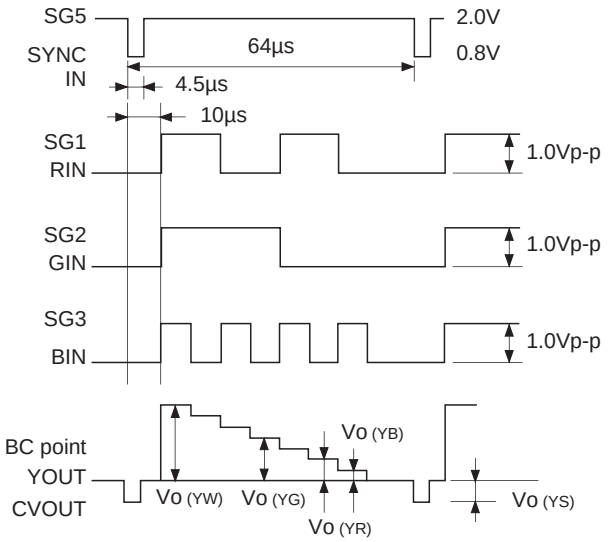


Fig. 4

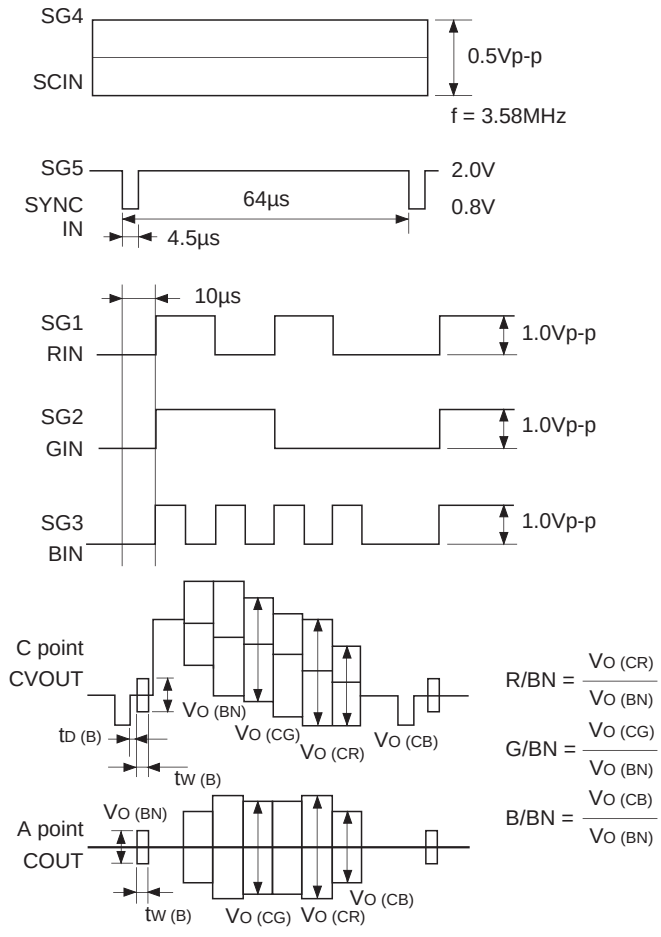
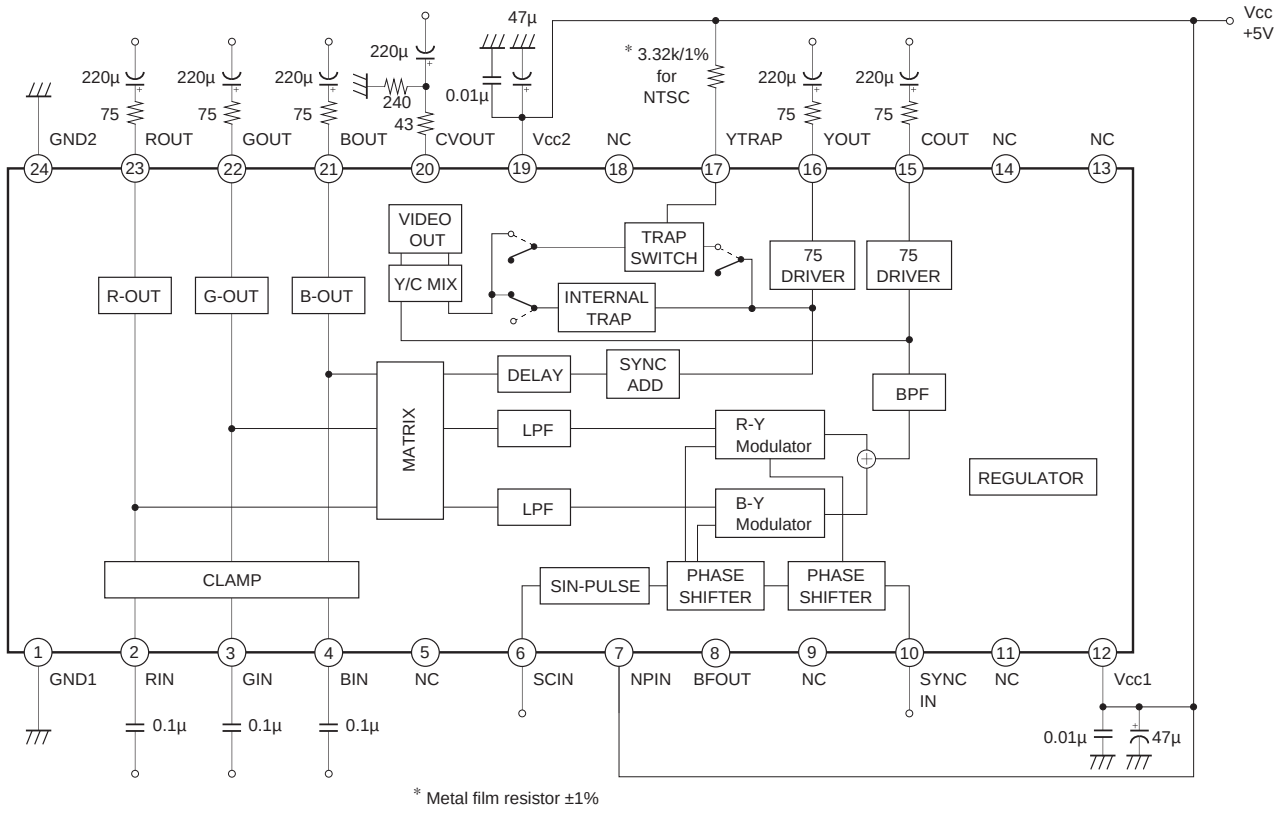
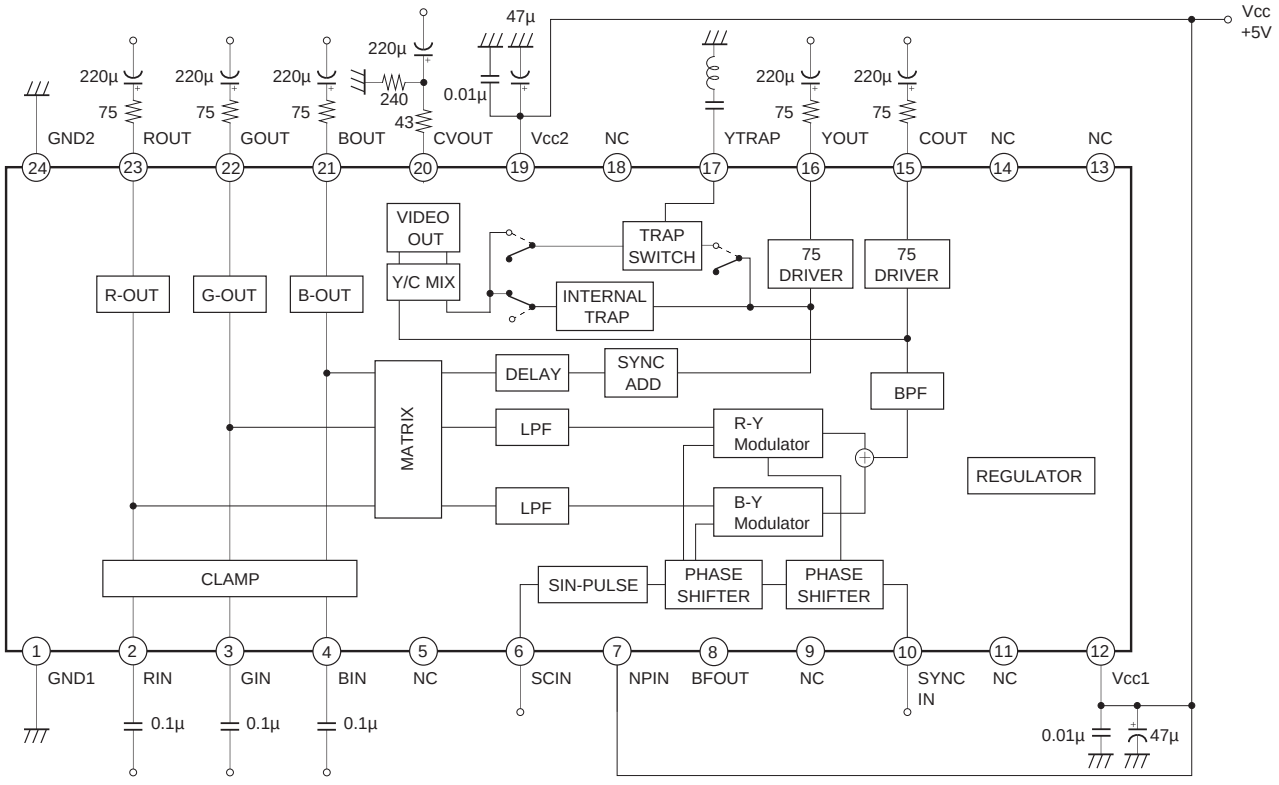


Fig. 5

Application Circuit (NTSC internal TRAP mode)

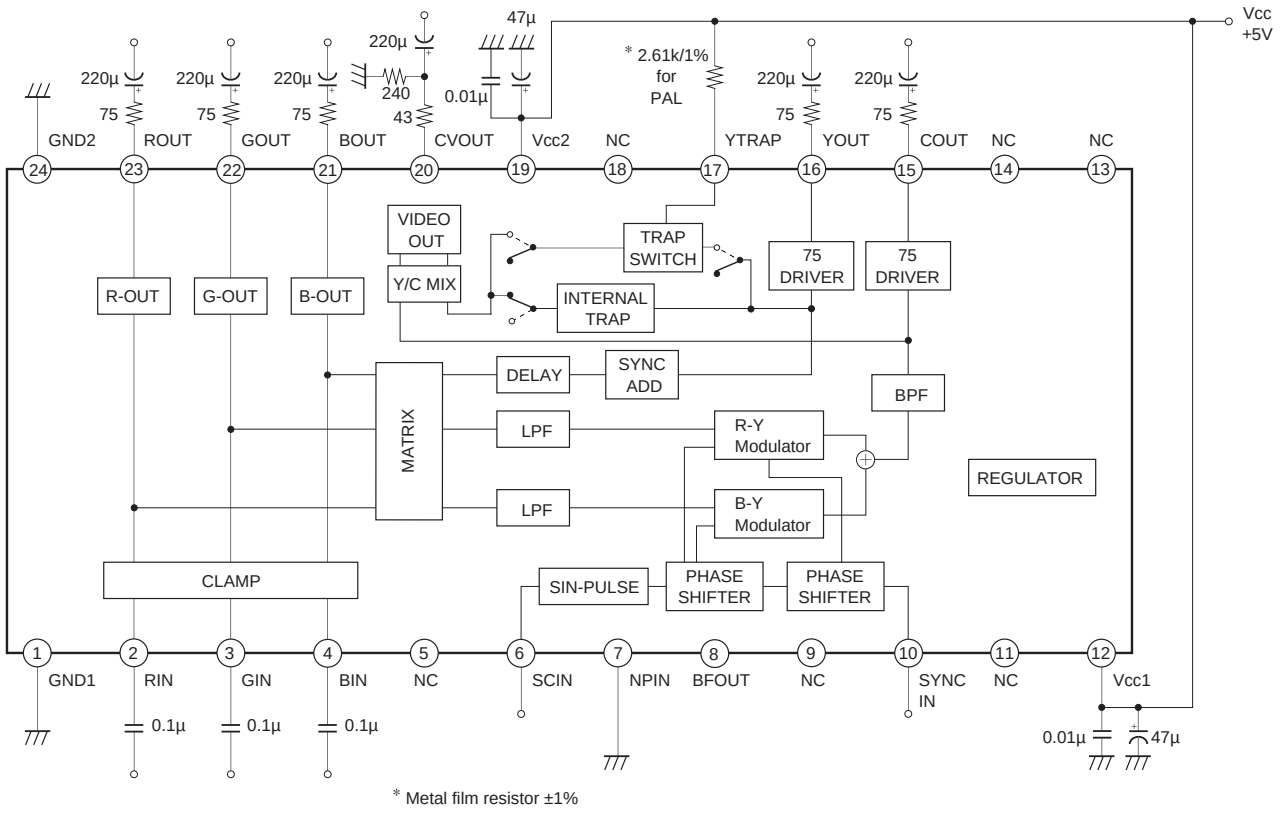


Application Circuit (NTSC external TRAP mode)

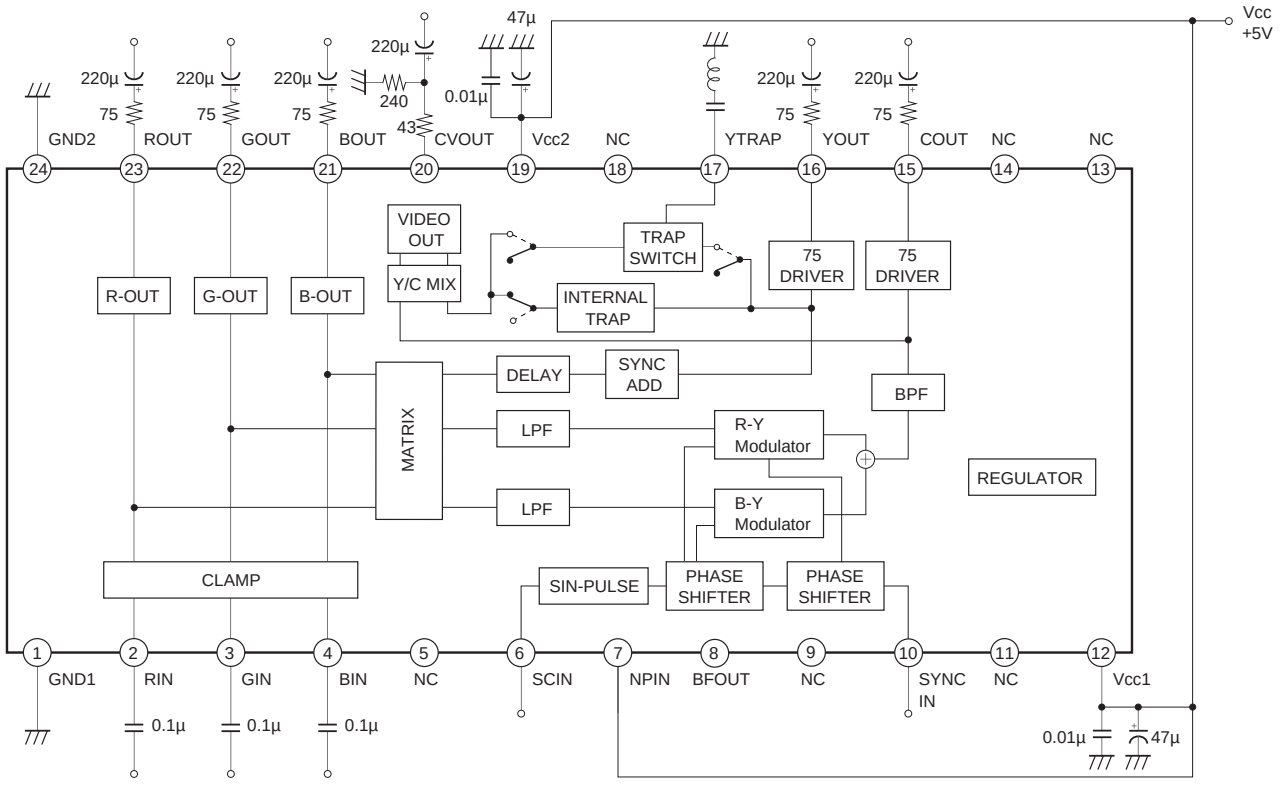


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (PAL internal TRAP mode)



Application Circuit (PAL external TRAP mode)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

Analog RGB signals input from Pins 2, 3 and 4 are clamped in the clamping circuit and output from Pins 23, 22 and 21, respectively.

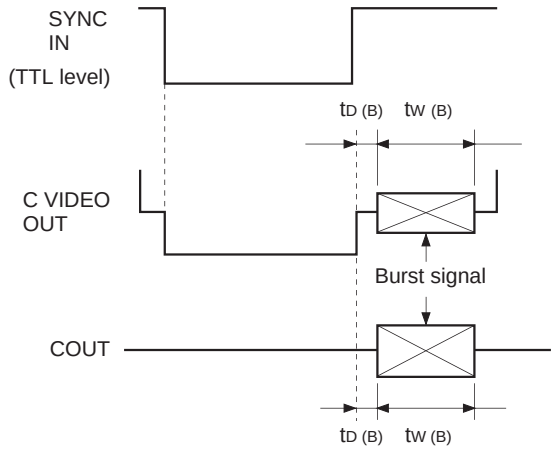
The matrix circuit performs operations on each input signal, generating luminance signal Y and color difference signals R-Y and B-Y. The Y signal enters the delay line to adjust delay time with the chroma signal C. Then, after addition of the CSYNC signal input from Pin 10, the Y signal is output from Pin 16.

A subcarrier input from Pin 6 is input to the phase shifter, where its phase is sfited 90°. Then, the subcarrier is input to the modulators and modulated by the R-Y signal and the B-Y signal. The modulated subcarriers are mixed, sent to the band-pass filter to eliminate higher harmonic components and finally output from Pin 15 as the C signal. At the same time, Y and C signals are mixed and output from Pin 20 as the composite video signal.

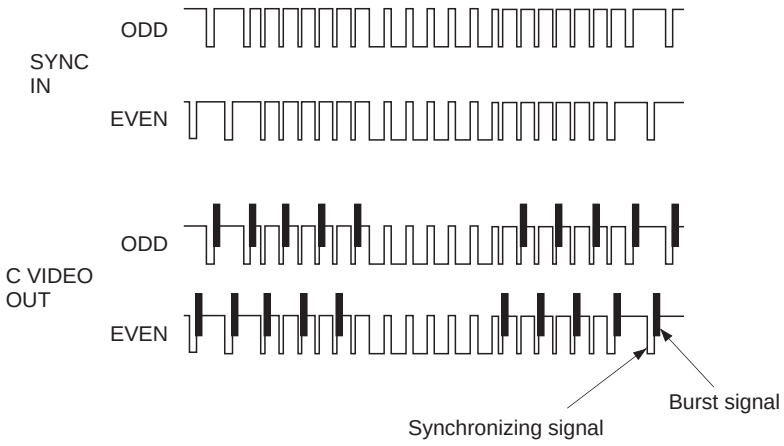
Burst Signal

The CXA2075M generates burst signals at the timing shown below according to the composite sync signal input.

H synchronization



V synchronization



Notes on Operation

Be careful of the following when using the CXA2075M.

1. Be sure that analog RGB signals are input at 1.0Vp-p maximum and have low enough impedance. High impedance may affect color saturation, hue, etc. Inputting RGB signals in excess of 1.3Vp-p may disable the clamp operation.

2. The SC input (Pin 6) can be either a sine wave or a pulse in the range from 0.4 to 5.0Vp-p.
   However, when a pulse is input, its phase may be shifted several degrees from that of the sine wave input. In the IC, the SC input is biased to 1/2 V_{CC}. Accordingly, when a 5.0Vp-p pulse is input and the duty factor deviates from 50%, High- and Low-level pulse voltages may exceed V_{CC} and GND in the IC, which causes subcarrier distortion. In such a case, be very careful that the duty factor keeps to 50%.

3. When designing a printed circuit board pattern, pay careful attention to the routing of the V_{CC} and GND leads. To decouple the V_{CC} pin, use tantalum, ceramic or other capacitors with good frequency characteristics. Ground the capacitors by connections shown below as closely to each IC pin as possible. Try to design the leads as short and wide as possible.

V_{CC}1... GND1
V_{CC}2... GND2

   Design the pattern so that V_{CC} is connected to GND via a capacitor at the shortest distance.

4. SC and SYNC input pulses
   Attach a resistor and a capacitor to eliminate high-frequency components of SC (Fig. A) and SYNC (Fig. B) before input.

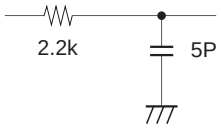


Fig. A

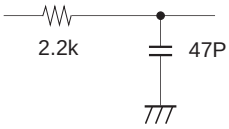
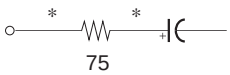


Fig. B

   Be careful not to input pulses containing high-frequency components. Otherwise, high-frequency components may flow into V_{CC}, GND and peripheral parts, resulting in malfunctions.

5. Connecting an external resistor to the 75Ω driver output pin
   A capacitance of several dozen picofarads at each pin may start oscillation. To prevent oscillation, design the pattern so that a 75Ω resistor is mounted near the pin (see Fig. C).



* Make these leads short.

Fig. C

   When any of the 75Ω driver output pins is not in use, leave it unconnected and design the pattern so that no parasitic capacitance is generated on the printed circuit board.

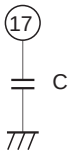
6. YTRAP pin (Pin 17)

There are the following three means of reducing cross color generated by subcarrier frequency components contained in the Y signal.

(1) Install a capacitor of 30 to 68pF between YTRAP and GND. Decide the capacitance by conducting image evaluation, etc., giving consideration to both cross color and resolution.

Relations between capacitance and picture quality are as follows:

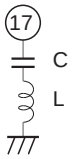
Capacitance	30pF ⟷ 68pF
Cross color Resolution	Large ⟷ Small High ⟷ Low



(2) Connect a capacitor C and an inductor L in series between YTRAP and GND. When the subcarrier frequency is f_0, the values C and L are determined by the equation $f_0 = \frac{1}{2\pi\sqrt{LC}}$. Decide the values in image evaluation, etc., giving consideration to both cross color and resolution.

Relations between inductor values and picture quality are as follows:

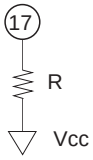
Inductor value	Small ⟷ Large
Cross color Resolution	Large ⟷ Small High ⟷ Low



For instance, L = 68µH and C = 28pF are recommended for NTSC. It is necessary to select an inductor L with a sufficiently small DC resistance. Method (2) is more useful for achieving a higher resoluation than method (1). When an even higher resolution is necessary, use of the S terminal (YOUT and COUT) is recommended.

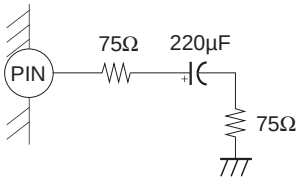
(3) TRAP built in the IC can be used. Connect a resistor which determines to between YTRAP (Pin 17) and Vcc. Refer to Application Circuit. Be very careful of frequency characteristics and picture quality, and then use them.

NTSC mode R = 3.32kΩ
PAL mode R = 2.61kΩ



7. Driving COUT (Pin 15), YOUT (Pin 16), CVOUT (Pin 20), and B.G.R OUT (Pins 21, 22 and 23) outputs

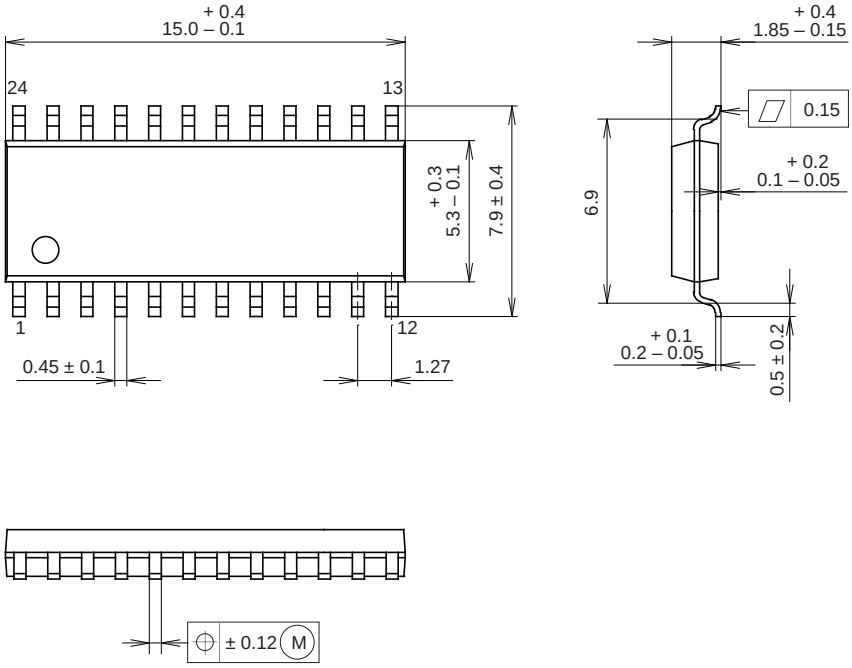
In Pin Description, "Capable of driving a 75Ω load" means that the pin can drive a capacitor +75Ω +75Ω load shown in the figure below. In other words, the pin is capable of driving a 150Ω load in AC.



8. This IC employs a number of 75Ω driver pins, so oscillation is likely to occur when measures described in Nos. 3 and 5 are not taken thoroughly. Be very careful of oscillation in printed circuit board design and carry out thorough investigations in the actual driving condition.

Package Outline Unit: mm

24PIN SOP (PLASTIC)



SONY CODE	SOP-24P-L01
EIAJ CODE	∗SOP024-P-0300-A
JEDEC CODE	————

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g