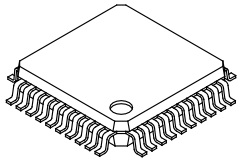
SONY

CXB1575AQ

155Mbps Clock & Data Recovery with High Sensitivity Limiting Amplifier

40 pin QFP (Plastic)



Description

The CXB1575AQ achieves 3R optical-fiber communication receiver functions (Reshaping and Regenerating and Retiming) on a single chip. This IC also equipped with the signal interruption alarm output, which is used to discriminate the existence of data input.

Features

- Auto-offset canceler circuit
- Signal interruption alarm output
- No reference clock required
- Single 3.3V power supply

Applications

- SONET/SDH: 155.52Mbps
- ATM: 155.52Mbps

Absolute Maximum Ratings

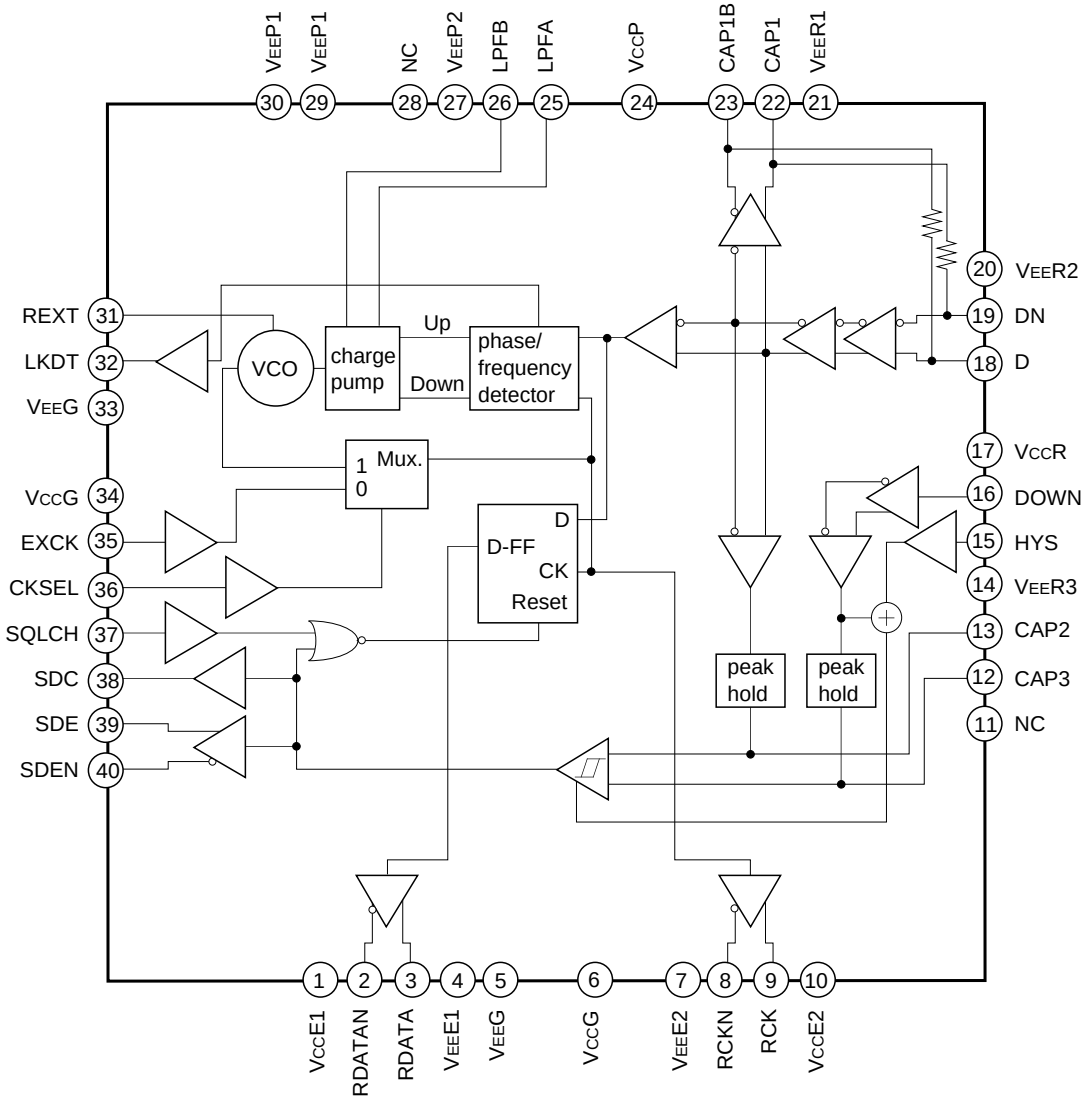
• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +5.0	V
• Storage temperature	Tstg	–65 to +150	°C
• Input voltage difference: $\lvert V_D - V_{DN} \rvert$	Vdif	0 to 2.5	V
• TTL input voltage	VinT	–0.5 to 5.5	V
• Output current (Continuous)	I_O	0 to 50	mA
(Surge)		0 to 100	mA

Recommended Operating Conditions

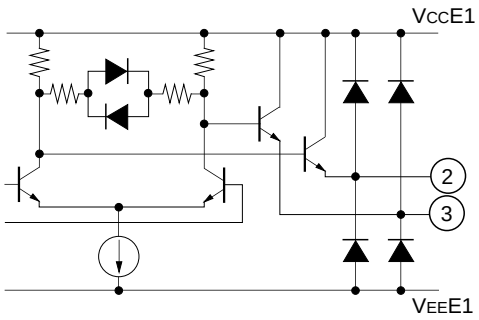
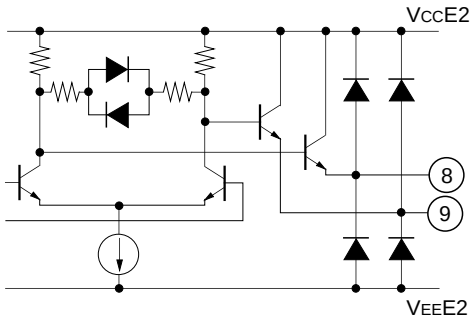
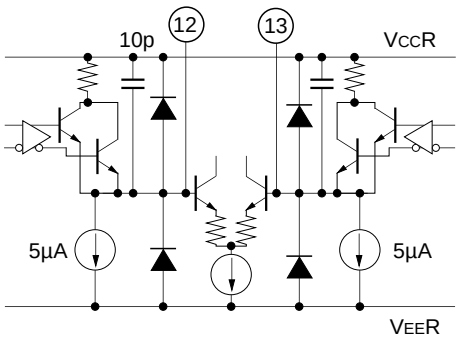
• Supply voltage	$V_{CC} - V_{EE}$	3.069 to 3.465	V
• Termination voltage (for RCK/RDATA)	$V_{CC} - V_{T1}$	1.8 to 2.2	V
• Termination voltage (for SDE)	V_{T2}	V_{EE}	V
• Termination resistance (for RCK/RDATA)	R_{T1}	46 to 56	Ω
• Termination resistance (for SDE)	R_{T2}	460 to 560	Ω
• Operating temperature	Ta	–40 to +85	°C

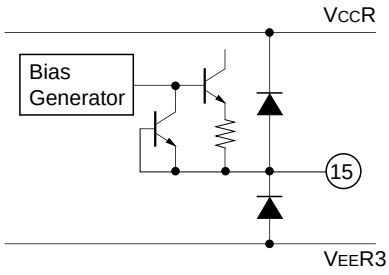
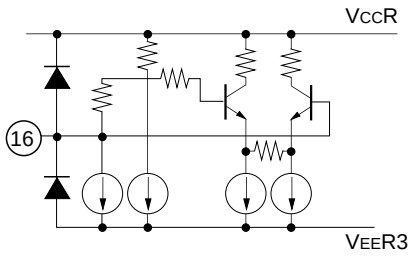
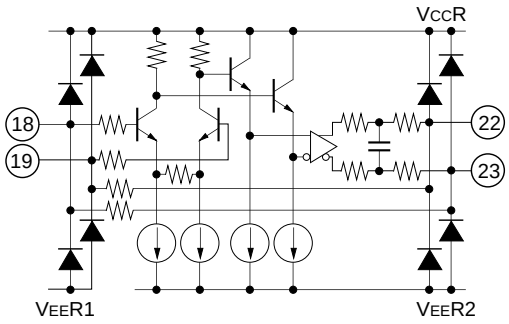
E97Y13-PS

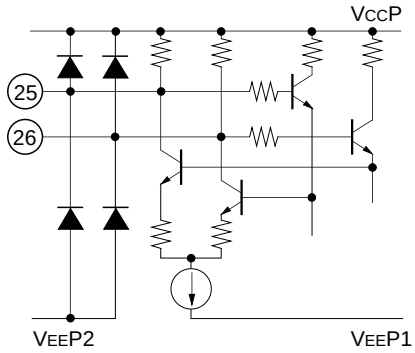
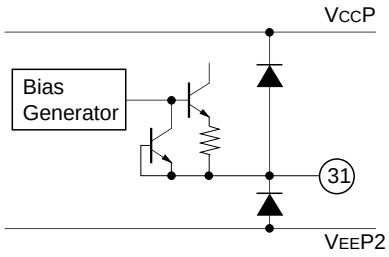
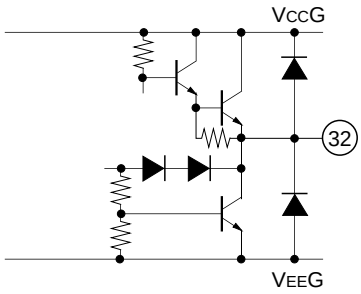
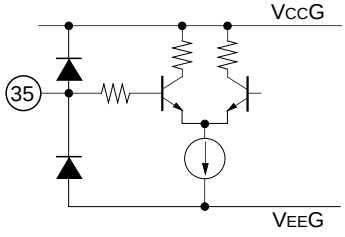
Block Diagram and Pad Configuration

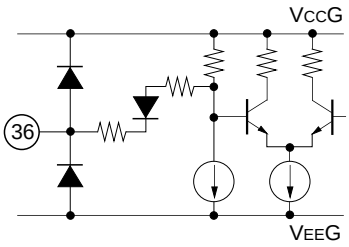
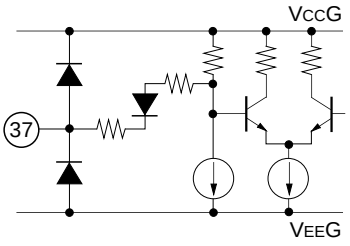
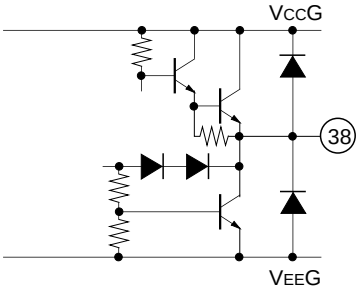
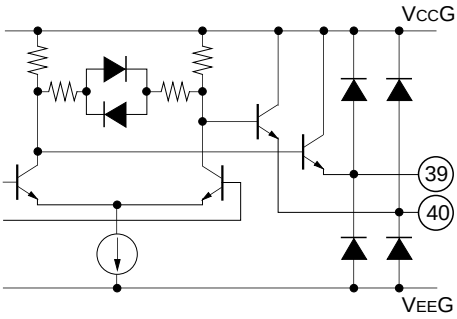


Pin Description

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
1	$V_{CC}E1$	3.3			Positive supply for RDATA/RDATAN output circuits.
2	RDATAN		1.6 to 2.4		Retimed data outputs.
3	RDATA		1.6 to 2.4		
4	$V_{EE}E1$	0			Ground for RDATA/RDATAN output circuits.
5, 33	$V_{EE}G$	0			Ground for digital circuits.
6, 34	$V_{CC}G$	3.3			Positive supply for digital circuits.
7	$V_{EE}E2$	0			Ground for RCK/RCKN outputs circuits.
8	RCKN		1.6 to 2.4		Recovered clock outputs.
9	RCK		1.6 to 2.4		
10	$V_{CC}E2$	3.3			Positive supply for RCK/RCKN output circuits.
11	NC				No connect
12	CAP3	2			Connect a peak hold capacitor for signal detector. Typically 470pF.
13	CAP2	2			

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
14	$V_{EE}R3$	0			Ground for signal detector.
15	HYS	0.2			Connect to $V_{EE}R3$ through an external resistor to determine signal detect hysteresis width (ΔP). When connect to $V_{EE}R3$ directly; $\Delta P \approx 6dB$ (Typ.) When connected 8.2kΩ to $V_{EE}R3$; $\Delta P \approx 3dB$ (Typ.)
16	DOWN	3			Connect to $V_{CC}R$ through an external resistor to decrease signal detect level (SDL). When open, SDL sets to 18mVp-p. (single-ended)
17	$V_{CC}R$	3.3			Positive supply for signal detector.
18	D				Serial data stream inputs.
19	DN				
22	CAP1	2.2			Connect an external capacitor, which determines low cut-off frequency for DC feedback loop. Typically 0.22µF.
23	CAP1B	2.2			
20	$V_{EE}R2$	0			Ground for post amplifier.
21	$V_{EE}R1$	0			Ground for post amplifier. Both $V_{EE}R1$ and $V_{EE}R2$ must be grounded.
24	$V_{CC}P$	3.3			Positive supply for PLL circuits.

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
25	LPFA	3.1			Connect an external loop filter capacitor. Typically 0.68µF (155.52Mbps).
26	LPFB	3.1			
27	VEEP2	0			Ground for PLL circuits.
28	NC				No connect
29, 30	VEEP1	0			Ground for PLL circuits. Both VEEP1 and VEEP2 must be grounded.
31	REXT	0.4			Connect to VEEP1 through an external resistor to determine VCO frequency. Typically 1.8kΩ.
32	LKDT		0.2 to 3.1		Lock detector (TTL). Driven low, while synchronization is lost.
35	EXCK	1.3			External clock input (ECL). For testing only. Normally, left open.

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
36	CKSEL	3.3			Clock selector (TTL). When low, EXCK is active instead of VCO output. Normally, left open.
37	SQLCH	3.3			TTL input. When Low, RCK and RDATA are fixed Low, in case of data loss. When high, RCK outputs VCO free-run frequency, in case of data loss.
38	SDC		0.2 to 3.1		Signal detect output (TTL). Driven low, while input serial data is lost.
39	SDE		1.6 to 2.4		Signal detect outputs (ECL). SDE is driven low, while input serial data is lost.
40	SDEN		1.6 to 2.4		

Electrical Characteristics

• **DC characteristics** (V_{CC} = +3.069 to +3.465V, V_{EE} = GND, Ta = –40°C to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current	I_{CC}	All outputs open		70	100	mA
TTL input High voltage	V_{IHT}		2		3.465	V
TTL input Low voltage	V_{ILT}		0		0.8	V
RDATA/RCK output High voltage	$V_{OH}1$*1	51Ω to V_{CC} – 2V	V_{CC} – 1.1		V_{CC} – 0.83	V
RDATA/RCK output Low voltage	$V_{OL}1$*1	51Ω to V_{CC} – 2V	V_{CC} – 1.88		V_{CC} – 1.55	V
SDE output High voltage	$V_{OH}2$*1	510Ω to V_{EE}	V_{CC} – 1.1		V_{CC} – 0.83	V
SDE output Low voltage	$V_{OL}2$*1	510Ω to V_{EE}	V_{CC} – 1.88		V_{CC} – 1.55	V
TTL output High voltage	V_{OHT}	I_{OH} = –0.2mA	2.4			V
TTL output Low voltage	V_{OLT}	I_{OL} = 2.1mA			0.5	V
Maximum input voltage amplitude	Vmax		1600			mV
D/DB input resistance	Rin		2250	3000	3750	Ω

*1 Ta = 0°C to +85°C

• **AC characteristics** (V_{CC} = +3.069 to +3.465V, V_{EE} = GND, Ta = –40°C to +85°C)

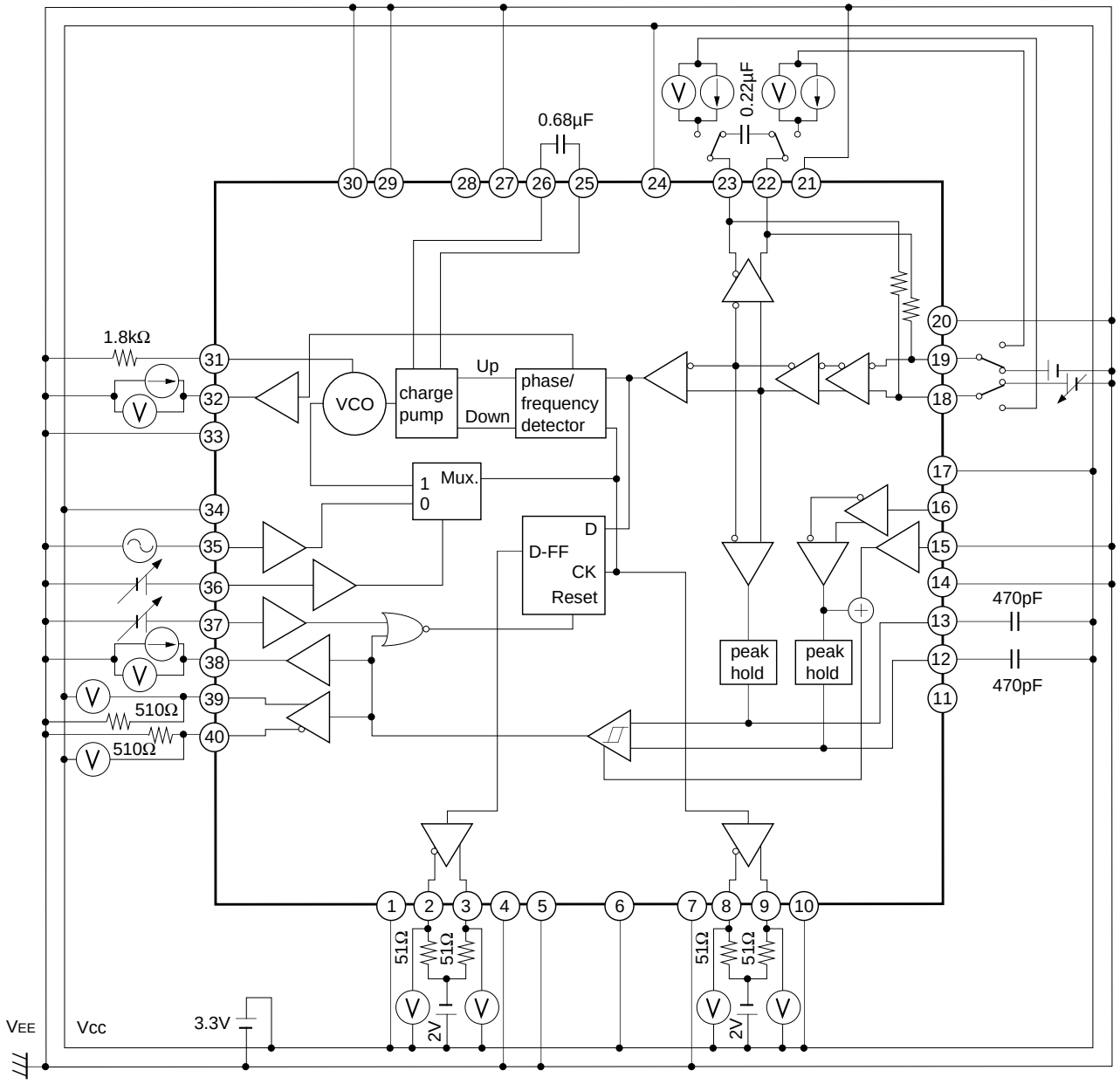
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Post amplifier gain	GL		50			dB
Signal detect hysteresis width	ΔP	HYS = V_{EE}R3, Rd = 22kΩ	3		8	dB
Signal detect response assert time*1	Tas		0		100	µs
Signal detect response deassert time*1	Tdas		2.3		100	µs
Jitter generation*2	R_J	with 12kHz high pass filter		0.008		UIrms
PLL band width*2	F_C			90	130	kHz
Jitter peaking*2				0.06	0.1	dB
Jitter tolerance*2, *3		f = 10Hz	1.5	16		UIp-p
		f = 30Hz	1.5	16		
		f = 300Hz	1.5	16		
		f = 6.5kHz	1.5	4		
		f = 65kHz	0.15	0.5		
PLL capture range*2		DRSEL = High	155.40	155.52	155.60	Mbps
PLL pull in time*2	Tp	DRSEL = High		42		ms
RCK, RDATA output rise time	Tr	51Ω to V_{CC} – 2V, 20% to 80%		600	1000	ps
RCK, RDATA output fall time	Tf	51Ω to V_{CC} – 2V, 20% to 80%		600	1000	ps

*1 D = 155.52Mbps, PN23-1 pattern, 100mVp-p single-ended, Rd = OPEN, CAP2/3 = 470pF

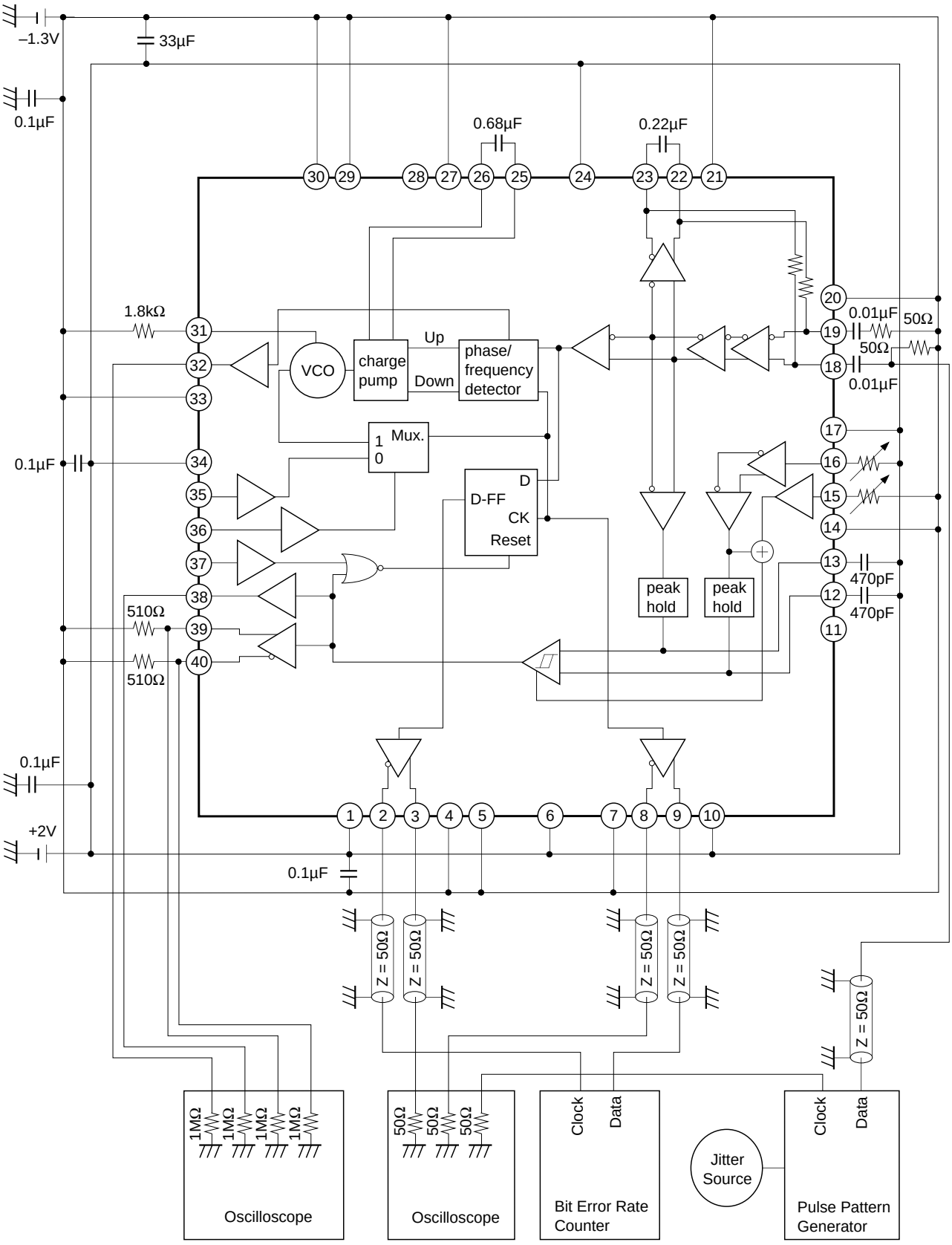
*2 D = 155.52Mbps, PN23-1 pattern, 20mVp-p single-ended, Cp = 0.68µF

*3 Bit Error Rate Threshold: 1E – 10

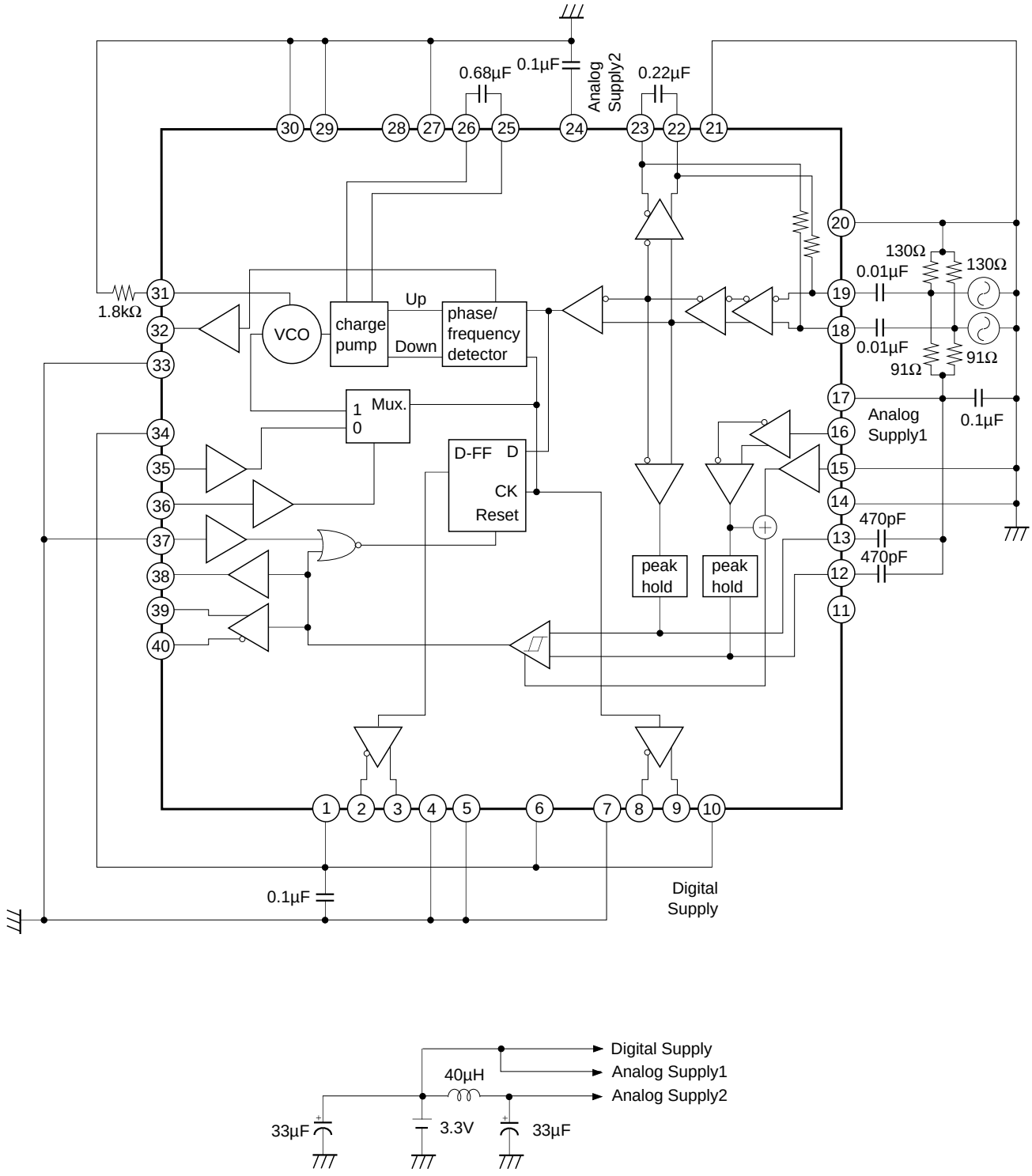
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Limiting amplifier block

The limiting amplifier block is equipped with the auto-offset canceler circuit. When external capacitors C1 and C2 are connected as shown in Fig. 1, the DC bias is set automatically in this block. External capacitor C1 and IC internal resistor R1 determine the low input cut-off frequency f2 as shown in Fig. 2. Similarly, external capacitor C2 and IC internal resistor R2 determine the high cut-off frequency f1 for DC bias feedback. Since peaking characteristics may occur in the low frequency area of the amplifier gain characteristics depending on the f1/f2 combination, set the C1 and C2 so as to avoid the occurrence of peaking characteristics. The target values of R1 and R2 and the typical values of C1 and C2 are as indicated below. When a single-ended input is used, provide AC grounding by connecting Pin 19 to a capacitor which has the same capacitance as capacitor C1.

R1 (internal): 3kΩ
C1 (external): 0.01µF
→ f2: 5.3kHz

R2 (internal): 10kΩ
C2 (external): 0.22µF
→ f1: 7.2kHz

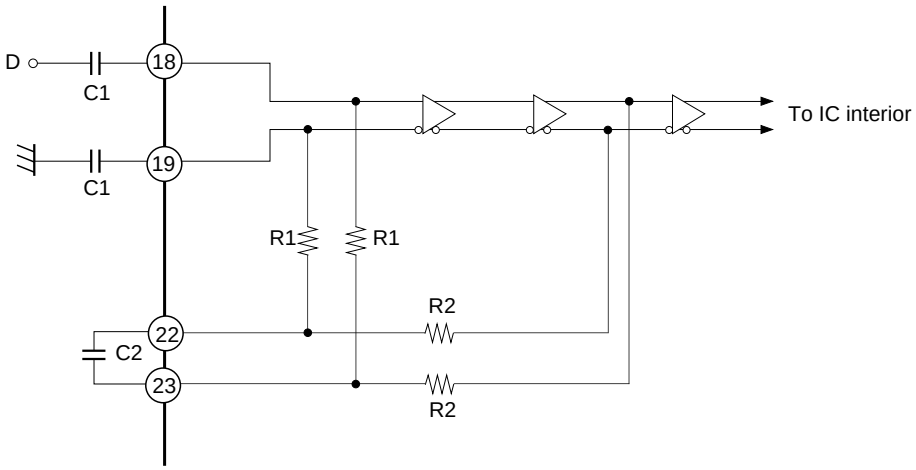


Fig. 1

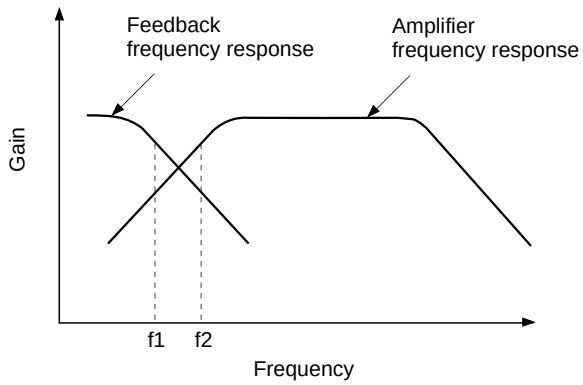


Fig. 2

2. Alarm block

This block provides a signal interruption alarm output used for open fibre control (OFC).
Signal detect threshold level and hysteresis width are both user adjustable.
Signal detect threshold default level is 18mVp-p (single-ended).
An external resister Rd between DOWN and V_{CC}R decrease it.
Typical characteristics of Rd vs. threshold level is shown in fig. 7, 8.
Hysteresis width can be also decreased by an external resister R_H. Typical characteristics of R_H vs. ΔP is shown in fig. 9.
Timing chart of signal detect function is shown in fig. 5. SD response assert/deassert time are decided by peak hold capacitor C_R and C_S.Their typical value is 470pF for 155Mbps operation.

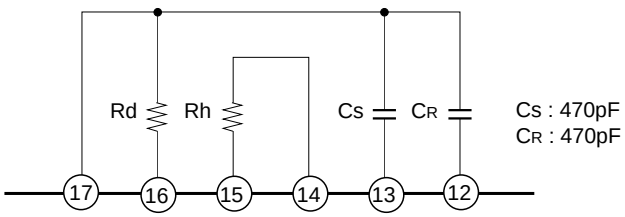


Fig. 3

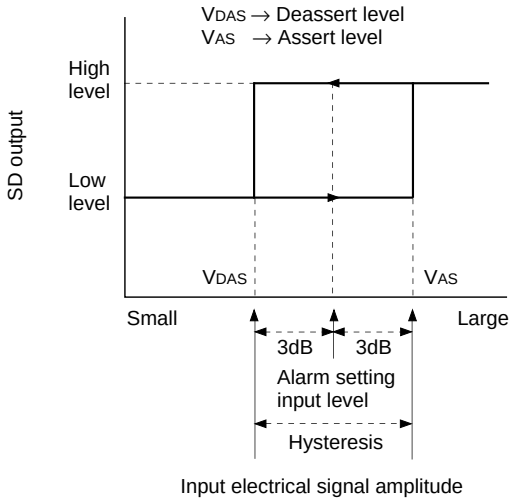


Fig. 4

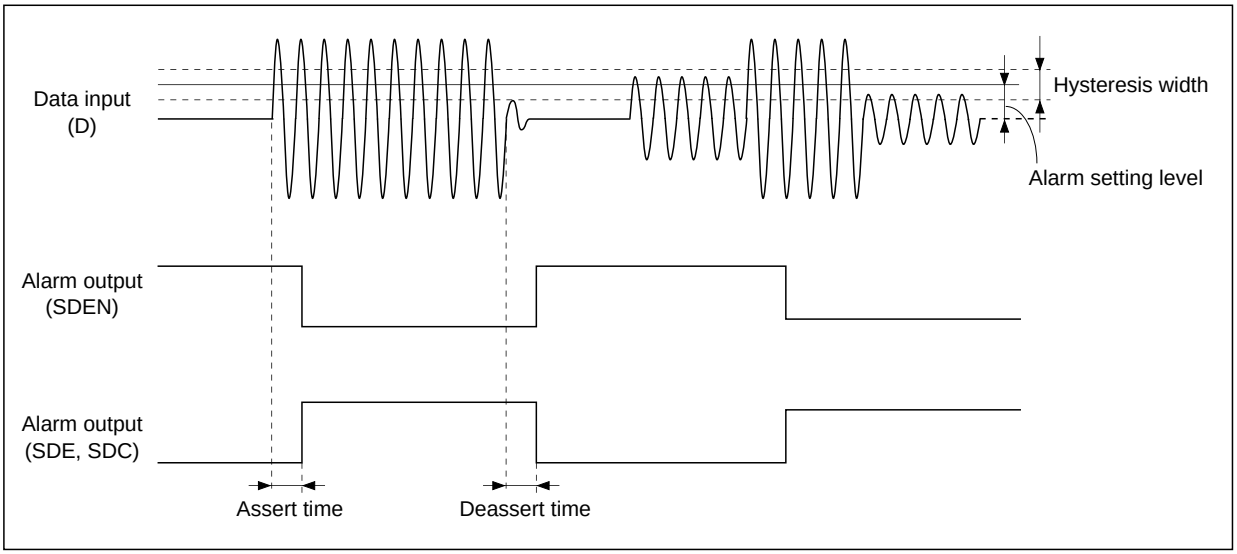


Fig. 5. Timing Chart

3. Clock and Data recovery block

Clock recovery is reallized by fully integrated phase locked loop (PLL), which needs no external reference clock. PLL accepts scrambled NRZ data with 50% mark density. Two external components Re and Cp are required. Their recommended values are shown in fig. 6.

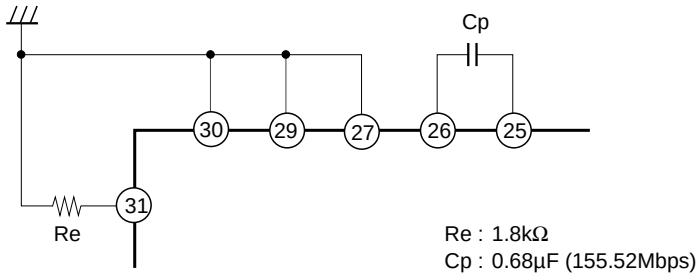


Fig. 6

Re is a resistor which decides VCO center frequency. To reduce the temperature dependence of the VCO oscillation frequency, Re should have a small temperature coefficient. In addition, Re should place as near as IC terminal to obtain good jitter performance.

Cp is a loop filter capacitance. Since loop damping factor ξ is function of $\sqrt{Cp}$, Cp is also important to have a small temperature coefficient. Damping factor ξ is given as

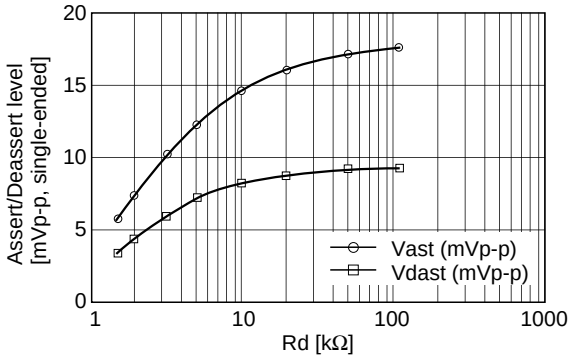
$20{,}000 \times \sqrt{Cp}$ (@ρ = 1/2) *3

Recommended Cp value gives a ξ of 10, and jitter peaking of under 0.1dB is specified.

*3 ρ: data transition density

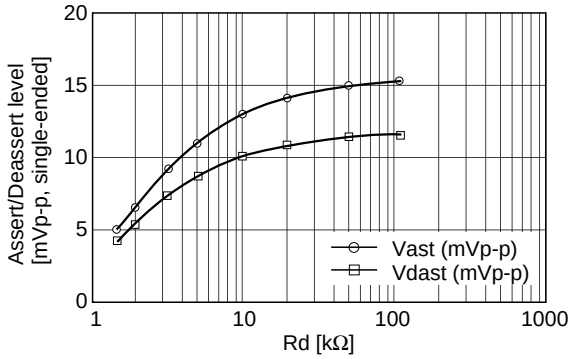
4. Others

Pay attention to handling this IC because its electrostatic discharge strength is weak.



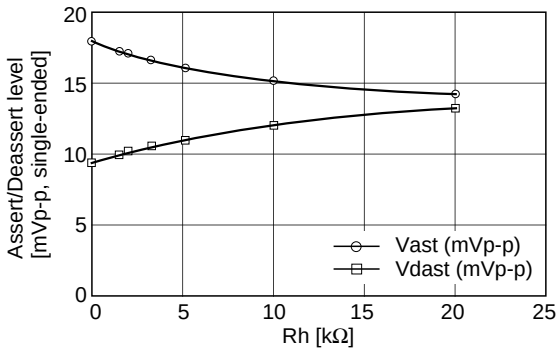
VCC = 3.3V, Ta = 27°C
D = 155.52Mbps, PRBS23-1
20mVp-p, single-ended
Rh = 0Ω

Fig. 7. Rd vs. SD assert/deassert level (Rh = 0Ω)



VCC = 3.3V, Ta = 27°C
D = 155.52Mbps, PRBS23-1
20mVp-p, single-ended
Rh = 8.2kΩ

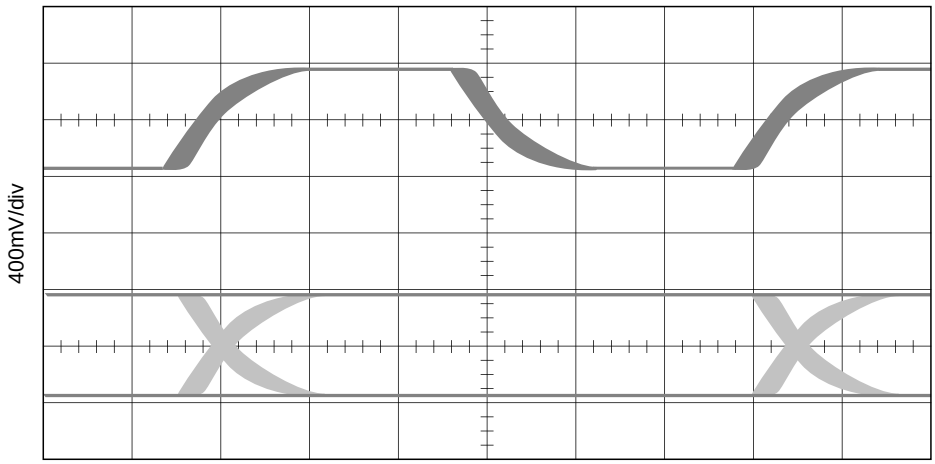
Fig. 8. Rd vs. SD assert/deassert level (Rh = 8.2kΩ)



VCC = 3.3V, Ta = 27°C
D = 155.52Mbps, PRBS23-1
20mVp-p, single-ended
Rd = ∞Ω

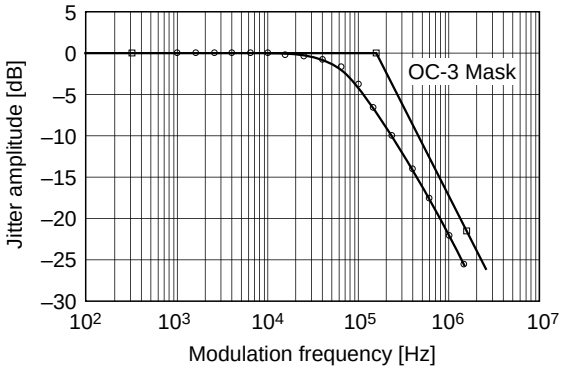
Fig. 9. Rh vs. SD assert/deassert level (Rd = ∞)

Example of Representative Characteristics



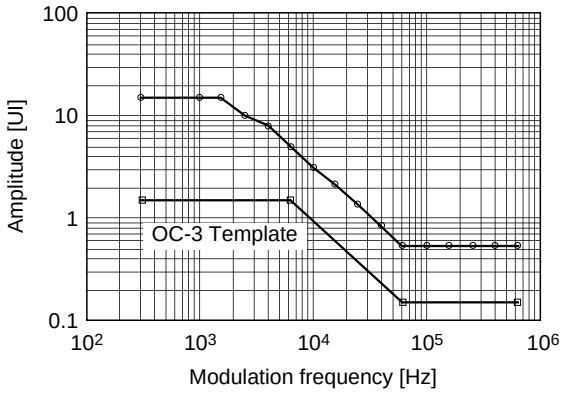
V_{CC} = 3.3V, Ta = 27°C
D = 155.52Mbps, PRBS23-1
20mVp-p, single-ended

Fig. 10. RCK/RDATA output waveform



V_{CC} = 3.3V, Ta = 27°C
D = 155.52Mbps, PRBS23-1
20mVp-p, single-ended

Fig. 11. Jitter transfer function

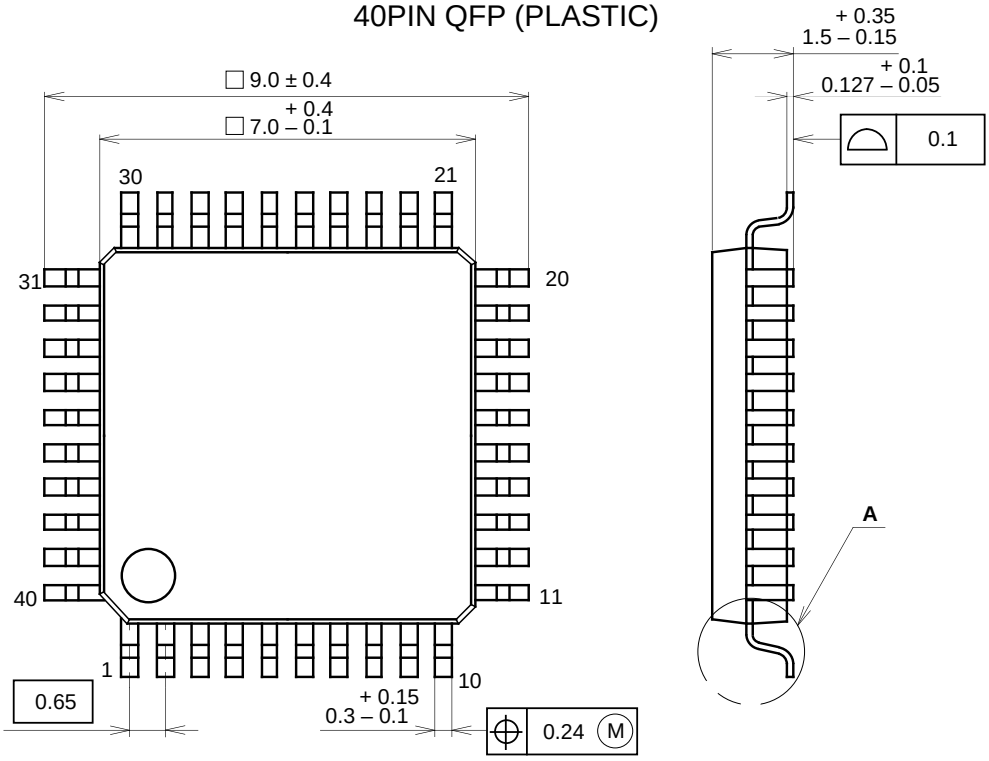


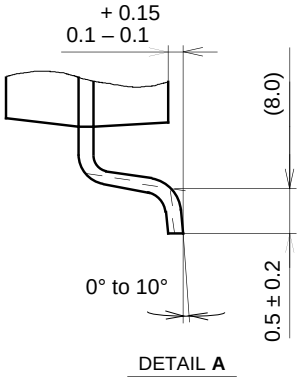
V_{CC} = 3.3V, Ta = 27°C
D = 155.52Mbps, PRBS23-1
20mVp-p, single-ended
Threshold = 1E – 10

Fig. 12. Jitter tolerance

Package Outline Unit: mm

40PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-40P-L01
EIAJ CODE	QFP040-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g