SONY

CXB1586R

10 Bit 1.0625 Gbaud Transceiver

Description

The CXB1586R is a transceiver IC with a built-in PLL for Fibre Channel. For a receiver 1.0625 Gbaud serial data is received and output it as the 10-bit parallel data; for transmitter 1.0625 Gbaud 10-bit parallel data is output as the serial data.

Features

- Transmitter and receiver in a single chip
- ANSI X3T11 Fibre Channel compatible (FC_0) at 1.0625 Gbaud
- Conforms to 10-bit interface specification
- TTL / ECL compatible
- Single +3.3 V power supply
- PLL for clock generation and clock / data recovery
- Byte sync detector (positive character of comma)
- Local loop back circuit
- Low power consumption (0.8 W typ.)
- 64-pin plastic LQFP package (14 mm × 14 mm)

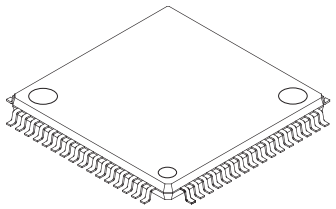
Applications

1.0625 Gbaud Fibre channel

Structure

Bipolar silicon monolithic IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

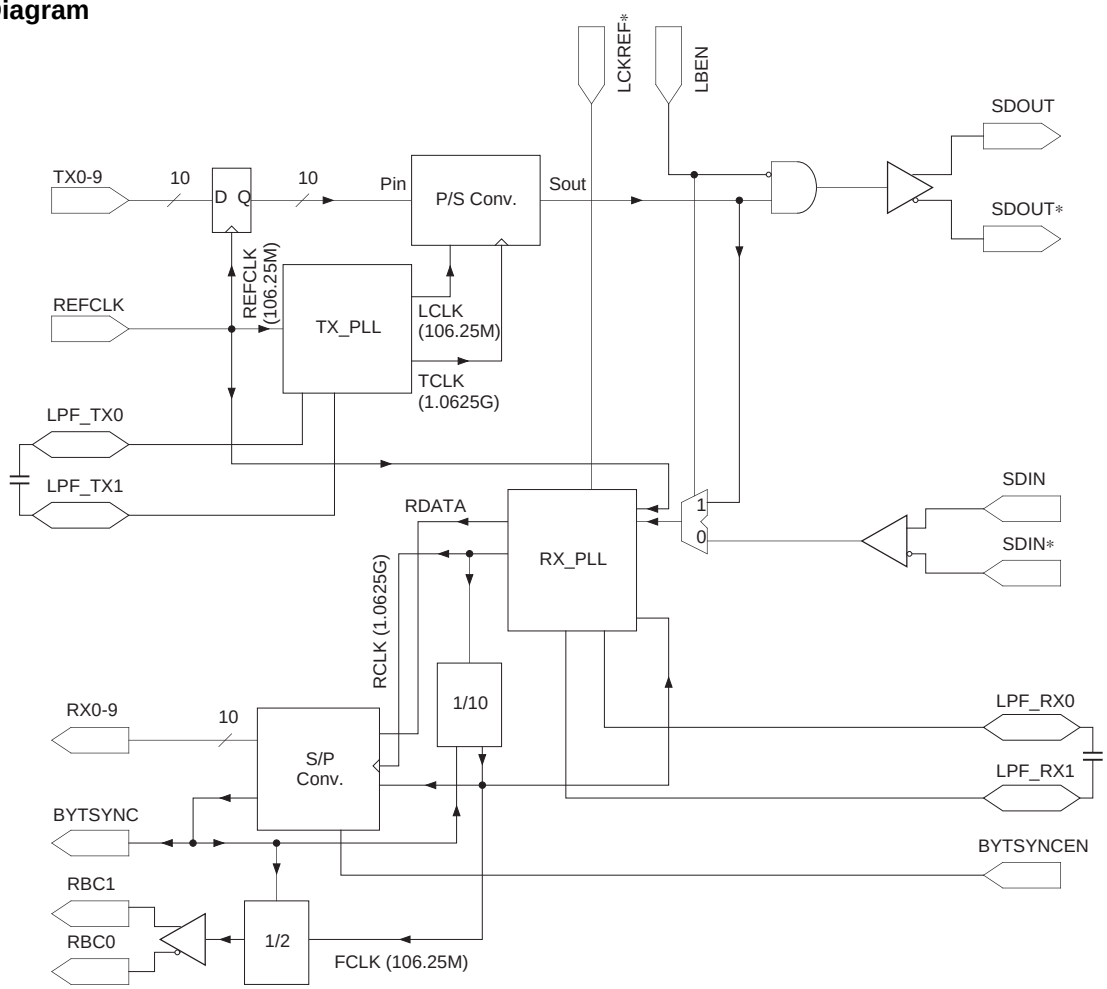
• Supply voltage	V_{CC}	–0.3 to 4	V
• Operating temperature	Topr	–55 to +70	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	to 1109	mW

Operating Conditions

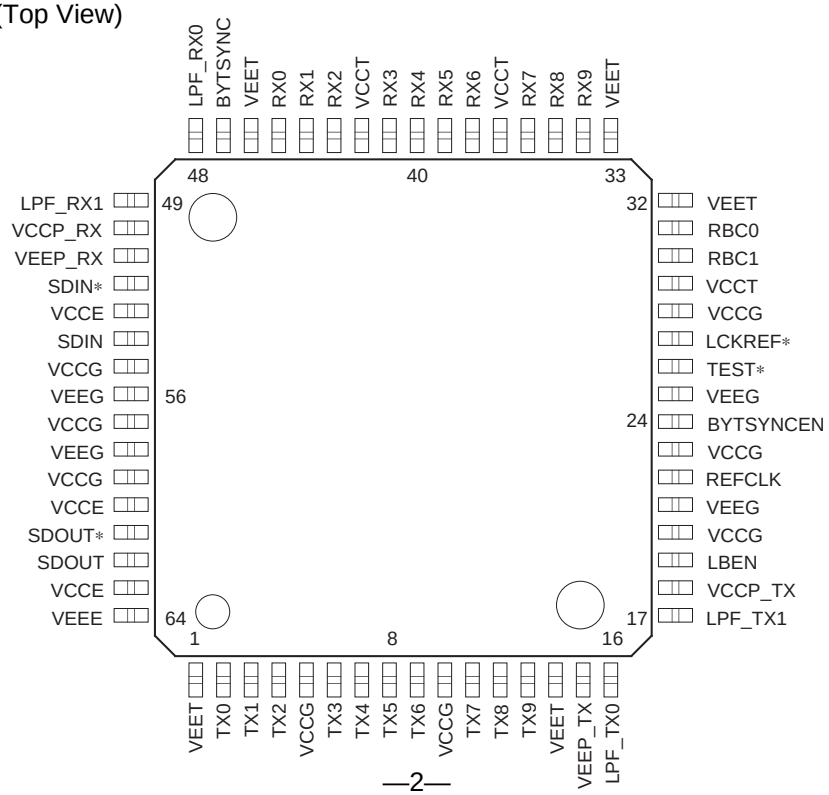
Supply voltage	V_{CC}	3.14 to 3.46	V

E96829D83-TE

Block Diagram



Pin Configuration (Top View)



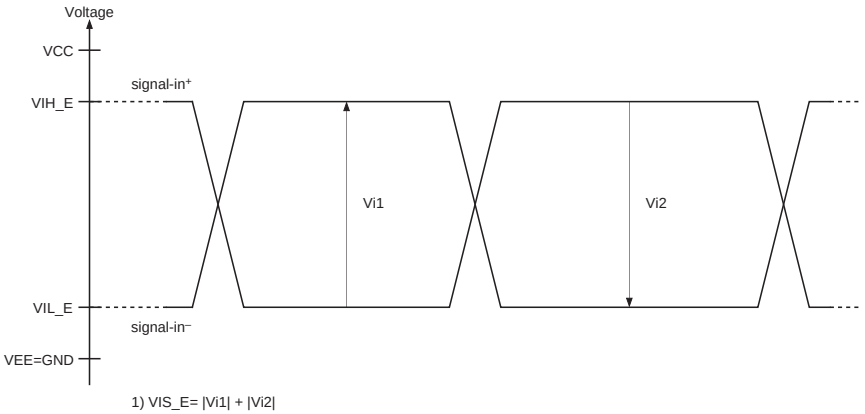
DC Characteristics (under the recommended conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
TTL high level input voltage	VIH_T	2		5.5	V	
TTL low level input voltage	VIL_T	0		0.8	V	
TTL high level input current	IIH_T			20	µA	Vin=V_{CC}
TTL low level input current	IIL_T	–400			µA	Vin=0
TTL high level output voltage	VOH_T	2.2			V	IOH=–0.4 mA
TTL low level output voltage	VOL_T			0.5	V	IOL=2 mA
ECL high level input voltage	VIH_E	V_{CC}–1.17		V_{CC}–0.88	V	
ECL low level input voltage	VIL_E	V_{CC}–1.81		V_{CC}–1.48	V	
ECL peak-to-peak differential input voltage swing	VIS_E **1)**	400		2000	mV	AC coupling input
ECL high level output voltage	VOH_E	V_{CC}–1.05		V_{CC}–0.81	V	50 Ω terminated to V_{CC}–2 V
ECL low level output voltage	VOL_E	V_{CC}–1.81		V_{CC}–1.55	V	50 Ω terminated to V_{CC}–2 V
ECL peak-to-peak differential output to voltage swing	VOS_E **2)**	1200		1900	mV	
Current consumption	I_{CC}		250	320	mA	Output pins open
Power dissipation	P_D		825	1109	mW	Output pins open

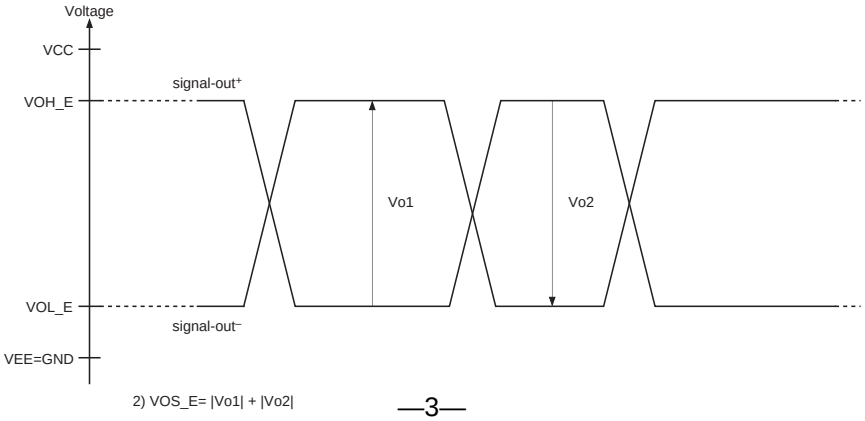
Note :

1) ECL peak-to-peak differential input voltage swing

2) ECL peak-to-peak differential output voltage swing



1) VIS_E= |Vi1| + |Vi2|



2) VOS_E= |Vo1| + |Vo2|

AC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
TTL input rise time of TX	Tir_TX	0.7		4.8	ns	0.8 V to 2.0 V
TTL input fall time of TX	Tif_TX	0.7		4.8	ns	2.0 V to 0.8V
TTL input rise time of REFCLK	Tir_REF	0.7		2.4	ns	0.8 V to 2.0 V
TTL input fall time of REFCLK	Tif_REF	0.7		2.4	ns	2.0 V to 0.8 V
TTL output rise time	Tor_T			3.5	ns	0.8 V to 2.0 V, CL=10 pF
TTL output fall time	Tof_T			3.5	ns	2.0 V to 0.8 V, CL=10 pF
ECL output rise time	Tor_E			400	ps	20 % to 80 %, CL=2 pF
ECL output fall time	Tof_E			400	ps	20 % to 80 %, CL=2 pF
REFCLK period	Tp_REF	9.26	9.41	9.56	ns	
REFCLK duty cycle	DC_REF	40		60	%	
REFCLK frequency tolerance	Ftol_REF	–100		100	ppm	
TX setup time to REFCLK	Ts_TX	2			ns	
TX hold time to REFCLK	Th_TX	1.5			ns	
RX setup time to RBC	Ts_RX	3			ns	
RX hold time to RBC	Th_RX	1.5			ns	
Skew between RBC0 and 1	Tsk_RBC	Tp/2–0.5	Tp/2	Tp/2+0.5	ns	Tp is period of RBC
RBC duty cycle	DC_RBC	40		60	%	in frequency lock
Deterministic jitter (p-p)	DJ		0.02	0.07	UI	Serial data output (k28.5)
Random jitter (p-p)	RJ		0.18	0.23	UI	Serial data output
Jitter tolerance	JT			0.7	UI	Serial data input

PLL AC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency acquisition time of TX and RX PLL	Tfa			500	µs	Loop damping capacitor=0.01 µF
Bit synchronization time of RX PLL	Tbs			2500	bit	

Absolute Maximum Ratings (VEEE, VEET, VEEG, VEEP=GND)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage (Except VCCT5)	V_{CC}	–0.3		4	V	
TTL DC input voltage	VI_T	–0.5		5.5	V	
ECL DC input voltage	VI_E	V_{CC}–2		V_{CC}	V	
ECL peak-to-peak differential input voltage swing	VIS_E	–4		4	V	
TTL output current (High level)	IOH_T	–20		0	mA	
TTL output current (Low level)	IOL_T	0		20	mA	
ECL output current	IO_E	–30		0	mA	
Ambient temperature	Ta	–55		70	°C	Under bias
Storage temperature	Tstg	–65		150	°C	

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage (Including VCCT5)	V_{CC}	3.135	3.3	3.465	V	
Ambient temperature	Ta	0		70	°C	

Pin description

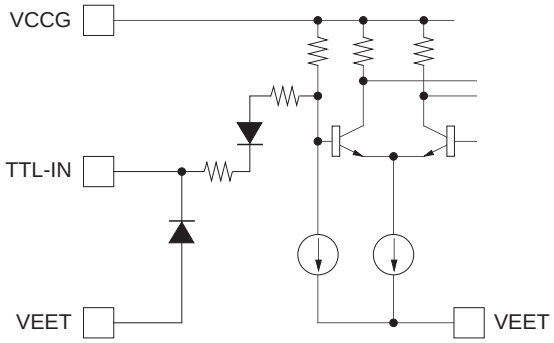
Pin No.	Symbol	Type	Description	Equivalent circuit
1, 14, 32, 33, 46	VEET	PS	Ground for TTL output : Normally 0 V.	—
2-4, 6-9, 11-13	TX0-9	I_TTL	Parallel transmit data inputs to be serialized. TX0 is serialized first and TX9 is last.	(a)
5, 10, 20, 23, 28, 55, 57, 59	VCCG	PS	Power supply for internal logic gates : Normally 3.3 V.	—
15	VEEP_TX	PS	Ground for TX PLL : Normally 0 V.	—
16 17	LPF_TX0 LPF_TX1	EX	Connect to external loop filter of TX PLL. Connect a capacitor (0.01 µF) between LPF_TX0 and LPF_TX1.	(e)
18	VCCP_TX	PS	Power supply for TX PLL : Normally 3.3 V.	—
19	LBEN	I_TTL	Loop back enable : When high, TX serializer output internally connects to RX deserializer input, SDOUT/SDOUT* is held low/high, and SDIN/SDIN* is disabled. When low, SDOUT/SDOUT* and SDIN/SDIN* are enabled.	(a)
21, 25, 56, 58	VEEG	PS	Power supply for internal logic gates : Normally 0 V.	—
22	REFCLK	I_TTL	Reference clock for PLL and transmit byte clock (106.25 MHz). Supplied by the host system.	(a)
24	BYTSYNCEN	I_TTL	Byte synchronization enable : When high, the positive comma character (0011111) detection circuit is enabled to establish byte synchronization (see Timing Chart).	(a)
26	TEST*	I_TTL	Test pin : Normally 3.3 V or open.	(a)
27	LCKREF*	I_TTL	Lock to reference clock : An active low input. LCKREF* forces the PLL lock to the REFCLK supplied by the host system.	(a)
29, 37, 42	VCCT	PS	Power supply for TTL output : Normally 3.3 V.	—
30 31	RBC1 RBC0	O_TTL	Receive byte clocks recovered from the serial data (53.125 MHz). These clocks are 180 degrees out of phase, and RX0-9 are alternatively clocked on the rising edge of these clocks (see Timing Chart)	(b)
34-36, 38-41, 43-45	RX0-9	O_TTL	Parallel receive data output : RX0 is received first and RX9 is last.	(b)
47	BYTSYNC	O_TTL	Byte synchronization indicator : High when a positive comma character is detected (see Timing Chart)	(b)
48 49	LPF_RX0 LPF_RX1	EX	Connect to external loop filter of RX PLL. Connect a capacitor (0.01 µF) between LPF_RX0 and LPF_RX1.	(e)
50	VCCP_RX	PS	Power supply for RX PLL : Normally 3.3 V.	—
51	VEEP_RX	PS	Ground for RX PLL : Normally 0 V.	—

Pin No.	Symbol	Type	Description	Equivalent circuit
52 54	SDIN* SDIN	I_ECL (Diff.)	Serial receive data inputs : These inputs are enabled when LBEN is low.	(c)
53, 60, 63	VCCE	PS	Power supply for ECL output : Normally 3.3 V	—
61 62	SDOUT* SDOUT	O_ECL (Diff.)	Serial transmit data output : These outputs are enabled when LBEN is low. When LBEN is high, SDOUT/SDOUT* is held to low/high.	(d)
64	VEEE	PS	Ground for ECL output : Normally 0 V.	—

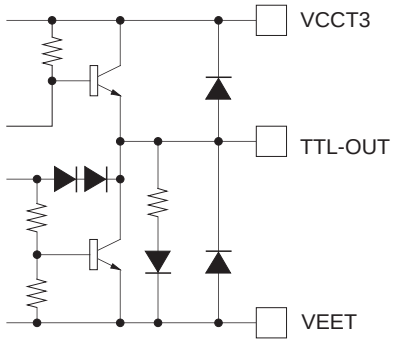
Pin Type Definition

Type	Definition
PS	Power supply or ground
I_TTL	Input TTL
O_TTL	Output TTL
I_ECL	Input ECL
O_ECL	Output ECL
EX	External circuit node

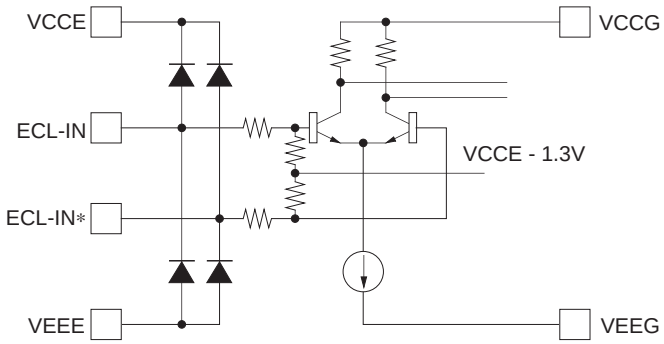
Equivalent Circuit



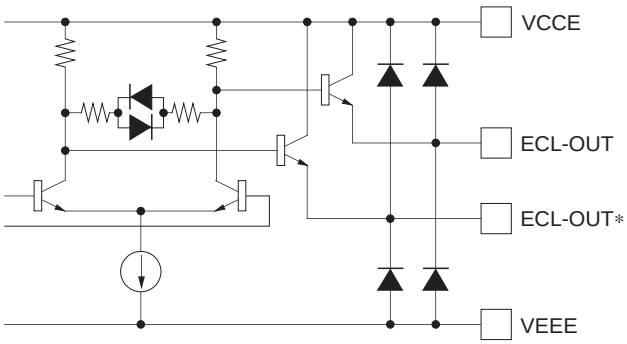
(a) TTL input



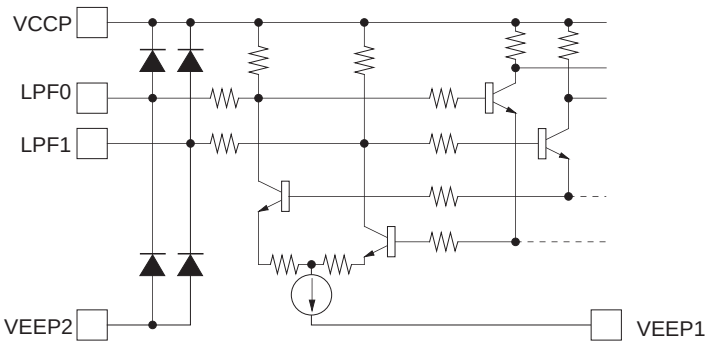
(b) TTL output



(c) ECL input

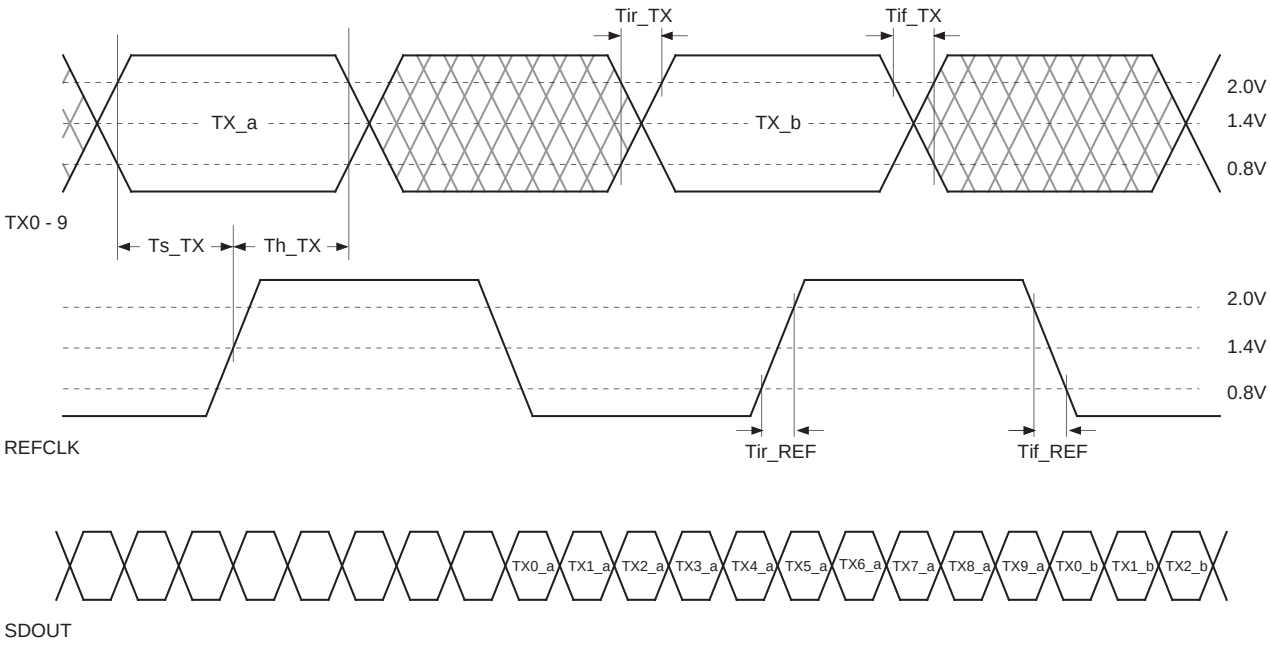


(d) ECL output

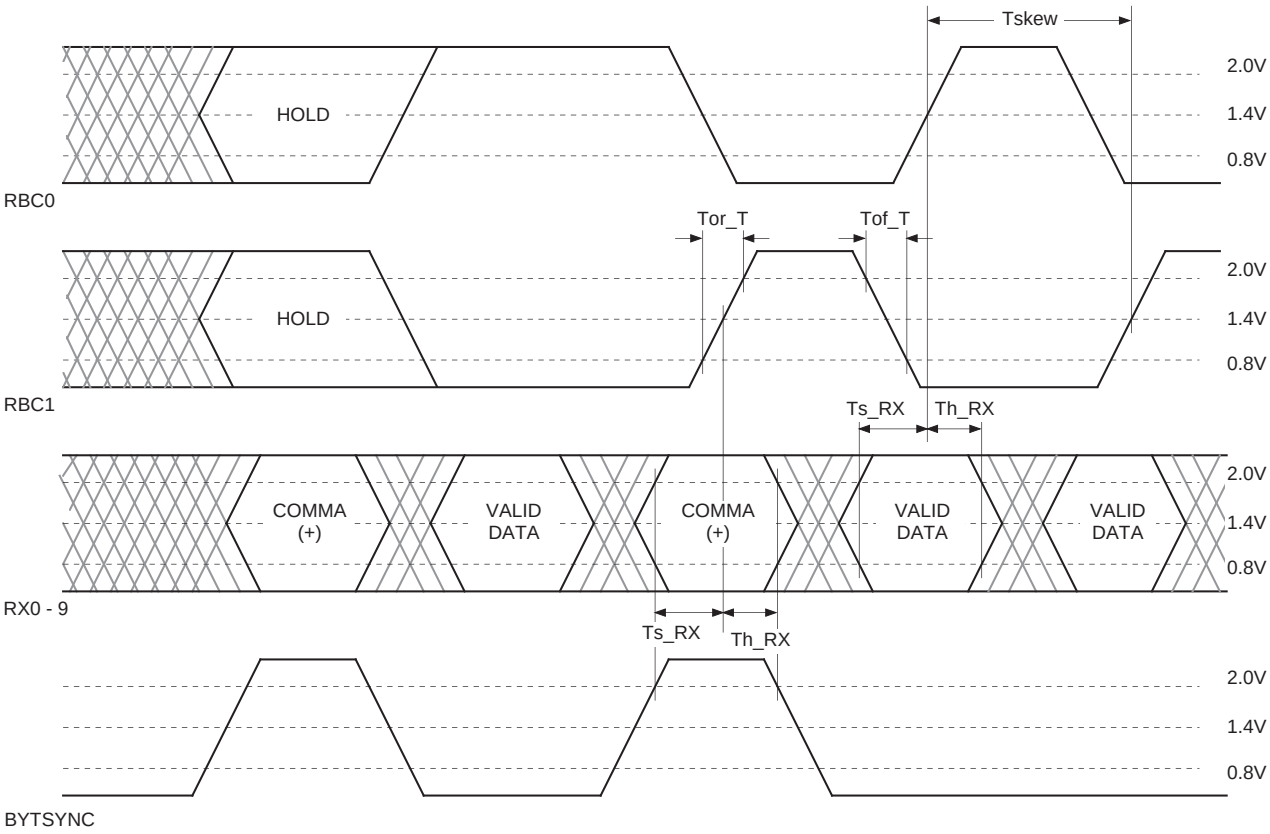


(e) LPF0/LPF1-pin

Timing Chart



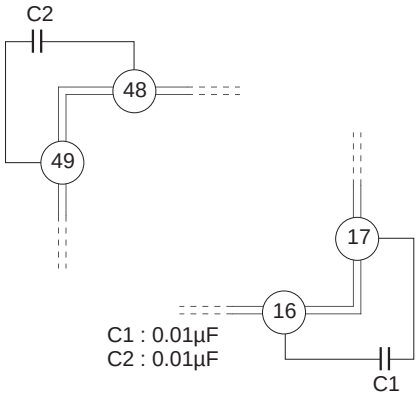
(a) Transmiter Section Timing



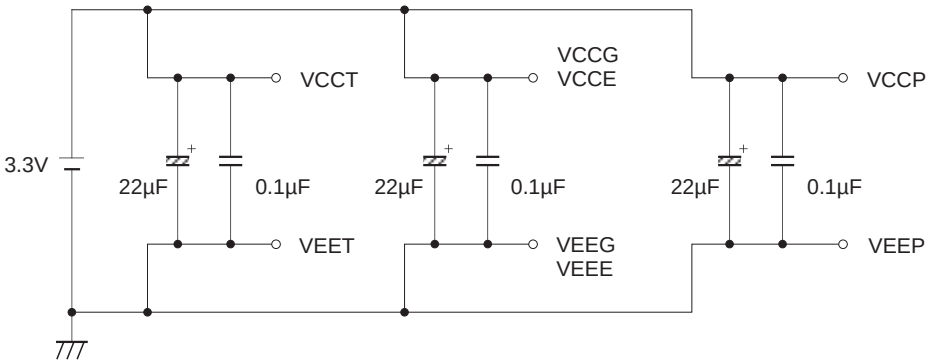
(b) Receiver Section Timing

Notes on Operation

1. External loop filters for PLLs
   The CXB1586R has two PLLs. One is for the transmitter and locks to the reference clock from REFCLK input pin. Another one is for the receiver and locks to the received serial data from SDIN/SDIN* input pins. They need external capacitors for the their loop filters. Typical values of the external capacitors are indicated below.

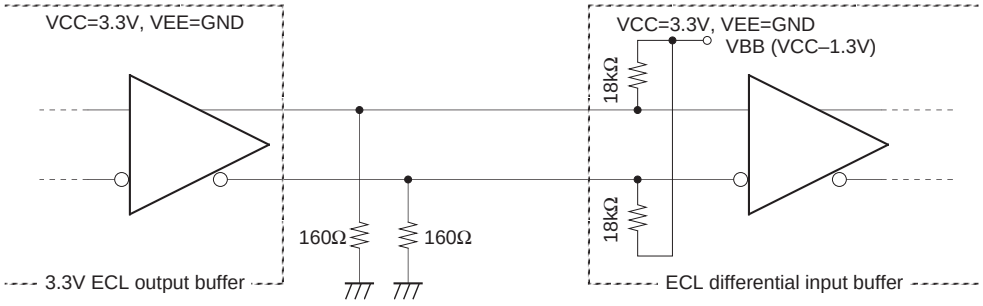


2. Example of power supply circuit

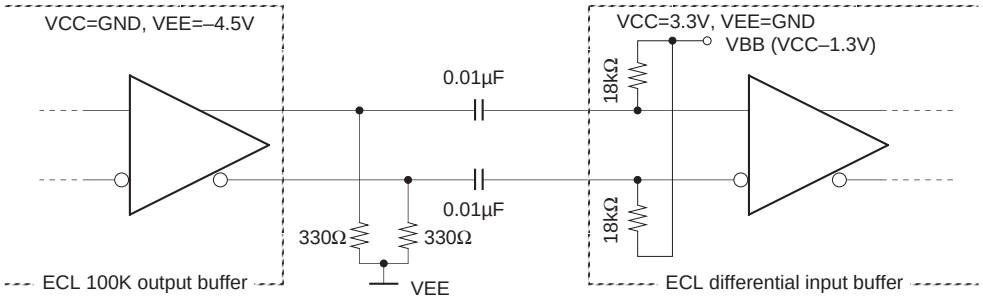


3. High-speed ECL differential input

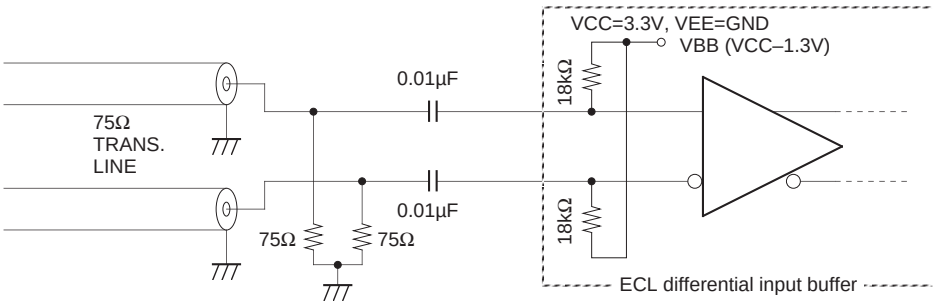
The high-speed ECL differential input pins are biased to VBB (V_{CC}–1.3V) via a 18 kΩ resistor in the IC. See the figures below for ECL differential input methods.



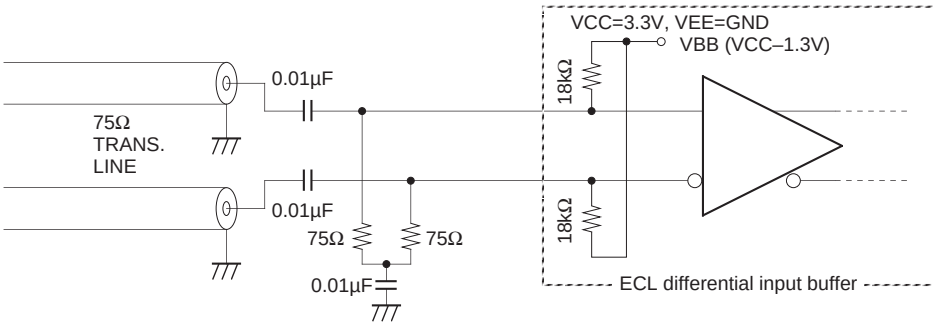
(a) ECL differential signal from 3.3V ECL output buffer



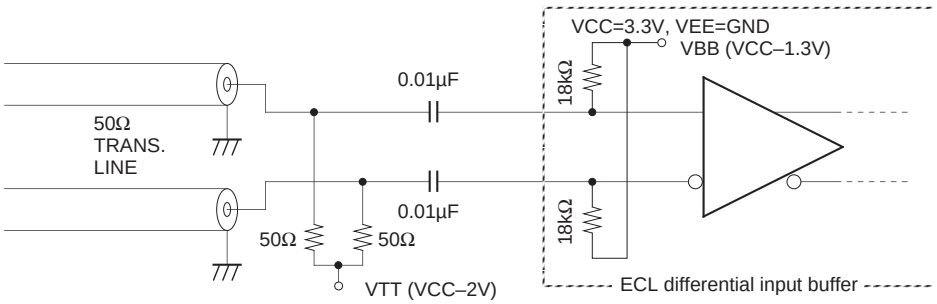
(b) ECL differential signal from ECL 100K output buffer



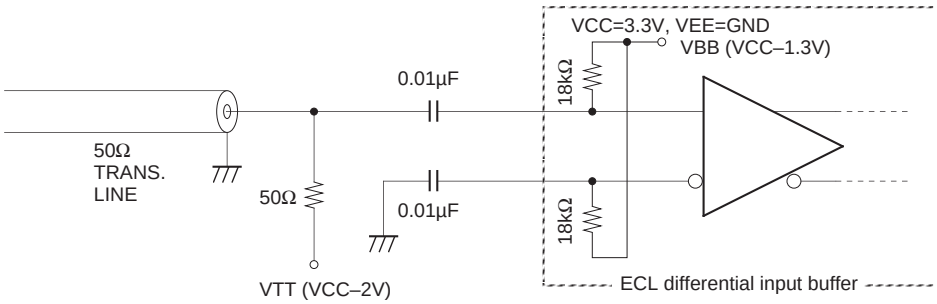
(c) differential signal from 75Ω transmission line (AC/DC termination)



(d) differential signal from 75Ω transmission line (AC termination)

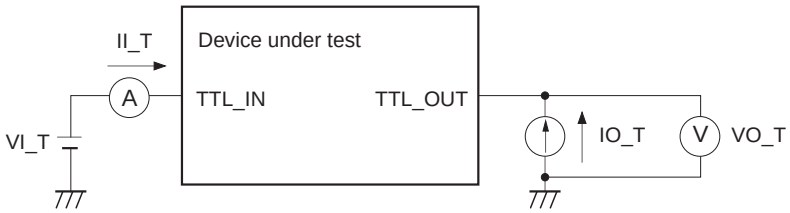


(e) ECL differential signal from 50Ω transmission line

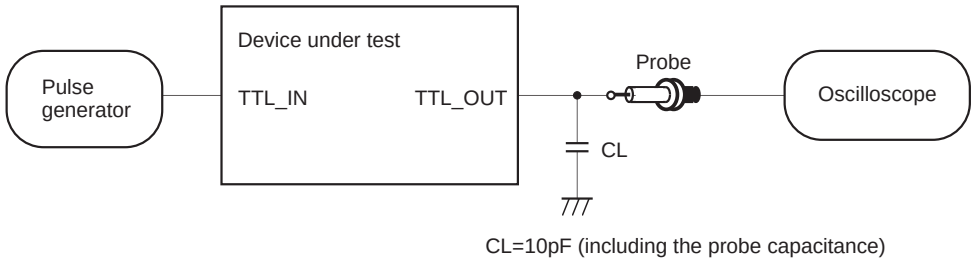


(f) ECL single signal from 50Ω transmission line

Electrical Characteristics Measurement Circuit

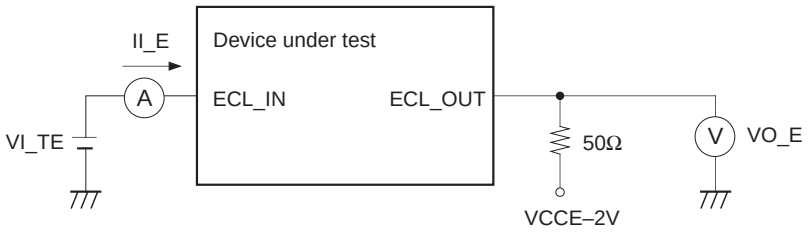


(a) TTL I/O DC characteristics measurement circuit

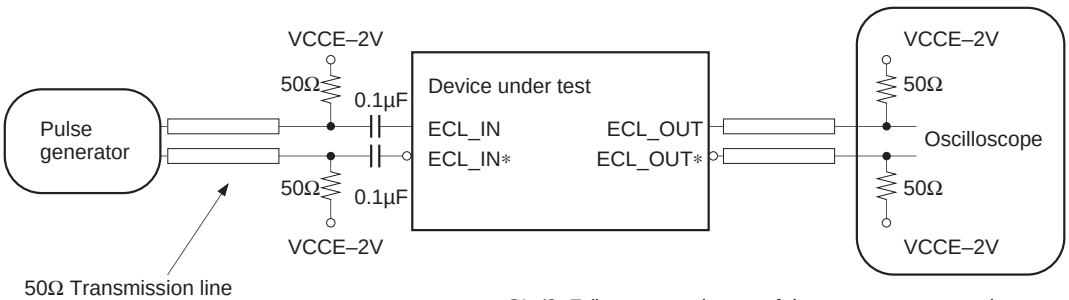


CL=10pF (including the probe capacitance)

(b) TTL I/O AC characteristics measurement circuit

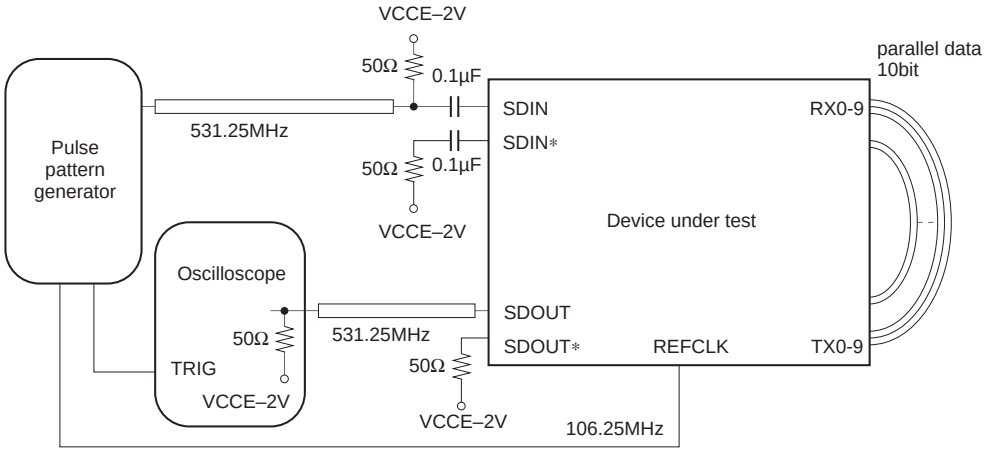


(c) ECL I/O DC characteristics measurement circuit

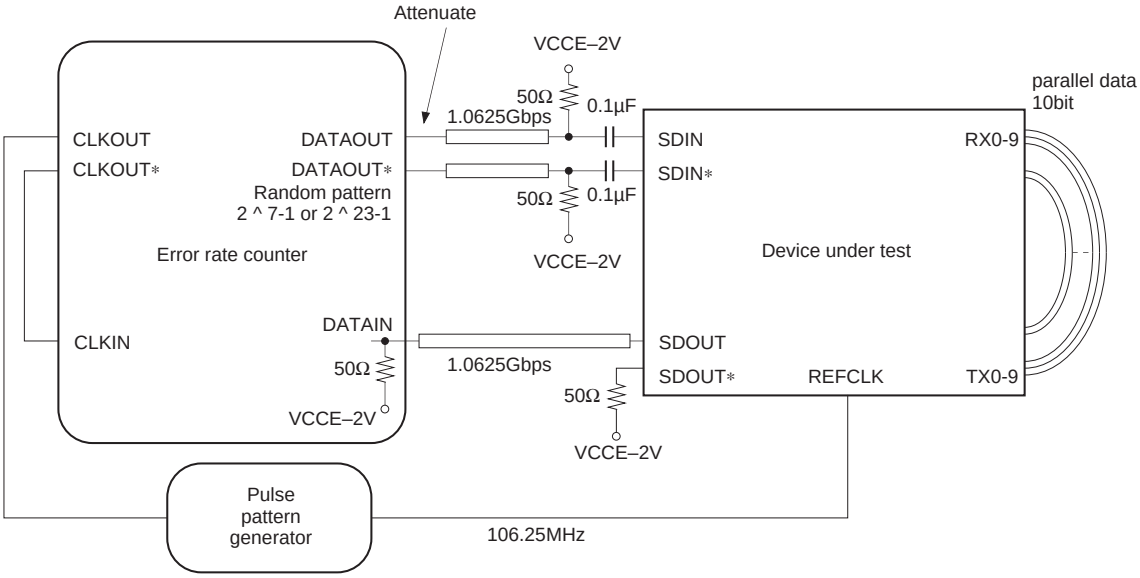


CL≤2pF (input capacitance of the measurement equipment and floating capacitance)

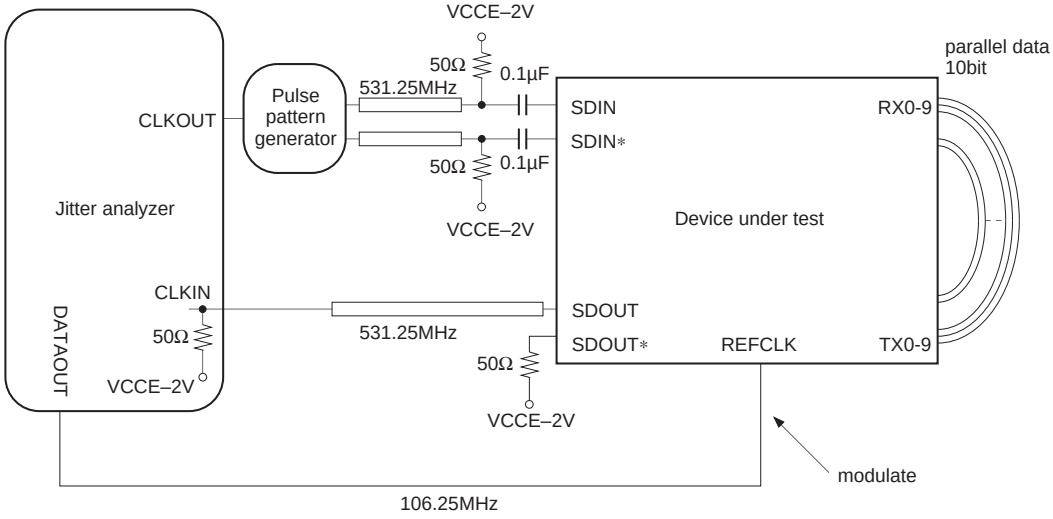
(d) ECL I/O AC characteristics measurement circuit



(e) TX random jitter measurement circuit



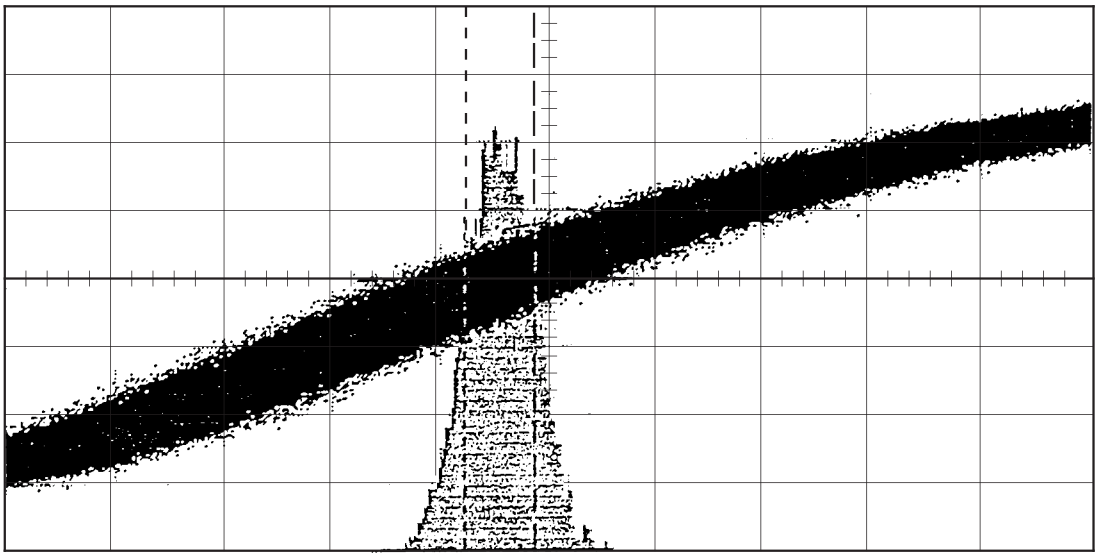
(f) Error rate measurement circuit



(g) TX jitter transfer measurement circuit

Example of Representative Characteristics

Example of TX Rj measurement (SDOUT)



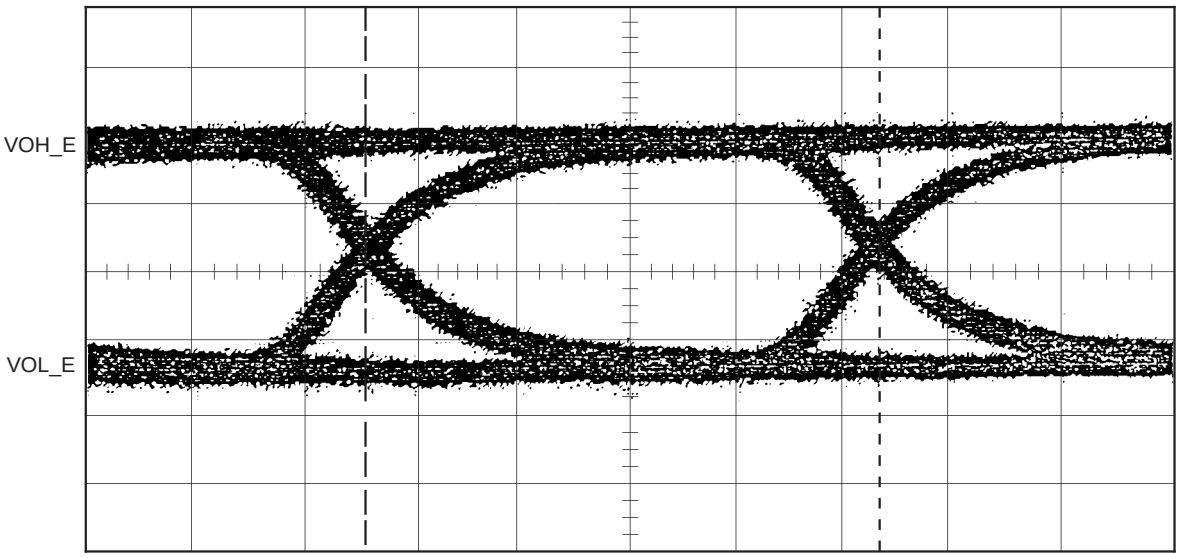
$C_1 = C_2 = 0.01\mu F$

SDIN input 1.0625Gbps (Transition Density : 100%)
REFCLK input 106.25MHz

Rj = 9.6psec

x : 30psec / div
y : 100mV / div

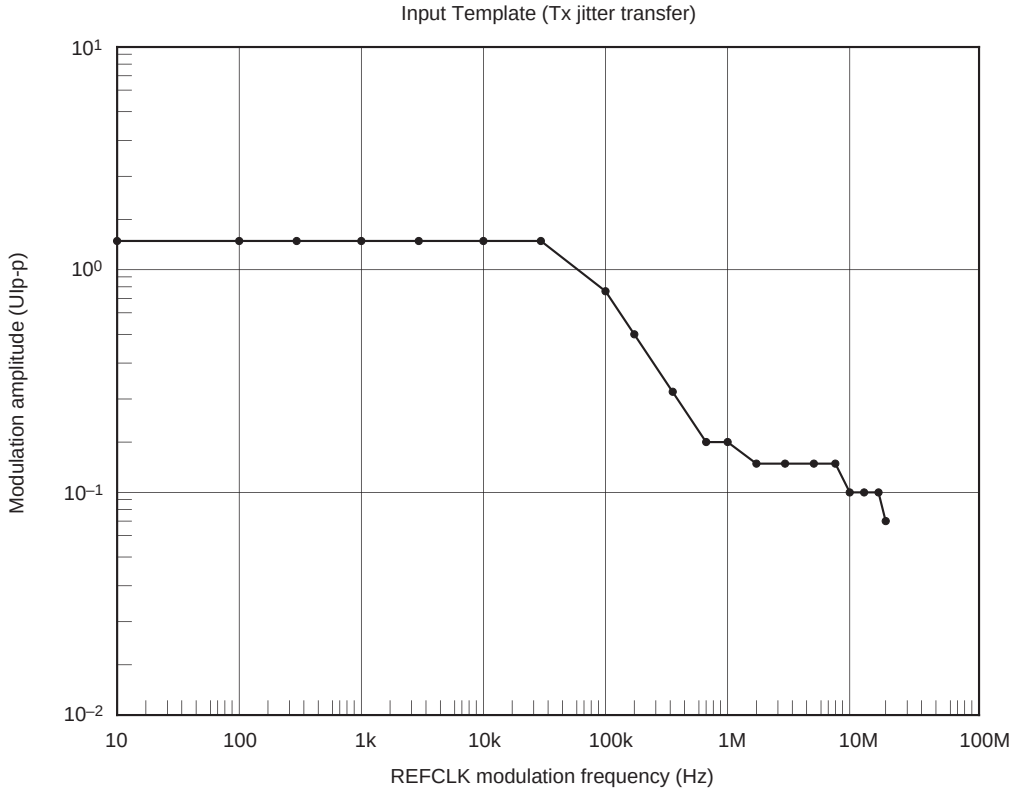
TX Eye Pattern (SDOUT 1.0625GHz operation)

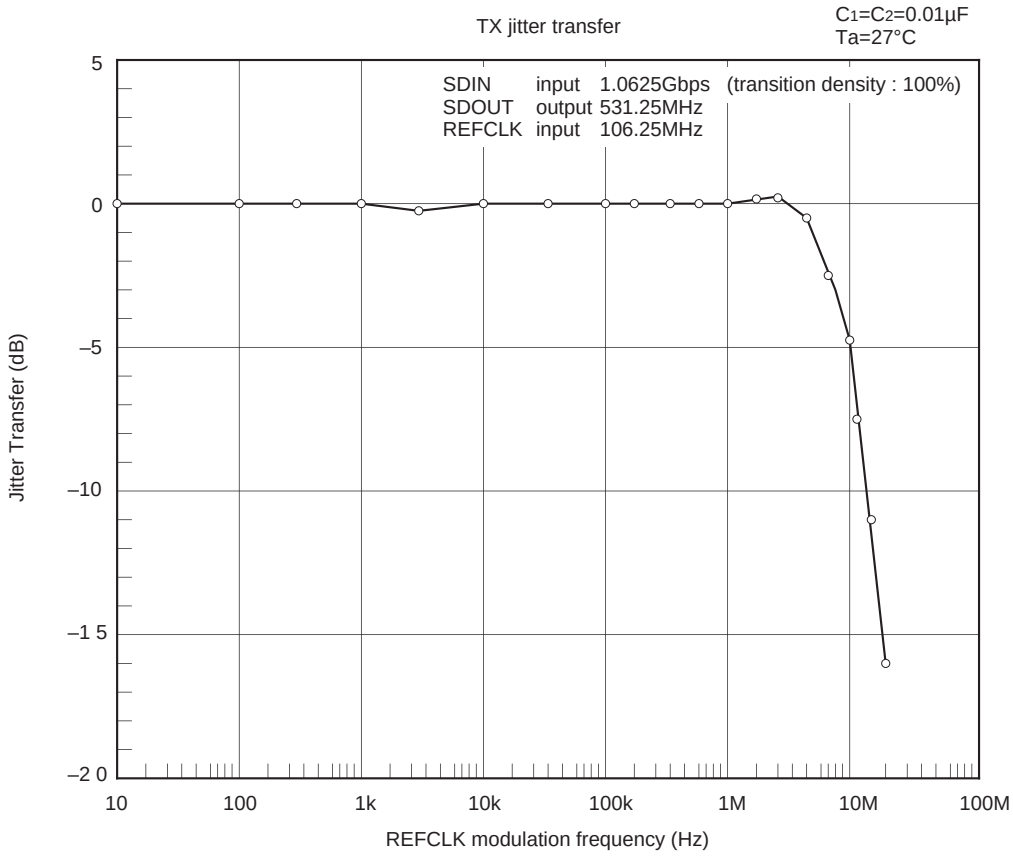


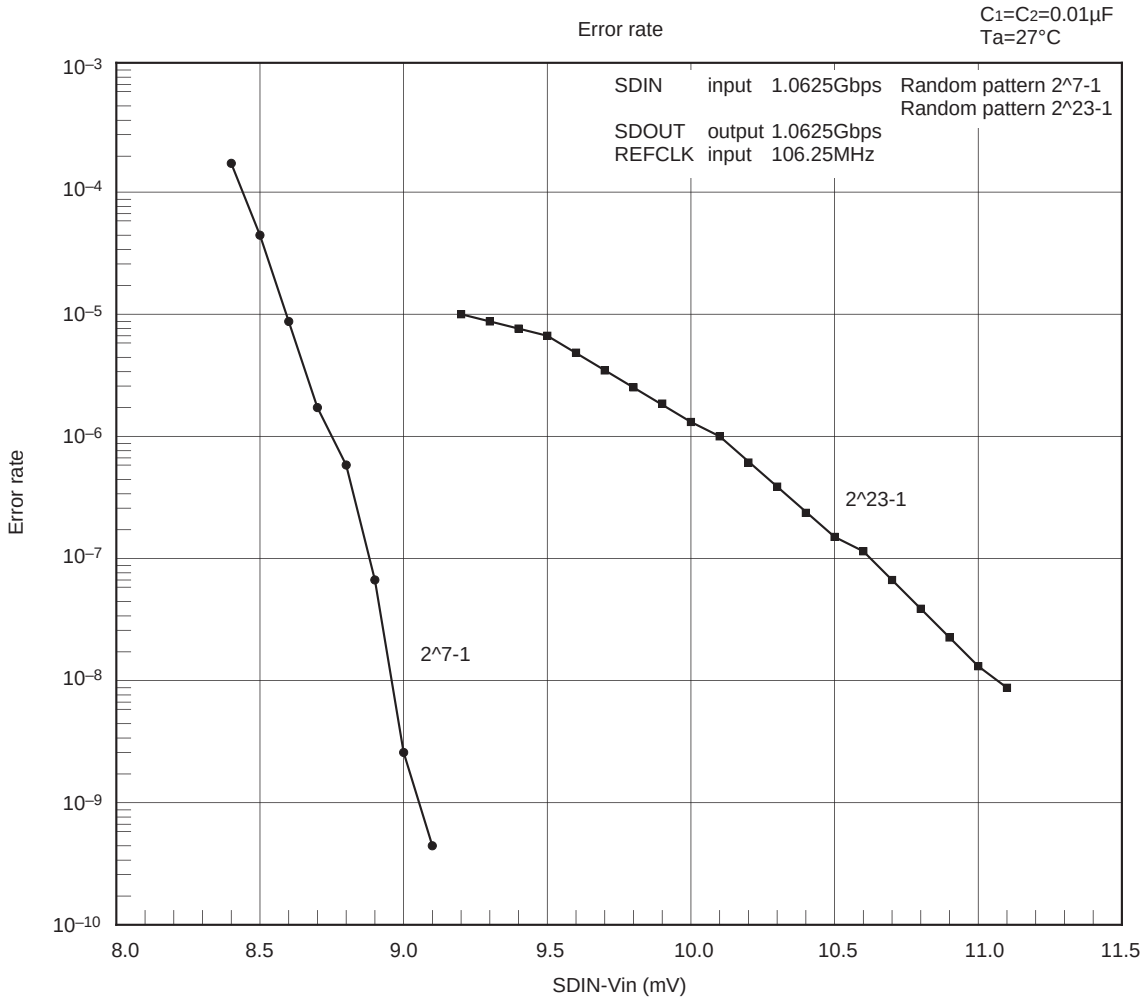
$C_1 = C_2 = 0.01\mu F$

SDIN input 1.0625Gbps Random pattern
REFCLK input 106.25MHz

x : 200psec / div
y : 200mV / div

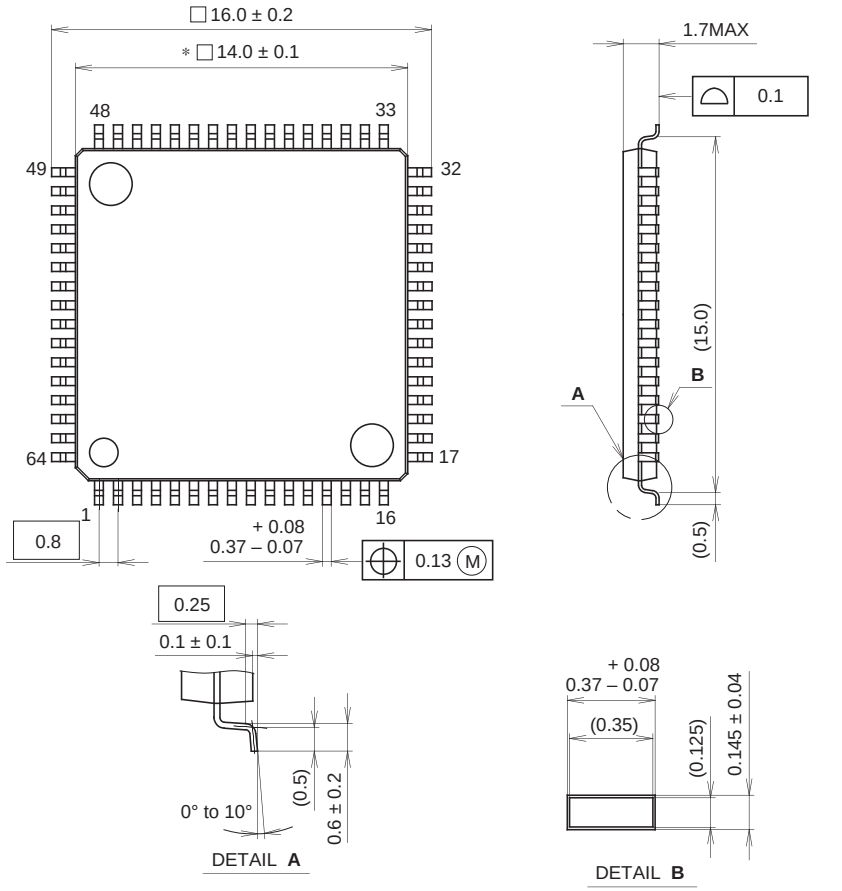

Input Template (Tx jitter transfer)
Modulation amplitude (UIp-p)
10^1
10^0
10^–1
10^–2
10
100
1k
10k
100k
1M
10M
100M
REFCLK modulation frequency (Hz)


TX jitter transfer
C1=C2=0.01µF
Ta=27°C
SDIN input 1.0625Gbps (transition density : 100%)
SDOUT output 531.25MHz
REFCLK input 106.25MHz
Jitter Transfer (dB)
5
0
–5
–10
–1 5
–2 0
10
100
1k
10k
100k
1M
10M
100M
REFCLK modulation frequency (Hz)


Error rate
C1=C2=0.01µF
Ta=27°C
SDIN input 1.0625Gbps Random pattern 2^7-1
Random pattern 2^23-1
SDOUT output 1.0625Gbps
REFCLK input 106.25MHz
2^23-1
2^7-1
Error rate
10–3
10–4
10–5
10–6
10–7
10–8
10–9
10–10
8.0
8.5
9.0
9.5
10.0
10.5
11.0
11.5
SDIN-Vin (mV)

Package Outline Unit : mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L02
EIAJ CODE	LQFP064-P-1414
JEDEC CODE	———————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g