SONY

CXD2304R

8-bit 20MSPS RGB 3-Channel D/A Converter

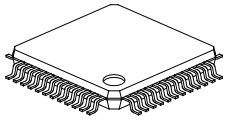
Description

The CXD2304R is an 8-bit high-speed D/A converter for video band use. It has an input/output equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, and others.

Features

- Resolution 8-bit
- Maximum conversion speed 20MSPS
- RGB 3-channel input/output
- Differential linearity error +0.5LSB
- Low power consumption 50mW
  (330Ω load at 1.2Vp-p output)
- Single 3.3V power supply
- Low glitch noise

48 pin LQFP (Plastic)



Structure

Sillicon gate CMOS IC

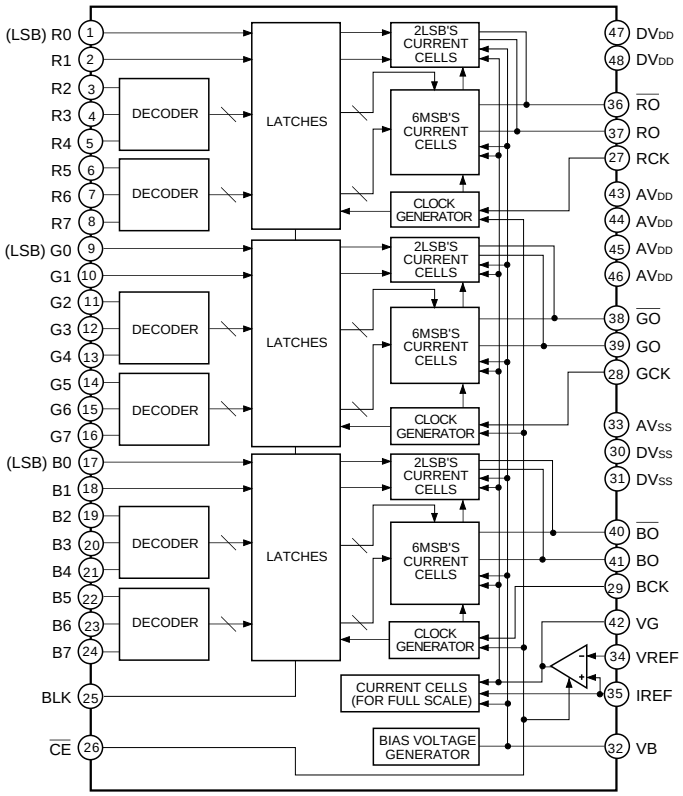
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	3.0 to 3.6	V
	DV_{DD}, DV_{SS}	3.0 to 3.6	V
• Reference input voltage	V_{REF}	1.2	V
• Clock pulse width	Tpw_1	25 (Min.)	ns
	Tpw_0	25 (Min.)	ns
• Operating temperature	Topr	–20 to + 75	°C

Absolute Maximum Ratings (Ta = 25°C)

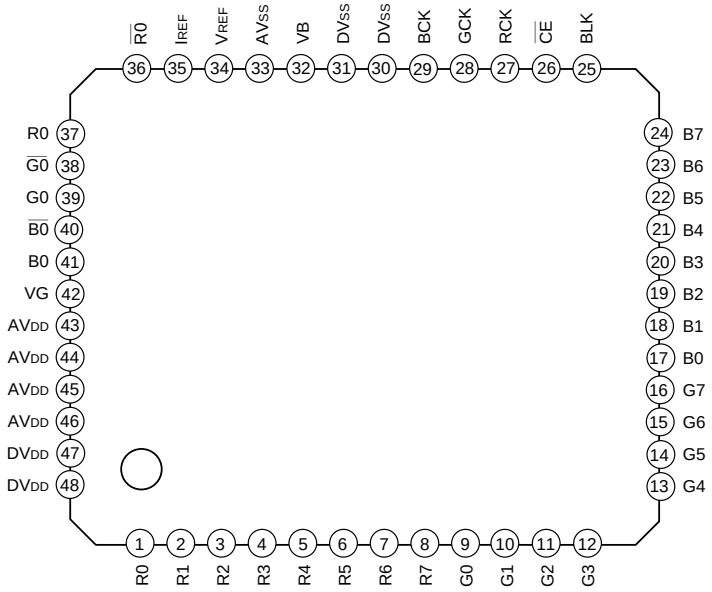
• Supply voltage	V_{DD}	7	V
• Input voltage	V_{IN}	V_{DD} to V_{SS}	V
• Output current (Every each channel)	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	–55 to +150	°C

Block Diagram

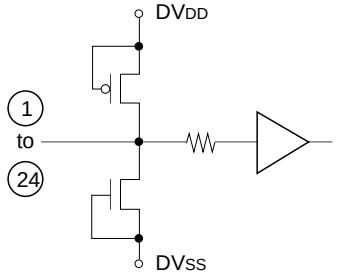
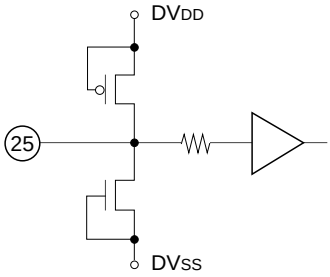
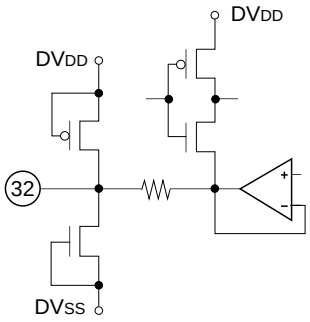


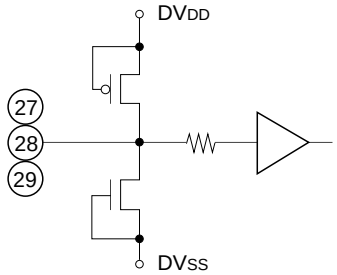
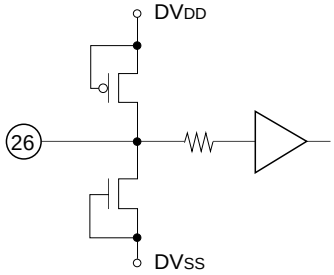
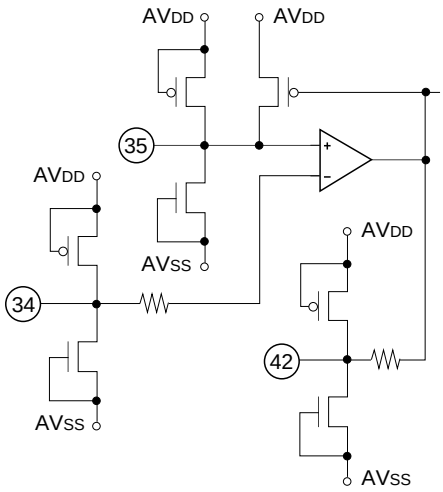
E94307-PK

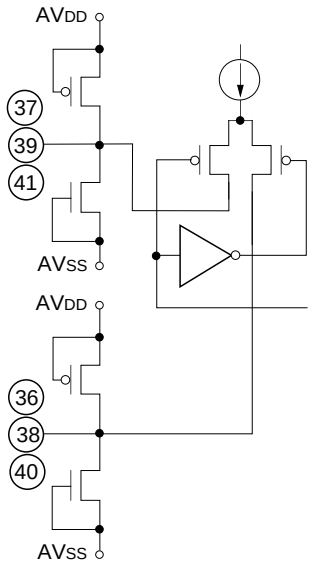
Pin Configuration



Pin Description and I/O Pins Equivalent Circuit

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	R0 to R7		Digital input
9 to 16	G0 to G7		
17 to 24	B0 to B7		
25	BLK		Blanking pin. No signal at "H" (Output 0V). Output condition at "L".
32	VB		Connect a capacitor of about 0.1µF.

Pin No.	Symbol	Equivalent circuit	Description
27	RCK		Clock pin.
28	GCK		
29	BCK		
30, 31	DVSS		Digital GND.
33	AVSS		Analog GND.
26	$\overline{CE}$		Chip enable pin. No signal (Output 0V) at "H" and minimizes power consumption.
35	IREF		Connect a resistance 16 times "16R" that of output resistance value "R".
34	VREF		Set full scale output value.
42	VG		Connect a capacitor of about 0.1µF.

Pin No.	Symbol	Equivalent circuit	Description
43 to 46	AV_{DD}		Analog V_{DD}.
37	RO		Current output pin. Voltage output can be obtained by connecting a resistance.
39	GO		
41	BO		
36	$\overline{RO}$		Inverted current output pin. Normally dropped to analog GND.
38	$\overline{GO}$		
40	$\overline{BO}$		
47, 48	DV_{DD}		Digital V_{DD}.

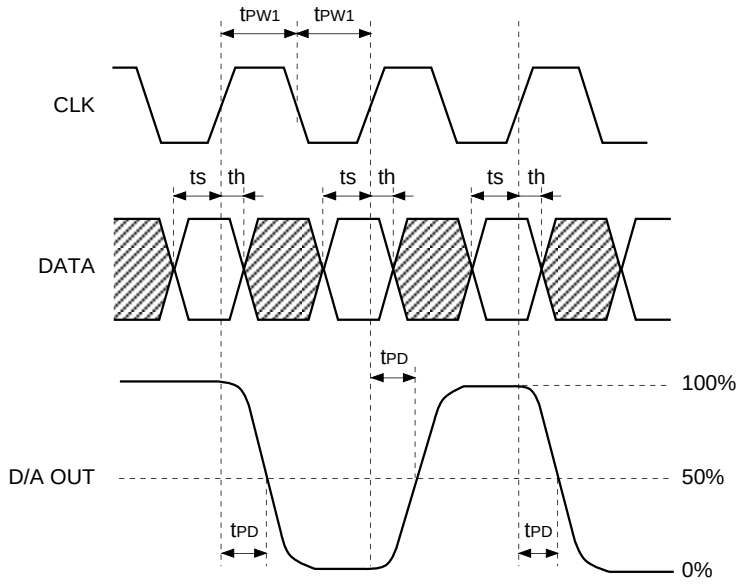
Electrical Characteristics (f_{CLK} = 20MHz, V_{DD} = 3.3V, R_{OUT} = 330Ω, V_{REF} = 1.2V, R_{IRF} = 5.1kΩ, Ta = 25°C)

Item		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}		20			MSPS
Linearity error		E_L		–2.5		2.5	LSB
Differential linearity error		E_D		–0.5		0.5	LSB
Full scale output voltage		V_{FS}		1.12	1.24	1.36	V
Full scale output ratio *1		F_{SR}		0	1.5	3	%
Full scale output current		I_{FS}			3.8		mA
Offset output voltage		V_{OS}				1	mV
Power supply current		I_{DD}	14.3MHz, at COLOR BAR DATA input		15		mA
Digital input current	H level	I_{IH}				5	µA
	V level	I_{IL}		–5			µA
Set up time		t_S		7			ns
Hold time		t_H		3			ns
Propagation delay time		t_{PD}			20		ns
Glitch energy		GE			150		pV-s
Crosstalk		CT	1MHz Sin WAVE OUTPUT		53		dB

*1 Full scale output ratio = $\left| \frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right| \times 100\ (\%)$

Description of Operation

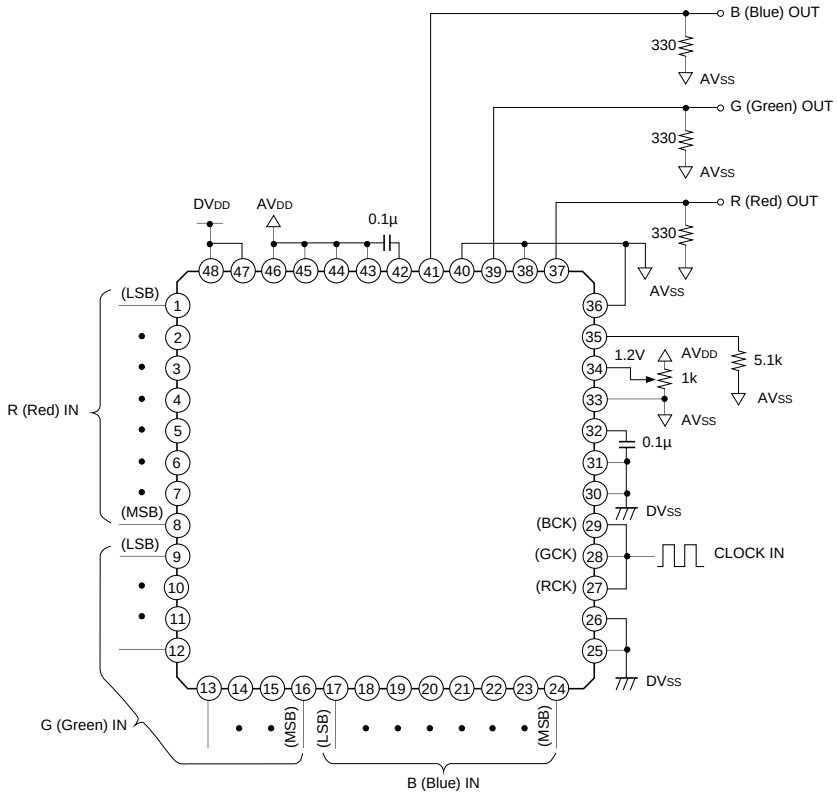
Timing Chart



I/O Chart (When full scale output voltage at 1.2V)

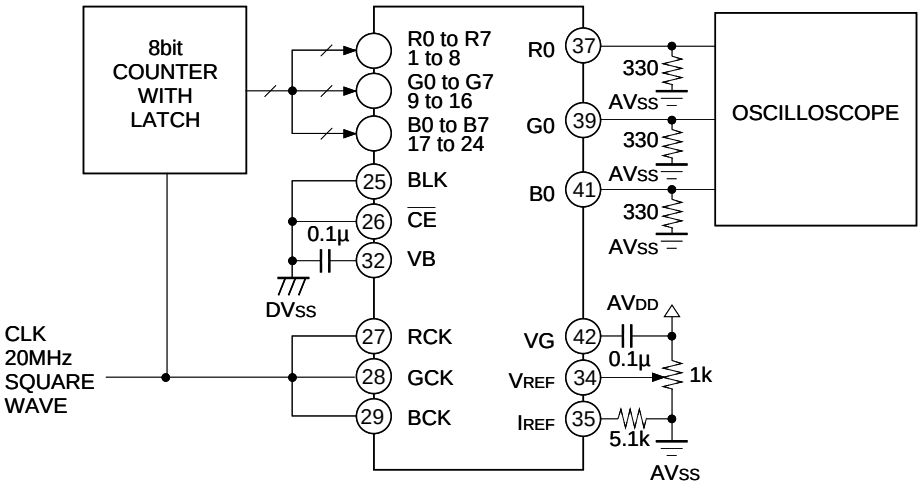
Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1	1.2V
:	
1 0 0 0 0 0 0 0	0.6V
:	
0 0 0 0 0 0 0 0	0V

Application circuit

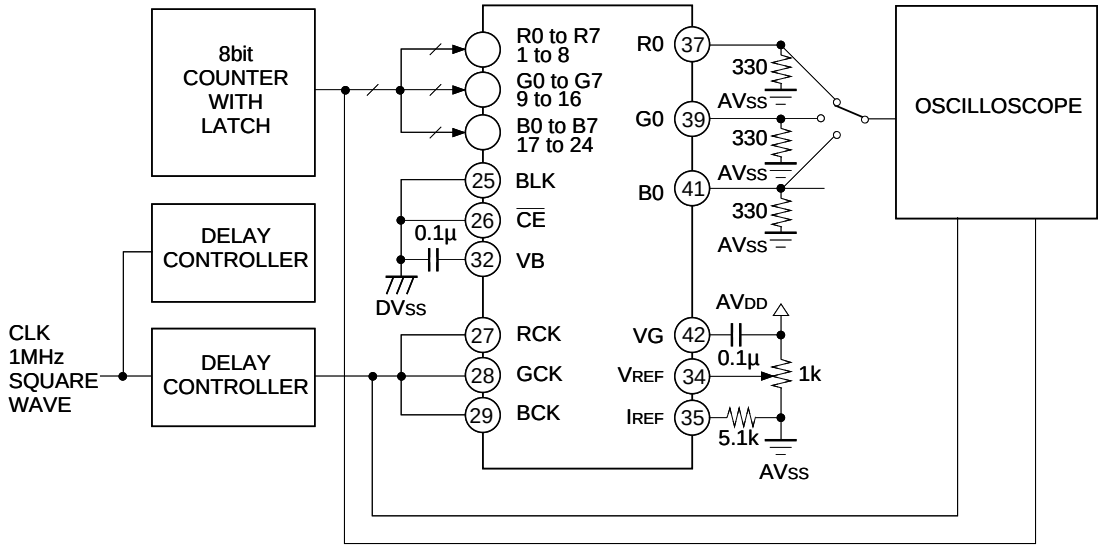


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

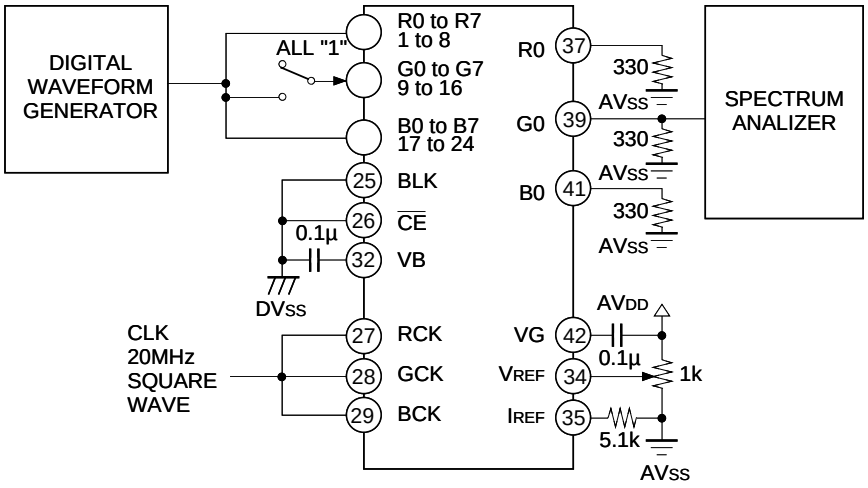
Maximum conversion velocity test circuit



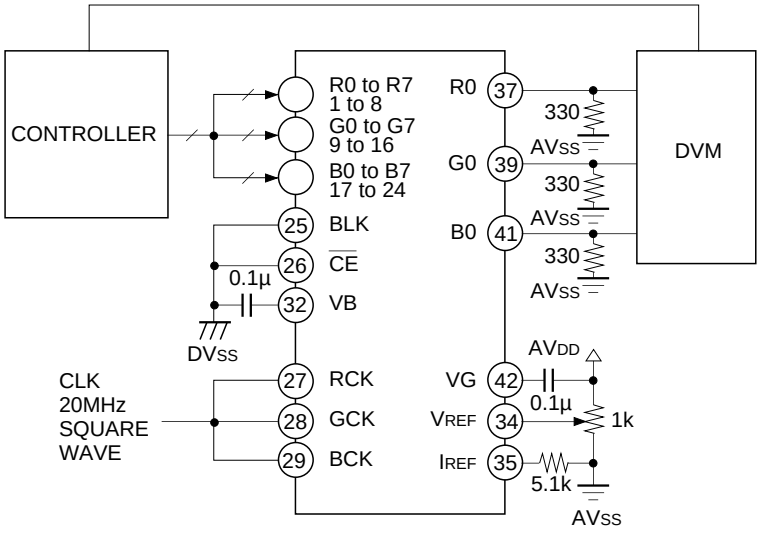
Set up hold time
Glitch energy **Test circuit**



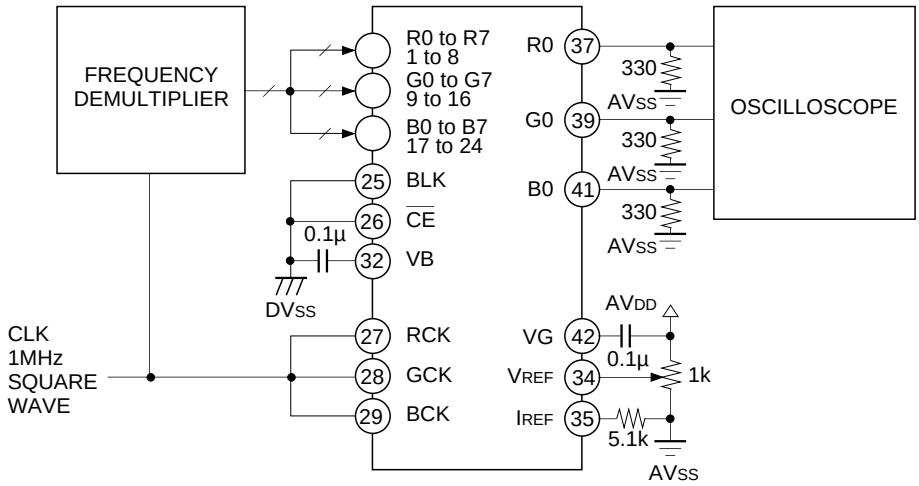
Crosstalk test circuit (Fig. 1)



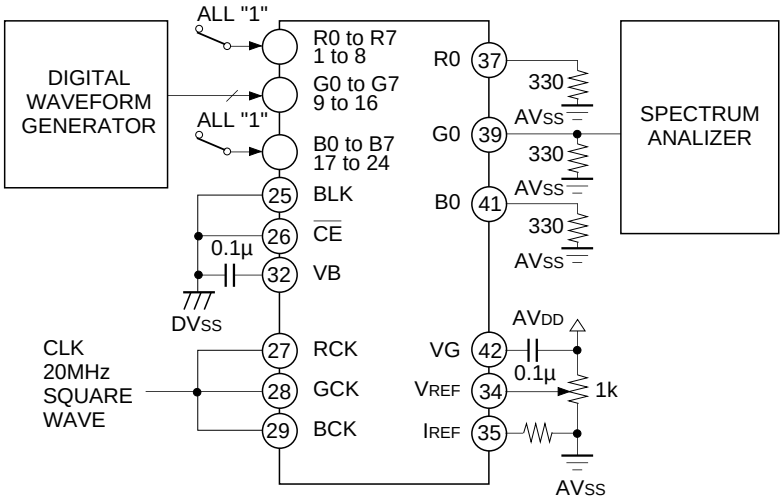
DC characteristics test circuit



Propagation delay time test circuit



SNR test circuit (Fig. 2)



SNR: Difference between primary component and secondary distortion

Example of Representative Characteristics

Fig. 1. Crosstalk

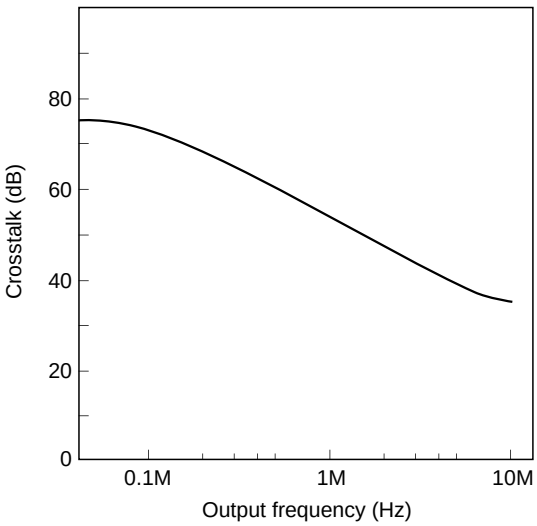


Fig. 2. SNR (Difference between primary component and secondary distortion)

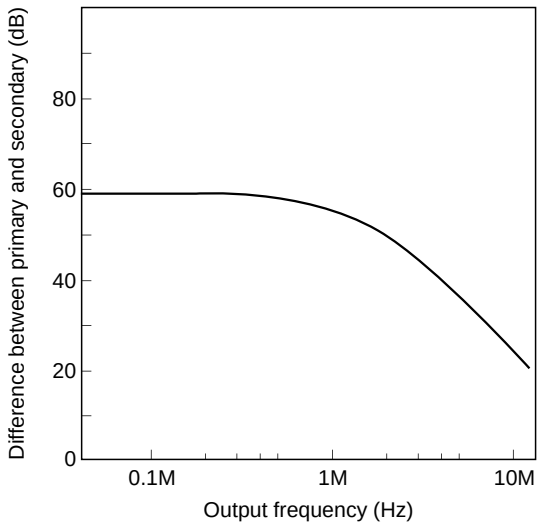


Fig. 3. Output full scale voltage vs. Ambient temperature

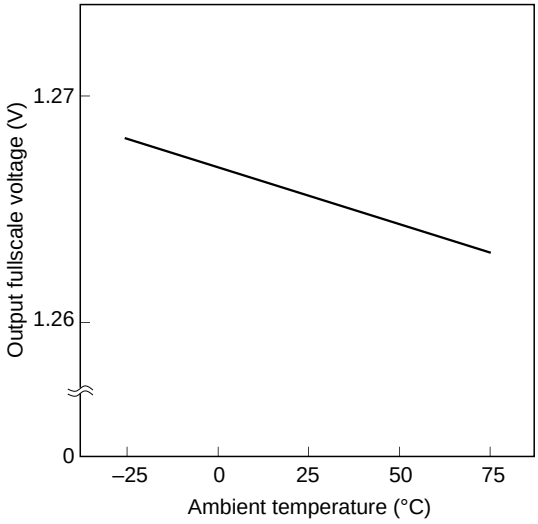


Fig. 4. Output frequency vs. Current consumption

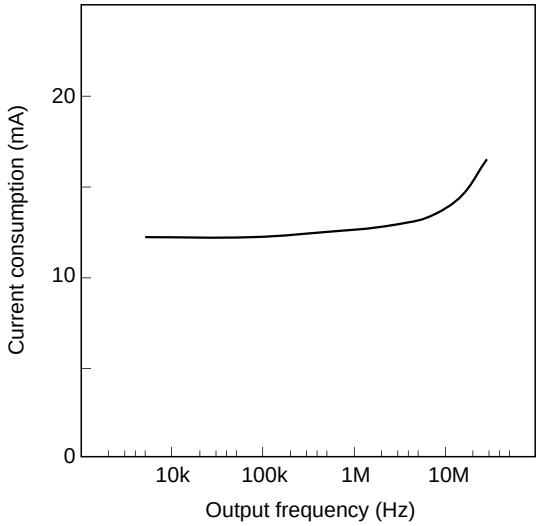
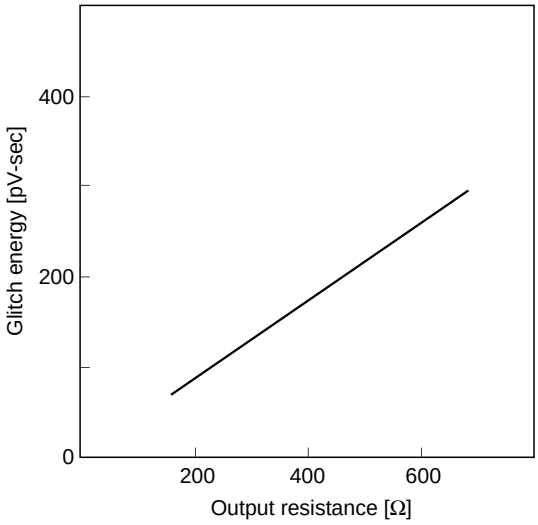


Fig. 5. Output resistance vs. Glitch energy



Reference measurement condition and description

- AV_{DD} = 3.3V
- DV_{DD} = 3.3V
- V_{REF} = 1.2V
- R_{IRF} = 5.1kΩ
- Ta = 25°C
- Fig. 1, 2 Refer to the measurement circuit.
- Fig. 3 is input data = all 1
- Fig. 4 is input data = output of incrimental counter, Current consumption is total of 3ch.

Notes on Operation

• How to select the output resistance

The CXD2304R is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin (R0, G0, B0). For specifications we have;

Output full scale voltage V_{FS} = 1.2 [V]

Output full scale current I_{FS} = 3.8 [mA]

Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF} \times 16R/R'$. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data setting time will inversely increase. Set the most suitable value sccording to the desired application.

• Phase relation between data and clock

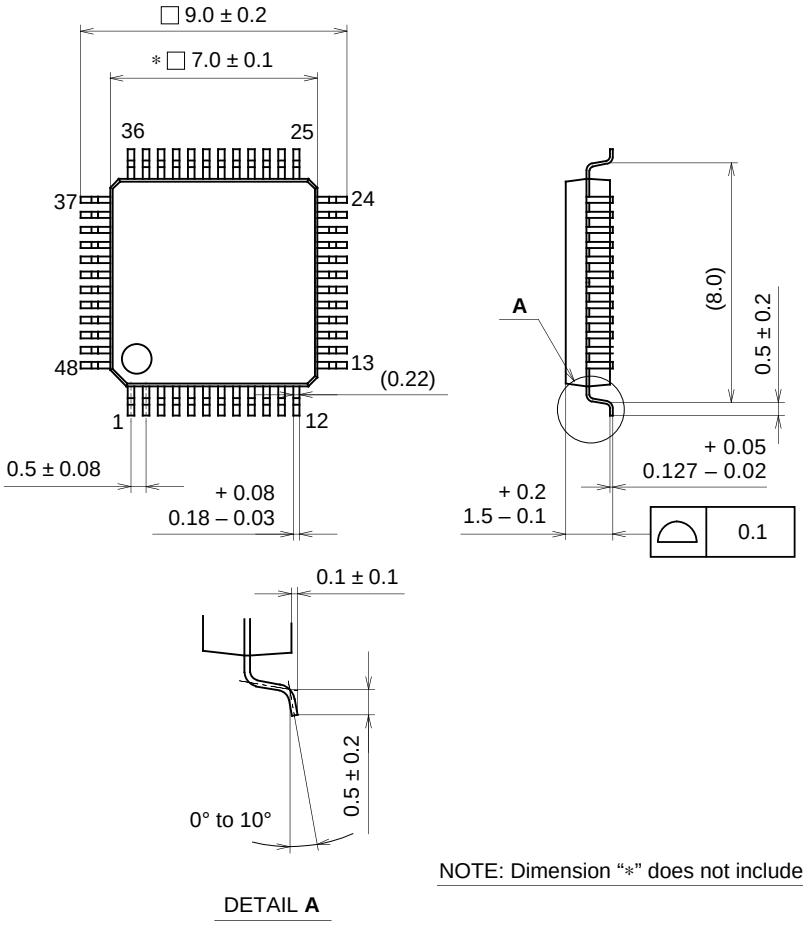
To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (ts) and hold time (th) as stipulated in the Electrical Characteristics.

• V_{DD}, V_{SS}

To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1µF, as close as possible to the pin.

Package Outline Unit : mm

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g