SONY

CXD2721Q-1

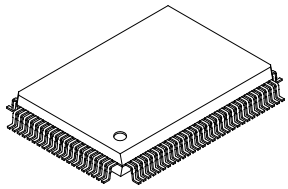
Single-Chip Digital Signal Processor for Karaoke

For the availability of this product, please contact the sales office.

Description

The CXD2721Q-1 is a Karaoke LSI suitable for use in video CD/LD/CD-G/CD and the like. A large capacity DRAM and AD/DA converters are built in, and a Karaoke mode providing simple surround and Karaoke functions such as key control, microphone echo and voice cancelling, and a music mode providing functions such as surround, parametric equalizer and bass/treble tone control are contained on a single chip.

100 pin QFP (Plastic)



Features

- 3-channel 1-bit AD converter, decimation filter and prefilter operational amplifier
  - S/N ratio: 92dB
  - THD + N: 0.02%
  - Filter pass band ripple: ±0.5dB or less
  - Filter stop band attenuation: –41dB or less
  - (all characteristics are typical values)
- 2-channel 1-bit DA converter, oversampling filter and post filter
  - S/N ratio: 97dB
  - THD + N: 0.005%
  - Filter pass band ripple: ±0.2dB or less
  - Filter stop band attenuation: –41dB or less
  - (all characteristics are typical values)
- In addition to analog I/O, digital I/O (2-channel input/2-channel output) are provided.
  The interface also supports a wide variety of formats.
- 128K-bit DRAM for key control, microphone echo and surround processing

Functions

- Key controller pitch settings can be varied to a maximum of ±1 octave with a precision of 14 bits.
- Microphone echo delay time can be varied to a maximum of 278ms (when Fs = 44.1kHz).
- Voice canceller supports settings other than center using panpot volumes.
- Voice parametric equalizer
- Voice pitch shifter
- Mixing function to support sound multiplexing software
- Digital de-emphasis function
- Simple surround function
- Music mode (switches with Karaoke mode)
  Compressor function
  Parametric equalizer function
  Surround function
  Bass/treble tone control function

Structure

Silicon gate CMOS

Applications

Equipment with Karaoke functions, such as video CD/LD/CD-G/CD, compact music centers, video games, etc.

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} +0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.25 (5.0 typ.)	V
• Operating temperature	Ta	–20 to +75	°C

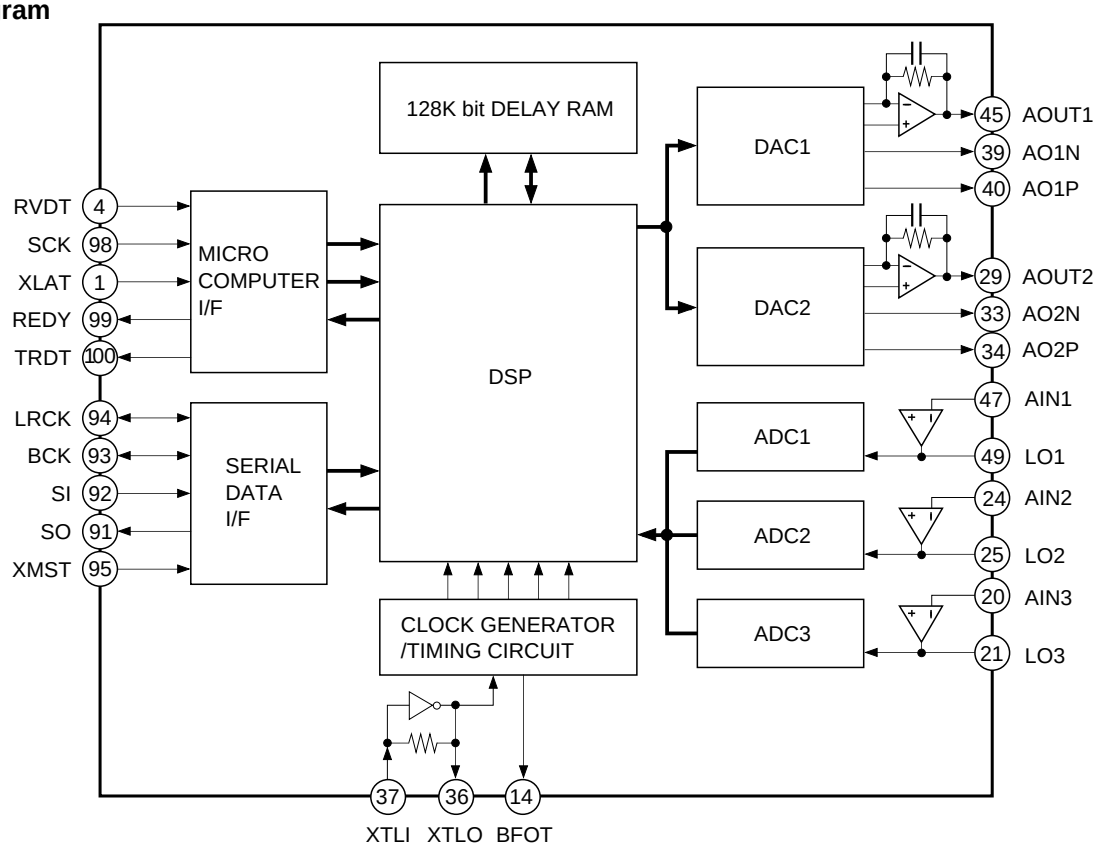
I/O Capacitance

• Input capacitance	C_{IN}	9 (max.)	pF
• Output capacitance	C_{OUT}	11 (max.)	pF
• I/O capacitance	$C_{I/O}$	11 (max.)	pF

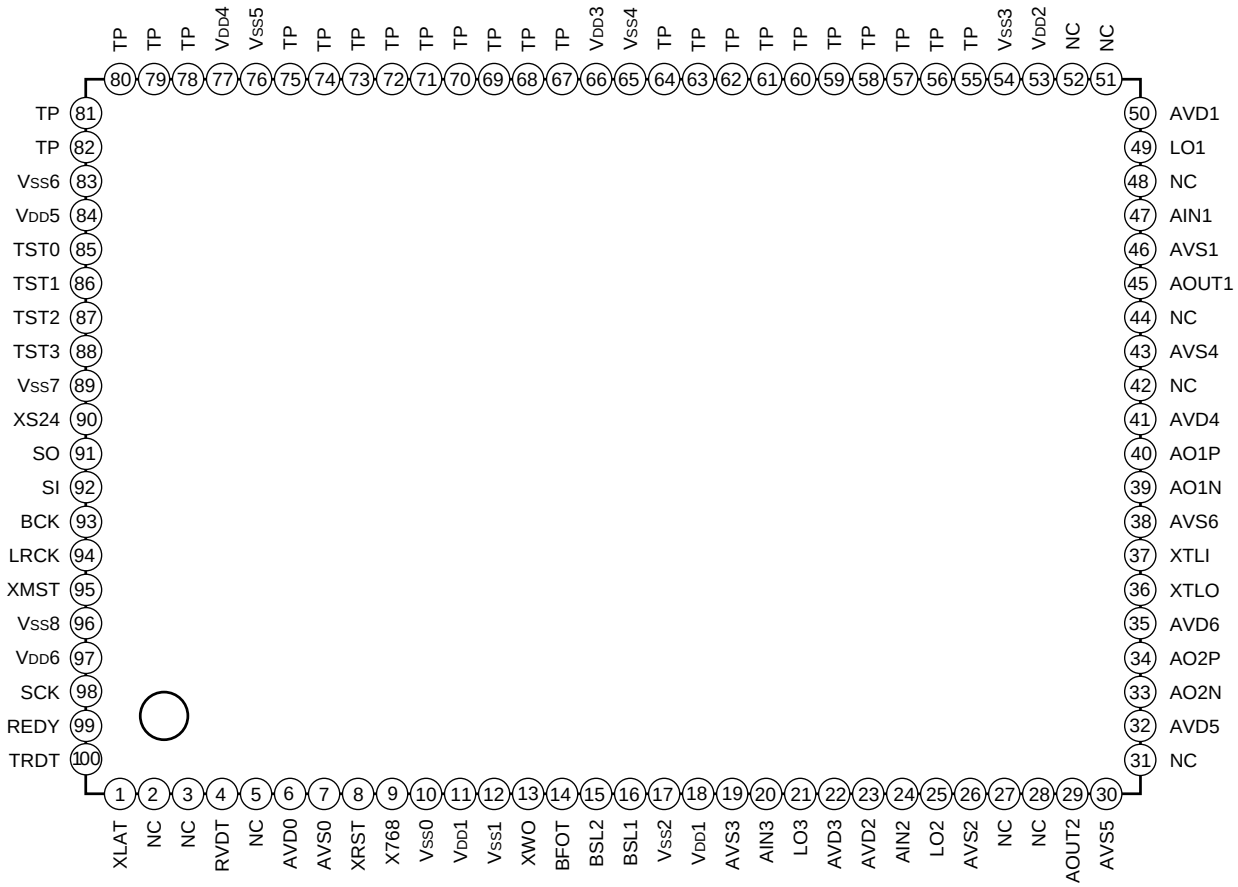
* Measurement conditions: V_{DD} = V_I = 0V, F = 1MHz

E97110A72

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	XLAT	I	Latch input for microcomputer interface.
2	NC		Open or fixed to Low.
3	NC		Open or fixed to Low.
4	RVDT	I	Data input for microcomputer interface.
5	NC		Open or fixed to Low.
6	AVD0	—	Digital power supply for built-in DRAM.
7	AVS0	—	Digital GND for built-in DRAM.
8	XRST	I	System reset input. Reset when Low.
9	X768	I	Test input pin. Normally fixed to Low.
10	$V_{SS}0$	—	Digital GND.
11	$V_{DD}1$	—	Digital power supply.
12	$V_{SS}1$	—	Digital GND.
13	XWO	I	Normally fixed to High.
14	BFOT	O	Clock, frequency divider output. (384/768/256/512fs)
15	BSL2	I	BFOT output clock frequency division ratio setting.
16	BSL1	I	BFOT output clock frequency division ratio setting.
17	$V_{SS}2$	—	Digital GND.
18	$V_{DD}1$	—	Digital power supply.
19	AVS3	—	CH3 AD converter GND.
20	AIN3	I	CH3 AD converter analog input. (for microphone input)
21	LO3	O	CH3 AD converter LPF operational amplifier inverted output. (for microphone input)
22	AVD3	—	CH3 AD converter power supply.
23	AVD2	—	CH2 AD converter power supply.
24	AIN2	I	CH2 AD converter analog input.
25	LO2	O	CH2 AD converter LPF operational amplifier inverted output.
26	AVS2	—	CH2 AD converter GND.
27	NC		Open or fixed to Low.
28	NC		Open or fixed to Low.
29	AOUT2	O	CH2 DA converter LPF output.
30	AVS5	—	CH2 DA converter GND.
31	NC		Open or fixed to Low.
32	AVD5	—	CH2 DA converter power supply.
33	AO2N	O	CH2 DA converter analog reversed phase output. (PWM)
34	AO2P	O	CH2 DA converter analog forward phase output. (PWM)
35	AVD6	—	Analog power supply for master clock.

Pin No.	Symbol	I/O	Description
36	XTLO	O	Crystal oscillator circuit output.
37	XTLI	I	Crystal oscillator circuit input.
38	AVS6	—	Analog GND for master clock.
39	AO1N	O	CH1 DA converter analog reversed phase output. (PWM)
40	AO1P	O	CH1 DA converter analog forward phase output. (PWM)
41	AVD4	—	CH1 DA converter power supply.
42	NC		Open or fixed to Low.
43	AVS4	—	CH1 DA converter GND.
44	NC		Open or fixed to Low.
45	AOUT1	O	CH1 DA converter LPF output.
46	AVS1	—	CH1 AD converter GND.
47	AIN1	I	CH1 AD converter analog input.
48	NC		Open or fixed to Low.
49	LO1	I	CH1 AD converter analog input. LPF operational amplifier inverted output.
50	AVD1	—	CH1 AD converter power supply.
51	NC		Open or fixed to Low.
52	NC		Open or fixed to Low.
53	$V_{DD}2$	—	Digital power supply.
54	$V_{SS}3$	—	Digital GND.
55	TP	O	Test monitor pin. Normally Low output. Leave open.
56	TP	O	Test monitor pin. Normally Low output. Leave open.
57	TP	O	Test monitor pin. Normally Low output. Leave open.
58	TP	O	Test monitor pin. Normally Low output. Leave open.
59	TP	O	Test monitor pin. Normally Low output. Leave open.
60	TP	O	Test monitor pin. Normally Low output. Leave open.
61	TP	O	Test monitor pin. Normally Low output. Leave open.
62	TP	O	Test monitor pin. Normally Low output. Leave open.
63	TP	O	Test monitor pin. Normally Low output. Leave open.
64	TP	O	Test monitor pin. Normally Low output. Leave open.
65	$V_{SS}4$	—	Digital GND.
66	$V_{DD}3$	—	Digital power supply.
67	TP	O	Test monitor pin. Normally Low output. Leave open.
68	TP	O	Test monitor pin. Normally Low output. Leave open.
69	TP	O	Test monitor pin. Normally Low output. Leave open.
70	TP	O	Test monitor pin. Normally Low output. Leave open.

Pin No.	Symbol	I/O	Description
71	TP	O	Test monitor pin. Normally Low output. Leave open.
72	TP	O	Test monitor pin. Normally Low output. Leave open.
73	TP	O	Test monitor pin. Normally Low output. Leave open.
74	TP	O	Test monitor pin. Normally Low output. Leave open.
75	TP	O	Test monitor pin. Normally Low output. Leave open.
76	$V_{SS}5$	—	Digital GND.
77	$V_{DD}4$	—	Digital power supply.
78	TP	O	Test monitor pin. Normally Low output. Leave open.
79	TP	O	Test monitor pin. Normally Low output. Leave open.
80	TP	O	Test monitor pin. Normally Low output. Leave open.
81	TP	O	Test monitor pin. Normally Low output. Leave open.
82	TP	O	Test monitor pin. Normally Low output. Leave open.
83	$V_{SS}6$	—	Digital GND.
84	$V_{DD}5$	—	Digital power supply.
85	TST0	I	Test pin. Normally fixed to Low.
86	TST1	I	Test pin. Normally fixed to Low.
87	TST2	I	Test pin. Normally fixed to Low.
88	TST3	I	Test pin. Normally fixed to Low.
89	$V_{SS}7$	—	Digital GND.
90	XS24	I	Serial data 24-/32-bit slot selection. 24-bit slot when Low. (valid for slave mode)
91	SO	O	1-sampling 2-channel serial data output.
92	SI	I	1-sampling 2-channel serial data input.
93	BCK	I/O	Serial bit transfer clock for serial I/O data SI and SO.
94	LRCK	I/O	Sampling frequency clock for serial I/O data SI and SO.
95	XMST	I	BCK, LRCK master/slave mode switching input. Master mode when Low.
96	$V_{SS}8$	—	Digital GND.
97	$V_{DD}6$	—	Digital power supply.
98	SCK	I	Shift clock input for microcomputer interface.
99	REDY	O	Transfer enabling signal output for microcomputer interface. Transfer prohibited when Low.
100	TRDT	O	Serial data output for microcomputer interface.

DC Characteristics (AVD0 to 6 = V_{DD}0 to 6 = 4.5V to 5.25V, AVS0 to 6 = V_{SS}0 to 8 = 0V, Ta = –20 to +75°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level	V_{IH}		0.7V_{DD}			V	*1, *4, *5
	Low level	V_{IL}				0.3V_{DD}	V	*1, *4, *5
Input voltage (2)	High level	V_{IH}	Schmitt input	0.8V_{DD}			V	*3
	Low level	V_{IL}				0.2V_{DD}	V	*3
Input voltage (3)		V_{IN}	Analog input	V_{SS}		V_{DD}	V	*2
Output voltage (1)	High level	V_{OH}	I_{OH} = –2.0mA	V_{DD} – 0.8			V	*6, *7, *8
	Low level	V_{OL}	I_{OL} = 4.0mA			0.4	V	*6, *7, *8, *9
Output voltage (2)	High level	V_{OH}	I_{OH} = –12.0mA	V_{DD}/2			V	*10
	Low level	V_{OL}	I_{OL} = 12.0mA			V_{DD}/2	V	*10
Input leak current (1)		I_I	V_{IH} = V_{DD}, V_{SS}	–10		10	µA	*1, *3, *5
Input leak current (2)		I_I	V_{IH} = V_{DD}, V_{SS}	–40		40	µA	*4
Output leak current		I_{OZ}	V_{IH} = V_{DD}, V_{SS}	–40		40	µA	*8, *9
Feedback resistance		R_{FB}		250k	1M	2.5M	Ω	Resistance between *5 and *10
Current consumption		I_{DD}	f_S = 44.1kHz		125	132	mA	

*1 XLAT, RVDT, X768, XWO, BSL2, BSL1, TST0 to TST3, XS24, SI, XMST, SCK

*2 AIN1, AIN2, AIN3

*3 XRST

*4 During input to bidirectional pins BCK and LRCK

*5 XTLI

*6 During output from bidirectional pins BCK and LRCK

*7 SO, BFOT

*8 TRDT

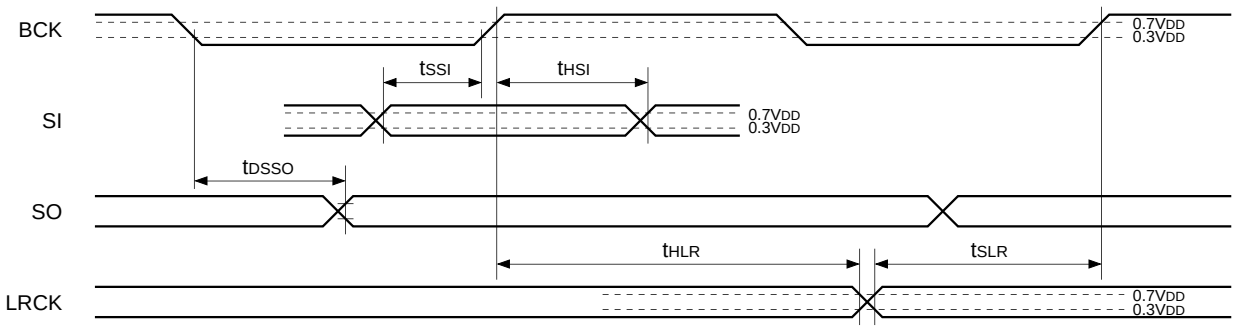
*9 REDY

*10 XTLO

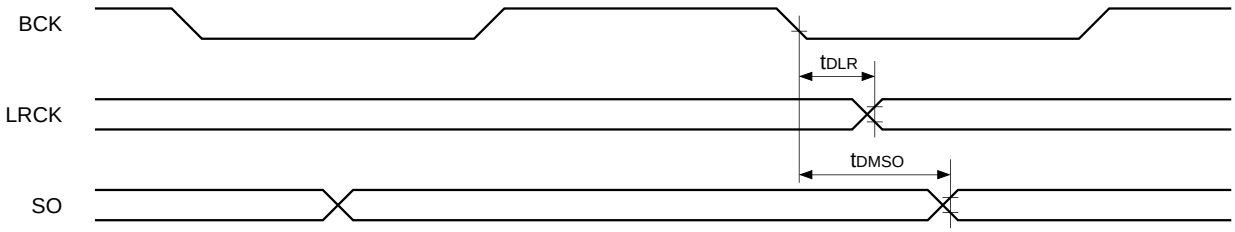
AC Characteristics (AVD0 to 6 = V_{DD}0 to 6 = 4.5V to 5.25V, AVS0 to 6 = V_{SS}0 to 8 = 0V, Ta = –20 to +75°C)

Serial Audio Interface Timing

[Slave mode]



[Master mode]

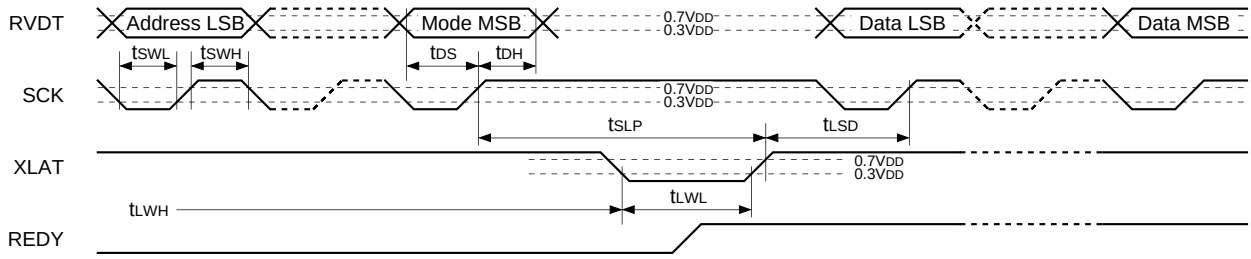


Item	Symbol	Conditions	Min.	Max.	Unit
SI setup time	t_{SSI}	Slave mode	20		ns
SI hold time	t_{HSI}	Slave mode	40		ns
SO delay time	t_{DSSO}	Slave mode, CL = 60pF		50	ns
LRCK setup time	t_{SLR}	Slave mode	20		ns
LRCK hold time	t_{HLR}	Slave mode	40		ns
LRCK delay time	t_{DLR}	Master mode, CL = 120pF		50	ns
SO delay time	t_{DMSO}	Master mode, CL = 60pF		100	ns

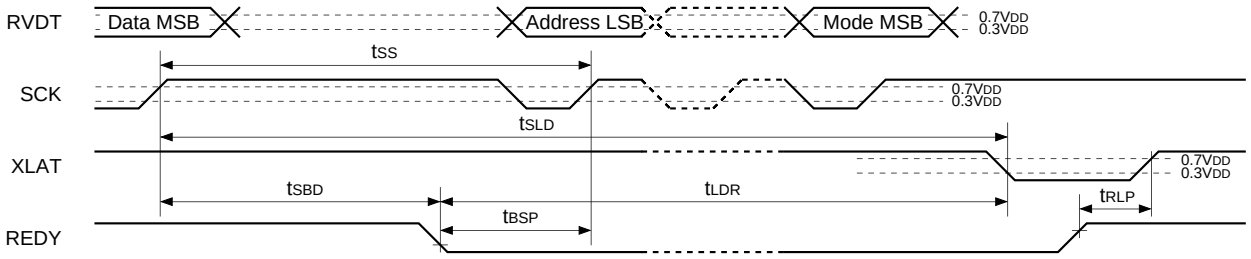
Microcomputer Interface Timing

[Write]

• Transfer timing for address section, transfer mode section and data section LSB

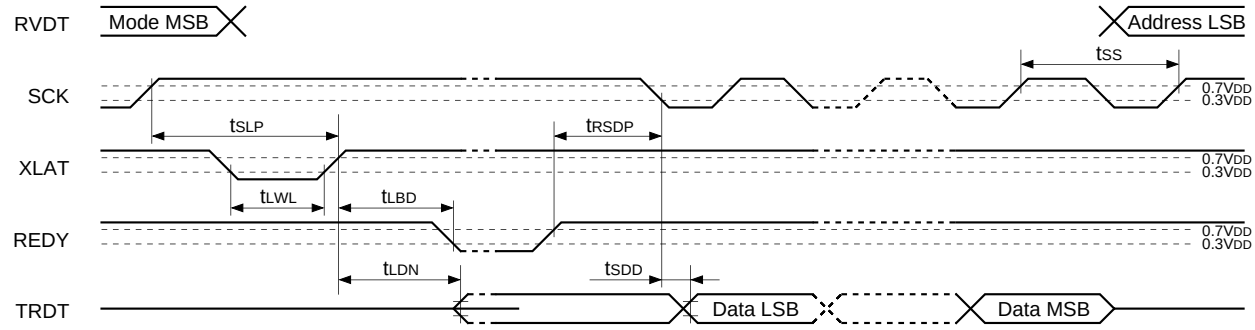


• Transfer timing from data section MSB to address section and transfer mode section



[Read]

• Transfer timing for address section and transfer mode section is the same as for write.



Item	Symbol	Min.	Max.	Unit
RVDT setup time relative to SCK rise	t_{DS}	20		ns
RVDT data hold time from SCK rise	t_{DH}	1t + 20		ns
SCK Low level width	t_{SWL}	1t + 20		ns
SCK High level width	t_{SWH}	1t + 20		ns
XLAT Low level width	t_{LWL}	1t + 20		ns
XLAT High level width	t_{LWH}	1t + 20		ns
SCK rise preceding time relative to XLAT rise	t_{SLP}	20		ns
SCK rise wait time relative to XLAT rise	t_{LSD}	3t + 20		ns
Delay time to REDY fall relative to XLAT rise	t_{LBD}		3t + 50	ns
Delay time to REDY fall relative to SCK rise	t_{SBD}		4t + 50	ns
REDY fall preceding time relative to SCK rise	t_{BSP}	20		ns
REDY rise preceding time relative to XLAT rise	t_{RLP}	20		ns
REDY rise preceding time relative to SCK fall	t_{RSDP}	20		ns
XLAT fall wait time relative to SCK rise	t_{SLD}	3t + 20		ns
XLAT fall delay time relative to REDY fall	t_{LDR}	20		ns
Delay time from XLAT rise until TRDT data becomes active	t_{LDN}		3t + 80	ns
Delay time from SCK rise until TRDT data becomes high-impedance	t_{SDF}		3t + 80	ns
Delay time from SCK fall until TRDT data is established	t_{SDD}		2t + 70	ns
SCK rise wait time for next transfer	t_{SS}	2t + 40		ns

Note 1) t is the cycle of 2/3 the clock frequency applied to the XTLI pin. (512fs)

Note 2) REDY and TRDT pins are the values for CL = 60pF.

Analog Characteristics (AVD0 to 6 = V_{DD}0 to 6 = 5.0V, AVS0 to 6 = V_{SS}0 to 8 = 0.0V,
DSP: each function = OFF, gain = 1, Ta = 25°C)

1. ADC + DAC Connection Total Characteristics

Total characteristics using the measurement circuit in Fig. 1, including the prefilter with built-in operational amplifier and the built-in post filter. Unless otherwise specified, the measurement conditions are as given below.

- IN ....0dB (= 2.0Vrms), 1kHz
- fs 44.1kHz

Item	Measurement conditions	Min.	Typ.	Max.	Unit
S/N ratio	EIAJ (with "A" weighting filter)	82	92		dB
THD + N*1	EIAJ (0dB)		0.1		%
	EIAJ (–1dB)		0.02		
	EIAJ (–10dB)		0.013	0.03	
Dynamic range	EIAJ		91		dB
Channel separation			95		dB
Level difference between channels			0.1		dB
ADC input level*2			1.33		Vrms
Output level*3			1.0		Vrms
Analog current consumption			27		mA

*1 See Graph 1.

*2 Input level to the ADC which outputs FS. (= prefilter output level)

*3 Prefilter gain = –3.52dB

2. DAC Characteristics

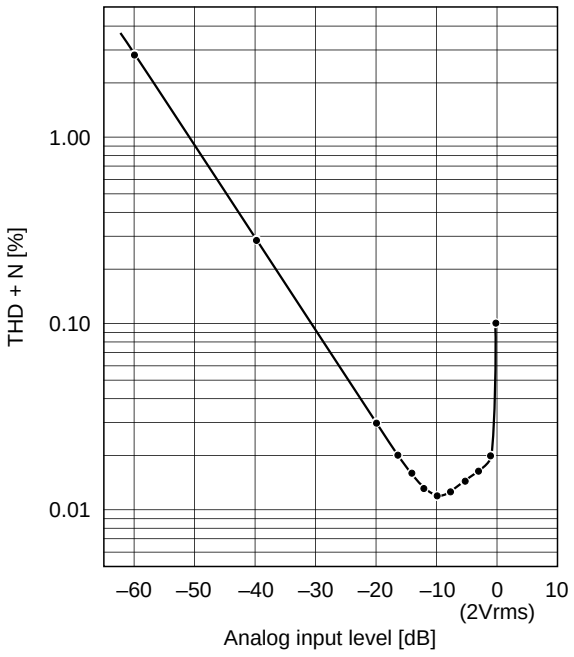
Characteristics using the measurement circuit in Fig. 2, including the built-in post filter. Unless otherwise specified, the measurement conditions are as given below.

- DATA ....0dB (= FS), 1kHz, 16bit
- fs 44.1kHz

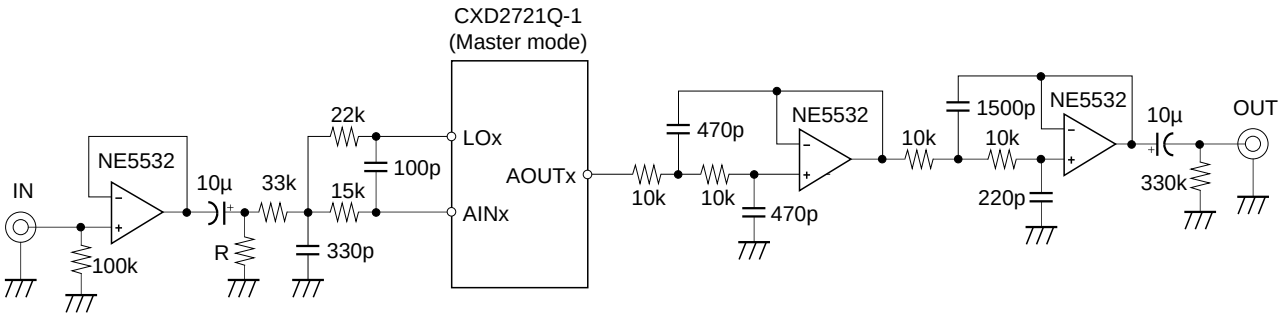
Item	Measurement conditions	Min.	Typ.	Max.	Unit
S/N ratio	EIAJ (with "A" weighting filter)		97		dB
THD + N	EIAJ (0dB)		0.009		%
	EIAJ (–1dB)		0.005		
Dynamic range	EIAJ (–60dB)		94		dB
Channel separation	EIAJ		118		dB
Level difference between channels	EIAJ		0.05		dB
Output level	EIAJ		1.11		Vrms

3. Filter Characteristics

Block	Item	Min.	Typ.	Max.	Unit
Prefilter	Feedback resistance value	10			kΩ
	Maximum amplification ratio (100kHz or less)			20	dB
Post filter	Load resistance value	10			kΩ
	Cut-off frequency (= fc)		90		kHz



Graph 1.



CH	AD1	AD2	AD3	Unit
R	∞ (= open)	∞ (= open)	1M	Ω

Fig. 1. ADC + DAC Measurement Circuit

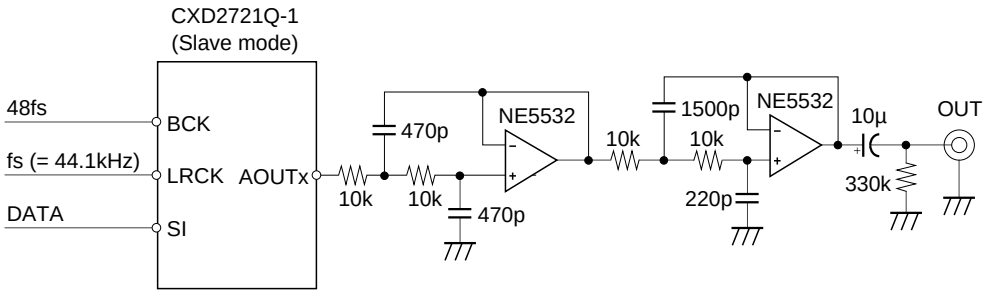


Fig. 2. DAC Measurement Circuit

Description of Functions

1. Master/Slave Modes

[Relevant pins] XMST, LRCK, BCK

When connecting multiple CXD2721Q-1 or when using this LSI as a pair with a DA converter such as the CXD2558M, one of the CXD2721Q-1 should be set to master mode to supply LRCK and BCK.

The clock applied to LRCK and BCK in slave mode must be synchronized to either the crystal oscillator clock of the XTLI and XTLO pins or the external clock input from the XTLI pin.

XMST	Mode	LRCK, BCK I/O
H	Slave mode	Input
L	Master mode	Output

Table 1-1. LRCK, BCK Mode Setting

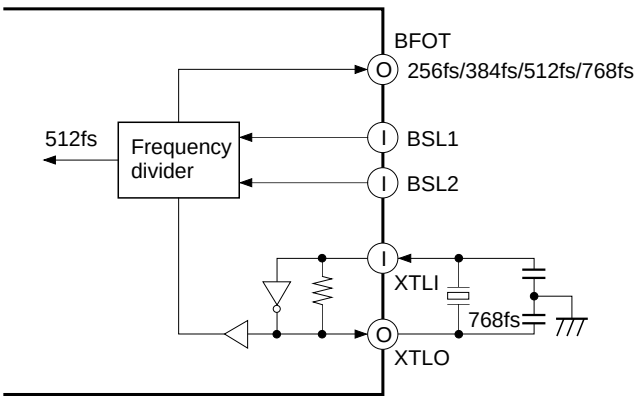
2. Master Clock System

[Relevant pins] XTLI, XTLO, BFOT, BSL1, BSL2

768fs (fs = 44.1kHz) is assumed for the master clock system and the connection is as shown below. BFOT outputs the clock obtained by frequency dividing the master clock. The frequency division ratio can be changed by BSL1 and BSL2.

BSL2	BSL1	BFOT
0	0	384fs
0	1	768fs
1	0	256fs
1	1	512fs

(1) Master



(2) Slave

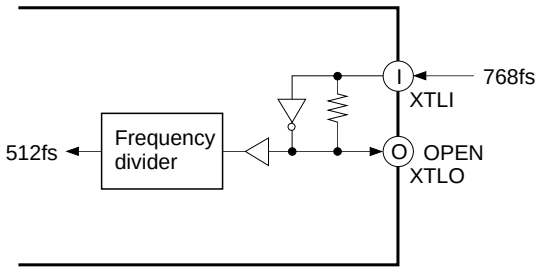


Fig. 2-1.

3. Reset Circuit

[Relevant pins] XRST, XTLI, XTLO

This LSI must be reset after the power is turned on.

Reset is performed by setting the XRST pin Low for 1/Fs or more after the supply voltage satisfies the recommended operating condition, and the crystal oscillator clock of the XTLI and XTLO pins or the external clock input from the XTLI pin is correctly applied.

4. Serial Audio Interface (SIF)

[Relevant pins] SI, SO, BCK, LRCK, XS24, XMST

Serial data is used for the external communication of the digital audio data.

The CXD2721Q-1 has one system each for input and output, and each system inputs/outputs 2 channels of data per 1 sampling cycle. Either the 32-bit clock mode or the 24-bit clock mode can be selected. In master mode, the setting is fixed to 32-bit clock mode.

(1) Pin Configuration

The pins shown in the table below are assigned to the SIF.

Symbol	I/O	Function
SI	I	Serial input; taken synchronized to BCK.
SO	O	Serial output; output synchronized to BCK.
BCK	I/O	BCK I/O; either 32-bit clock mode (64fs) or 24-bit clock mode (48fs). BCK output supports 32-bit clock mode only.
LRCK	I/O	LRCK I/O (1fs).
XS24	I	SI0 slot number (24/32) selection input. Low: 24-bit slot; High: 32-bit slot. Valid only in slave mode.
XMST	I	BCK, LRCK master mode/slave mode switching input. Low: master mode; High: slave mode.

Table 4-1. Pin Configuration

(2) Operating Modes

LRCK/BCK mode and SI/SO system settings can be selected by the setup register settings as follows.

LRCK/BCK Mode Settings

Setup register	Function	Contents
SQ11	LRCK format	"0": normal, "1": IIS
SQ10	LRCK polarity selection	"0": Lch "H", "1": Lch "L"
SQ09	BCK polarity selection relative to LRCK edge	"0": edge ↓, "1": edge ↑

Table 4-2. LRCK/BCK Mode Settings

SI/O System Register Settings

SI system

Setup register	Function	Contents
SQ08	SI data order	"0": MSB first, "1": LSB first
SQ07	SI frontward/rearward truncation	"0": Frontward truncation, "1": Rearward truncation
SQ06 SQ05	SI data word length SI data word length	SQ06 SQ05 0 0 : 16 bits 0 1 : 18 bits 1 0 : 20 bits 1 1 : 24 bits

Table 4-3. SI System Register Settings

SO system

Setup register	Function	Contents
SQ04	SO data order	"0": MSB first, "1": LSB first
SQ03	SO frontward/rearward truncation	"0": Frontward truncation, "1": Rearward truncation
SQ02 SQ01	SO data word length	SQ02 SQ01 0 0 : 16 bits 0 1 : 18 bits 1 0 : 20 bits 1 1 : 24 bits

Table 4-4. SO System Register Settings

(3) SIF Format

The serial interface has one input/output system each, and except for the slot number, the following formats can be set independently for the input and output systems by setting the setup register. The serial interface can also be made to support IIS format, to enable connection to Philips and other devices. The timing charts for each data format are shown on pages 18 and 19.

32-bit slot (XS24 = High)

SI format \ Setup register			SQ05	SQ06	SQ07	SQ08
MSB first	16 bits	Frontward truncation	0	0	0	0
MSB first	18 bits	Frontward truncation	1	0	0	0
MSB first	20 bits	Frontward truncation	0	1	0	0
MSB first	24 bits	Frontward truncation	1	1	0	0
MSB first	16 bits	Rearward truncation	0	0	1	0
LSB first	16 bits	Rearward truncation	0	0	1	1
LSB first	18 bits	Rearward truncation	1	0	1	1
LSB first	20 bits	Rearward truncation	0	1	1	1
LSB first	24 bits	Rearward truncation	1	1	1	1

Table 4-5. 32-bit Slot Serial IN

SO format \ Setup register			SQ01	SQ02	SQ03	SQ04
MSB first	16 bits	Rearward truncation	0	0	1	0
MSB first	18 bits	Rearward truncation	1	0	1	0
MSB first	20 bits	Rearward truncation	0	1	1	0
MSB first	24 bits	Rearward truncation	1	1	1	0
MSB first	24 bits	Frontward truncation	1	1	0	0
LSB first	24 bits	Rearward truncation	1	1	1	1

Table 4-6. 32-bit Slot Serial OUT

24-bit slot (XS24 = Low)

SI format \ Setup register			SQ05	SQ06	SQ07	SQ08
MSB first	16 bits	Rearward truncation	0	0	1	0
MSB first	16 bits	Frontward truncation	0	0	0	0
MSB first	18 bits	Frontward truncation	1	0	0	0
MSB first	20 bits	Frontward truncation	0	1	0	0
MSB first	24 bits		1	1	0	0
LSB first	16 bits	Rearward truncation	0	0	1	1
LSB first	18 bits	Rearward truncation	1	0	1	1
LSB first	20 bits	Rearward truncation	0	1	1	1
LSB first	24 bits		1	1	1	1

Table 4-7. 24-bit Slot Serial IN

SO format \ Setup register			SQ01	SQ02	SQ03	SQ04
MSB first	16 bits	Rearward truncation	0	0	1	0
MSB first	18 bits	Rearward truncation	1	0	1	0
MSB first	20 bits	Rearward truncation	0	1	1	0
MSB first	24 bits		1	1	*	0
LSB first	24 bits		1	1	*	1

Table 4-8. 24-bit Slot Serial OUT

Note) * means "don't care".

Digital Audio Data Input Timing (with polarities: SQ11 = 0, SQ10 = 0, SQ09 = 0)

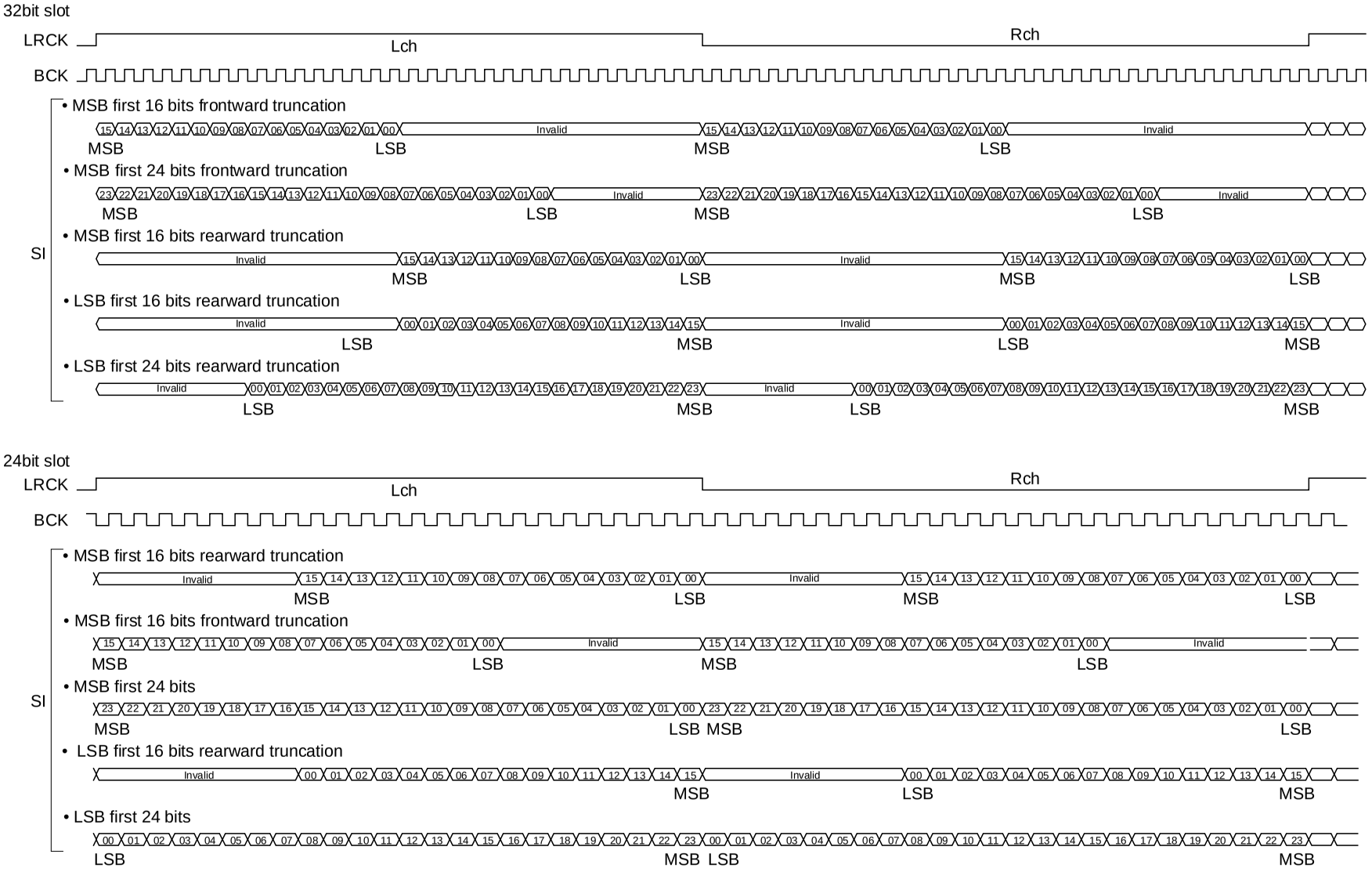


Fig. 4-1.

Digital Audio Data Output Timing (with polarities: SQ11 = 0, SQ10 = 0, SQ09 = 0)

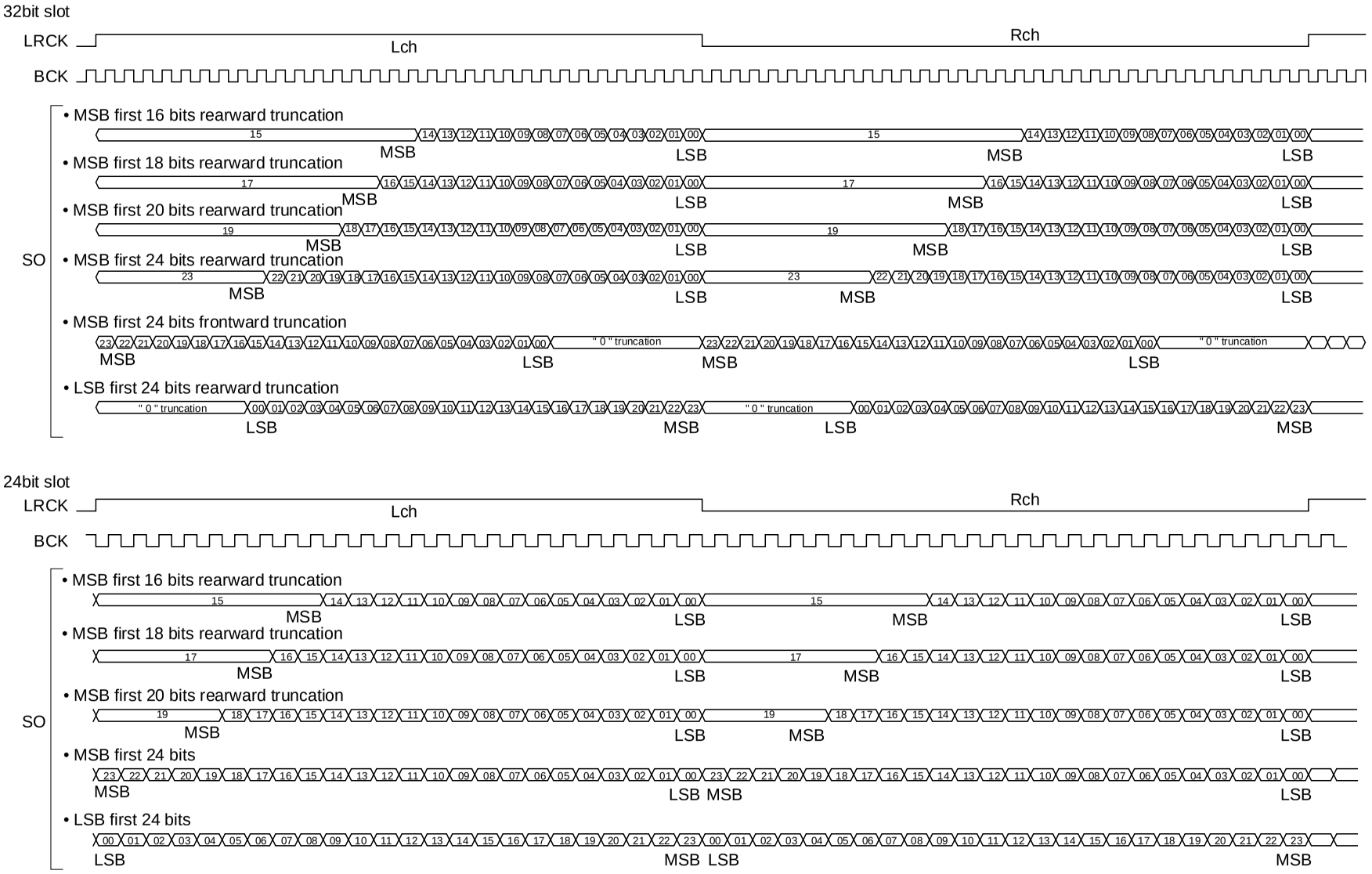


Fig. 4-2.

5. Microcomputer Interface

[Relevant pins] RVDT, TRDT, SCK, XLAT, REDY

The CXD2721Q-1 performs the serial audio interface format setting and coefficient settings such as volume and microphone echo delay amount by serial data from the microcomputer.

Further, bidirectional communication such as internal data read from the CXD2721Q-1 to the microcomputer can be performed at the rate of once per 1 LRCK.

(1) Pin Configuration

The five external pins indicated in the table below are assigned to the microcomputer interface.

The microcomputer interface begins operation when XLAT is received, so multiple CXD2721Q-1 can be used by connecting RVDT, TRDT, SCK and REDY in common and controlling (wiring) only XLAT separately.

Symbol	I/O	Function
RVDT	I	Serial data input from microcomputer.
TRDT	O	Serial data output to the microcomputer. High impedance status unless this pin is set to internal data read status by the microcomputer. Therefore, pull-up or pull-down should be performed so that the potential is not unstable when this pin is not active.
SCK	I	Shift clock for serial data. Input data from RVDT is taken according to the SCK rise, and output data from TRDT is sent out according to the SCK fall.
XLAT	I	Interprets the 8 bits of RVDT before this signal rises as transfer mode data, and the bits before that as address data.
REDY	O	Transfer prohibited when Low level. Transfer enabled when High. This pin is an open drain, and must be pulled up externally.

Table 5-1. Microcomputer Interface External Pins

(2) Description of Communication Formats

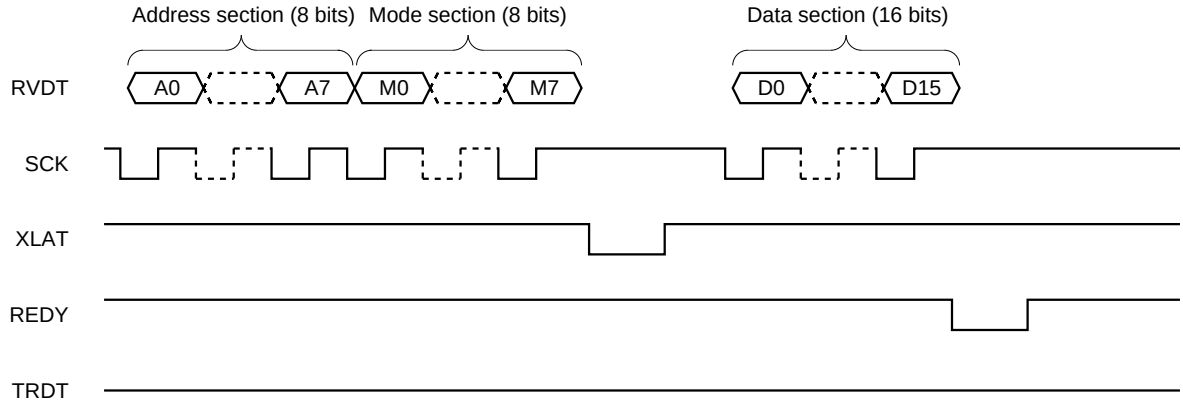
The data transfer timing between the microcomputer interface and the coefficient RAM and setup register is called the SV cycle, and is generated once per 1 LRCK.
The SV cycle is generated immediately preceding the signal processing program, so it has absolutely no effect on signal processing, and there is no risk of the sound being cut.

In read/write modes,

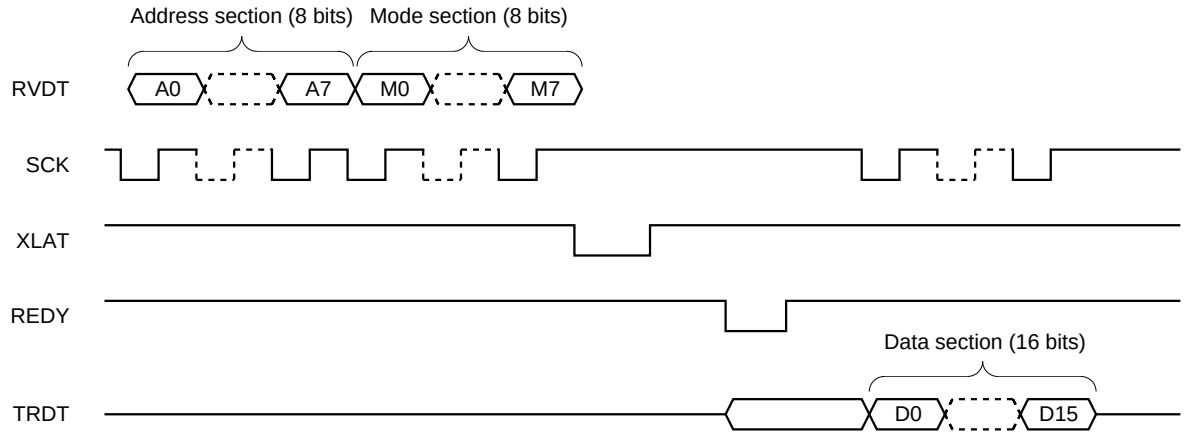
Address section + Mode section + Data section

act as one package of data to perform data transfer between the microcomputer and the CXD2721Q-1.

[Write] • For coefficient RAM



[Read] • For coefficient RAM



Note) For both read and write, the data section is 24 bits for the setup register.

Fig. 5-1. Examples of Communication

(3) Data Structure

The data structure is classified into three types as shown in the table below. All data communication is performed with LSB first.

Symbol	Bit length	Contents	Remarks
A0 to A7	8	Address section	
M0 to M7	8	Transfer mode section	
D0 to D15/SQ00 to SQ23	16/24	Data section	Coefficient RAM is 16 bits; setup register is 24 bits

Table 5-2. Data Structure

(3)-1. Transfer Mode Section

The transfer mode section is 8 bits and has the following functions.

Bit	Symbol	Function	
M7	XVMT	SO Mute	0: ON (No sound) 1: OFF
M6		Reserve	
M5			
M4	VS1	Data type	VS1 VS0 0 0 Setup register (Setup Register) 1 0 Coefficient RAM (K-RAM)
M3	VS0		
M2		Reserve	
M1			
M0	VRD	Receive/Send	0: Receive 1: Send **Note)** Polarity as seen from the CXD2721Q-1

Table 5-3. Transfer Mode Section

(3)-2. Address Section

The coefficient RAM has a 192-word structure, so the address section is 8 bits. The setup register has a 1-word structure, so the address section data may be optional.

(3)-3. Data Section

The coefficient RAM has a 16-bit structure (D0 to D15), so 16 SCK are required. The setup register has a 24-bit structure (SQ00 to SQ23), so 24 SCK are required.

(4) Details of Communication Methods

The definitions of signal timing required for control from the microcomputer are given below.

(4)-1. Write

First, address and mode section data are sent from the microcomputer, synchronized with SCK, to the RVDT pin.
The address section data is 8 bits for both the coefficient RAM and setup register. The setup register has a 1-word length, so optional data can be transferred. Address section data is transferred with LSB first.
Mode section data is fixed at 8 bits regardless of the transfer contents.

The phase relationship between SCK and RV data (data applied to the RVDT pin) has the following restrictions:

- RV data must be established before SCK rises ($t_{DS} \geq 20$ns).
- RV data must be held for 1t + 20ns or more after SCK rises (t_{DH}).

SCK itself has the following restrictions:

- SCK Low level must be 1t + 20ns or more (t_{SWL}).
- SCK High level must also be 1t + 20ns or more (t_{SWH}).

After SCK rises, which corresponds to the final mode section data, XLAT rises ($t_{SLP} \geq 20$ns). The XLAT Low level width must be maintained at 1t + 20ns or more (t_{LWL}). Further, fall timing restrictions are:

- For the preceding transfer, if REDY falls due to SCK, as for write, 3t + 20ns or more is required (t_{SLD}).
- For the preceding transfer, if REDY falls due to XLAT, as for read, 20ns or more is required (t_{LDR}).

Further, if preceding transfers have been performed and REDY = Low, XLAT must wait for REDY = High before rising.

The procedure until this point is the same for write and read.

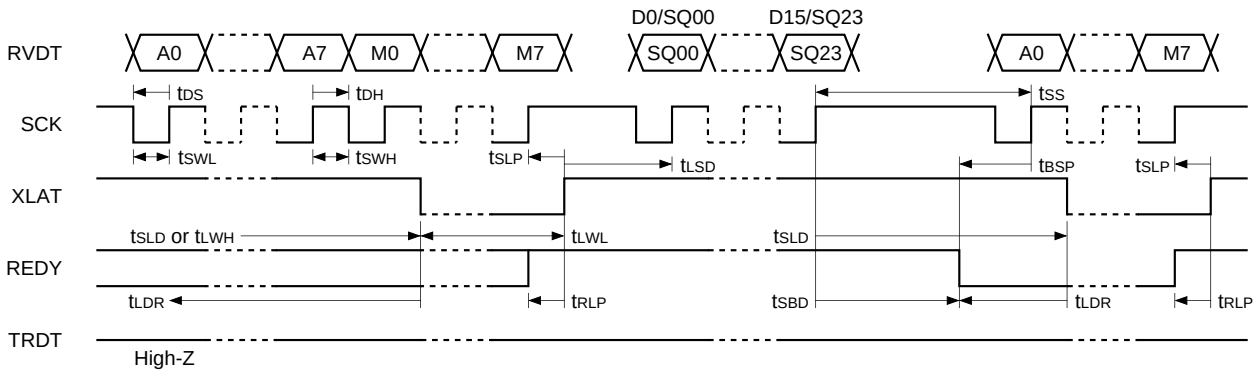


Fig. 5-2. Write Timing

Data section write begins after XLAT rises, and here also transfer must be performed with LSB first, with t_{DS} and t_{DH} restrictions. In addition, after XLAT rises at the starting point for sending to the data section, wait for 3t + 20ns or more for the first SCK rise (t_{LSD}).

When 16 bits (coefficient RAM) or 24 bits (setup register) of this write is repeated, REDY goes Low within 4t + 50ns, and the microcomputer is informed of waiting status for the SV cycle, which is the dedicated data rewrite cycle, by the microcomputer interface (t_{SBD}).
When REDY goes High again, the corresponding data is written.

The next communication can be restarted by using the REDY signal as follows.

- When REDY = Low, SCK can rise for the next transfer ($t_{BSP} \geq 20$ns).
- Similarly, when REDY = Low, XLAT can fall for the next transfer ($t_{LDR} \geq 20$ns).

REDY will fall due to this communication, but it is prohibited for XLAT to rise for the next transfer before REDY rises. Be sure that the next XLAT rises after REDY rises ($t_{RLP} \geq 20$ns).

In order to restart the next transfer without using the REDY signal, the following conditions must be observed.

- There should be 2t + 40ns or more left between the SCK rise for the final data section and the SCK rise for the next transfer (t_{SS}).
- Similarly, XLAT can fall for the next transfer after waiting 3t + 20ns or more after the final data section SCK rise (t_{SLD}).

The t_{SS} and t_{SLD} here are shorter times than $t_{SBD} \leq 4t + 50$ns, so these are rather loose restrictions. However, even in this case the XLAT rise for the next transfer must come after REDY rises ($t_{RLP} \geq 20$ns).

Further, the restriction for the XLAT fall at the starting point of this write from t_{SLD} can be:

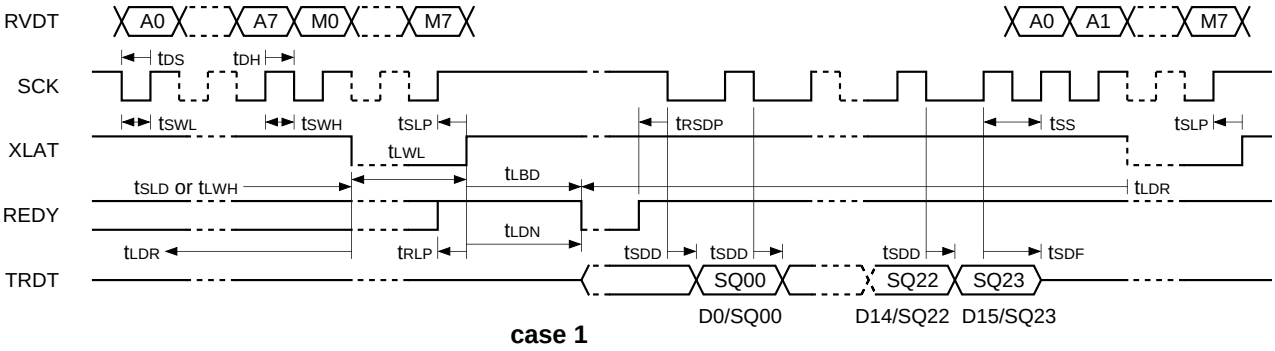
- $t_{SLD} \geq 3t + 20$ns if the preceding transfer was "write".

(4)-2. Read

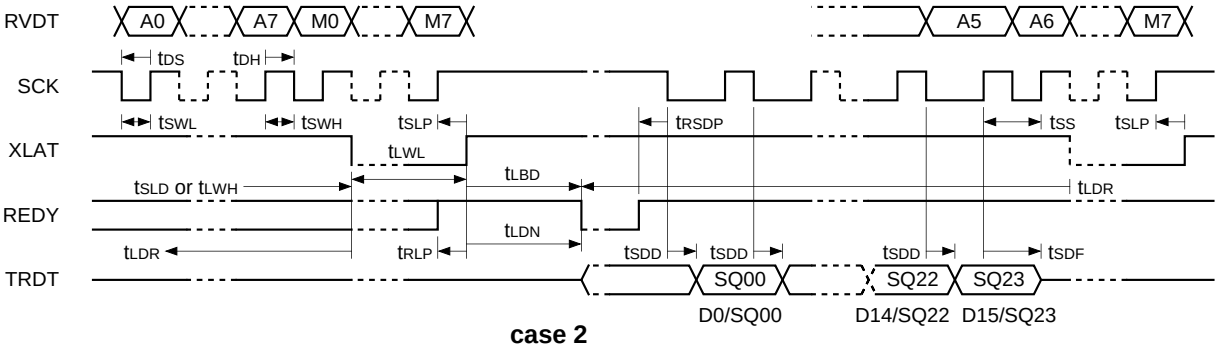
First, address and mode section data are transferred synchronized to SCK, and XLAT rises together with this. The procedure until this point is the same as for write, so the description is omitted here.

Read differs from write in that after XLAT rises, REDY falls within 3t + 50ns (t_{LBD}), and the microcomputer is informed of SV cycle waiting.
At this time, the TRDT pin changes from high-impedance status to active status ($t_{LDN} \leq 3t + 80ns$) simultaneously with the fall of REDY. When the read data is ready, the REDY pin changes from Low to High. When the data read out from the TRDT pin is made TR, and SCK falls ($t_{RSDP} \geq 20ns$) when the REDY pin goes High, the first TR data is established within 2t + 70ns (t_{SDD}). The microcomputer reads this data at the SCK rise. The TR data is read in order from the LSB with 16 bits for the coefficient RAM and 24 bits for the setup register by adding SCK. When all the corresponding data is read, read is completed.

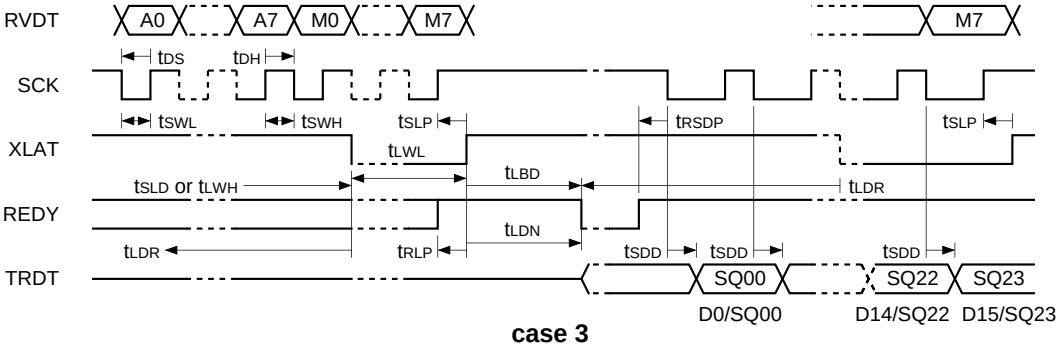
Next, the method for restarting transfer after read is completed is described.
As in Case 1, there is a method for sending address and mode section data consecutively after reading all of the 16- or 24-bit data. 2t + 40ns or more should be left between the SCK rise for the final data read and the next SCK rise (t_{SS}), and this is established by the conditions $t_{SWL} \geq 1t + 20ns$ and $t_{SWH} \geq 1t + 20ns$. Further, at this read REDY changes from High to Low, but it is prohibited for the XLAT for the next transfer to fall before this. If REDY = Low has been established, XLAT can fall ($t_{LDR} \geq 20ns$).
Also, while 16- or 24-bit data is being read from the TRDT pin, address and mode section data writing to the RVDT pin for the next transfer can be started.
In Case 3, the final section of read data and the final data in the mode section overlap, and this allows shifting to the next transfer processing in the shortest possible time after data read.
It is also possible to have data read and address and mode section write overlap partially, as shown by Case 2.



case 1



case 2



case 3

Fig. 5-3. Read Timing

6. Setup Register

When the setup register is selected in the microcomputer interface transfer mode, the following settings are possible for the serial audio interface and DAC.

Data section bit	Control		When system reset is Low
SQ23 to 14, SQ12	Reserve bit	Must be Low for setup register settings to change	All Low
SQ13	DAC output selection	0: Built-in LPF used 1: External LPF used (PWM output)	Built-in LPF
SQ11	LRCK format	0: Normal 1: IIS	Normal
SQ10	LRCK polarity selection	0: Lch High 1: Lch Low	Lch High
SQ09	BCK polarity selection relative to LRCK edge	0: Falling edge 1: Rising edge	Falling edge
SQ08	SI data order	0: MSB first 1: LSB first (24-bit rearward truncation only)	MSB first
SQ07	SI frontward/rearward truncation	0: Frontward truncation (valid only for MSB first/24 bits/32 slots) 1: Rearward truncation	Frontward truncation
SQ06, 05	SI data word length	SQ06 SQ05 0 0: 16 bits 0 1: 18 bits 1 0: 20 bits 1 1: 24 bits	16 bits
SQ04	SO data order	0: MSB first 1: LSB first	LSB first
SQ03	SO frontward/rearward truncation	0: Frontward truncation 1: Rearward truncation	Frontward truncation
SQ02, 01	SO data word length	SQ02 SQ01 0 0: 16 bit 0 1: 18 bit 1 0: 20 bit 1 1: 24 bit	16 bits
SQ00	DAC forced mute	0: ON 1: OFF	ON

Table 6-1.

7. Coefficient RAM Settings

When the coefficient RAM is selected in the microcomputer interface transfer mode, Karaoke mode or music mode can be selected and coefficient parameters such as each section's volume and microphone echo delay amount can be set. Coefficient RAM addresses other than those given in these specifications are "don't care".

7-1. Mode Settings

[Relevant coefficients] SW1 (address = 10H), SW2 (address = 18H), SW3 (address = 78H)

The CXD2721Q-1 functions include Karaoke mode which consists mainly of Karaoke applications and music mode which consists mainly of surround functions. Karaoke mode is further divided into two modes by the delay RAM assignment, and the delay amount can be changed by varying the microphone echo and surround decimation ratios (only for Karaoke mode). The settings for each mode are as follows.

Setting item / Mode	SW1 (10H)	SW2 (18H)	Key control for accompaniment	Key control for voice	Microphone echo	Surround
Karaoke mode 0	0000H	0000H	32K bits	8K bits	64K bits	24K bits
Karaoke mode 1	0000H	8000H	56K bits	8K bits	64K bits	
Music mode	8000H	—	—	—	—	128K bits

Fig. 7-1-1. Operating Modes and Built-in Delay RAM Assignments

Setting item / Mode	SW1 (10H)	SW2 (18H)	SW3 (78H)	Microphone echo			Surround		
				Decimation ratio	Band (kHz)	Maximum delay (ms)	Decimation ratio	Band (kHz)	Maximum delay (ms)
Karaoke mode 0	0000H	0000H	0000H	1/2	Approxi-mately 8	Approxi-mately 185	1/1	Approxi-mately 20	Approxi-mately 35
Karaoke mode 0	0000H	0000H	8000H	1/3	Approxi-mately 6	Approxi-mately 278	1/1	Approxi-mately 20	Approxi-mately 35
Karaoke mode 1	0000H	8000H	0000H	1/2	Approxi-mately 8	Approxi-mately 185*1	1/2	Approxi-mately 8	Approxi-mately 185*1
Karaoke mode 1	0000H	8000H	8000H	1/3	Approxi-mately 6	Approxi-mately 278*1	1/3	Approxi-mately 6	Approxi-mately 278*1
Music mode	8000H	—	—	—	—	—	1/1	Approxi-mately 20	Approxi-mately 185

*1 The microphone echo and surround decimation ratios can be selected in Karaoke mode 1, and the maximum delay amount of approximately 185ms for 1/2 decimation and approximately 278ms for 1/3 decimation can be divided as desired between microphone echo and surround. For example, if a delay of 200ms is assigned to microphone echo with 1/3 decimation, the surround delay amount is 78ms.

Fig. 7-1-2. Operating Modes and Microphone Echo/Surround Settings

7-2. Karaoke Mode

Karaoke mode simultaneously provides key control, voice cancellation, microphone echo, voice pitch shifter, voice PEQ, simple surround and other functions.

(1) Fixed Values for System Initialization

When the system is initialized, the coefficient RAM must be set to the fixed values shown below for internal operation.

Address	Fixed value	Address	Fixed value	Address	Fixed value
01H	68A9H	3CH	0000H	A5H	F72AH
02H	5121H	48H	2000H	A6H	0A4EH
03H	0000H	49H	0B00H	A7H	2706H
10H	0000H	4AH	1500H	A8H	34EEH
13H	8B2AH	4BH	1FF0H	AAH	6000H
14H	3BF7H	4CH	8000H	ABH	FF80H
15H	38DFH	4DH	0000H	ACH	00A1H
16H	4E77H	52H	0008H	ADH	016EH
17H	2E90H	58H	82EAH	AEH	01F8H
1AH	0000H	6BH	8000H	AFH	0193H
1CH	4000H	79H	5555H	B0H	0024H
20H	0010H	7AH	0000H	B1H	FE70H
21H	4000H	7CH	AAAAH	B2H	FDBAH
27H	8000H	7DH	0008H	B3H	FED8H
28H	0000H	7EH	0010H	B4H	015AH
2DH	0008H	9BH	0092H	B5H	037FH
30H	0000H	9CH	0209H	B6H	0344H
31H	0000H	9DH	02CDH	B7H	FFFFH
32H	8000H	9EH	0109H	B8H	FB5CH
33H	0000H	9FH	FDA0H	B9H	F8E3H
34H	0000H	A0H	FD19H	BAH	FBF6H
35H	0000H	A1H	0189H	BBH	0575H
36H	0000H	A2H	058AH	BCH	129CH
37H	0000H	A3H	016DH	BDH	1E0DH
38H	8000H	A4H	F7BEH	BEH	2294H

Table 7-2-1. Coefficient Setting Values for Karaoke Mode Initialization

Note) Consult your Sony representative with regard to use at other than fs = 44.1kHz, as the fixed values change.

(2) Setting Data

The relationships between the coefficient RAM and each function during DSP operation are as follows.

Address	Symbol	Function	Setting value
00H	Ki	SI data input level control	See Table 7-2-9
04H	Ke	De-emphasis ON/OFF	ON = ac19H OFF = 0000H
05H	DC1a1	DC cut1 coefficient for accompaniment	See Table 9-1
06H	DC1a0	DC cut1 coefficient for accompaniment	See Table 9-1
07H	DC1b	DC cut1 coefficient for accompaniment	See Table 9-1
08H	KisLm	SI CH1 data → Lch mix	See Table 7-2-9
09H	KisRc	SI CH2 data → Lch mix	See Table 7-2-9
0AH	KiaLm	ADC CH1 data → Lch mix	See Table 7-2-9
0BH	KiaRc	ADC CH2 data → Lch mix	See Table 7-2-9
0CH	KisRm	SI CH2 data → Rch mix	See Table 7-2-9
0DH	KisLc	SI CH1 data → Rch mix	See Table 7-2-9
0EH	KiaRm	ADC CH2 data → Rch mix	See Table 7-2-9
0FH	KiaLc	ADC CH1 data → Rch mix	See Table 7-2-9
10H	SW1	Karaoke/music mode switch	Karaoke mode=0000H,Music mode=8000H
11H	PL	Panpot volume for voice cancellation	See Table 7-2-3
12H	PR	Panpot volume for voice cancellation	See Table 7-2-3
18H	SW2	Karaoke mode 0/1 switch	Mode 0 = 0000H; mode 1 = 8000H
19H	Kvc	Voice cancellation ON/OFF	ON = 8000H OFF = 0000H
1BH	TRi	Key control setting value for accompaniment	See Table 7-2-5
1EH	TVi	Key control setting value for voice	See Table 7-2-5
22H	nRpR	Pitch ratio for accompaniment	See Table 7-2-4
23H	KWR	Key control setting value for accompaniment	See Table 7-2-5
24H	KRigh	Key control setting value for accompaniment	See Table 7-2-5
25H	KLeft	Key control setting value for accompaniment	See Table 7-2-5
26H	KWR-1	Key control setting value for accompaniment	See Table 7-2-5
2EH	Ks	Key control ON/OFF for accompaniment	ON = 8000H OFF = 0000H
3BH	Kimc	Microphone input level control	See Table 7-2-9
3DH	DC2a1	DC cut2 coefficient for voice	See Table 9-1
3EH	DC2a0	DC cut2 coefficient for voice	See Table 9-1
3FH	DC2b	DC cut2 coefficient for voice	See Table 9-1
40H	PEQa	PEQ coefficient for voice	See Table 9-4
41H	PEQb1	PEQ coefficient for voice	See Table 9-4
42H	PEQb2	PEQ coefficient for voice	See Table 9-4
43H	PEQg	PEQ coefficient for voice	See Table 9-5
44H	HCa1	High cut1 coefficient for voice	See Table 9-2

Table 7-2-2 (1). Coefficient RAM Setting Data for Karaoke Mode (1/3)

Note) See "8. DSP Signal Flow" regarding the symbols.

Address	Symbol	Function	Setting value
45H	HC1a0	High cut1 coefficient for voice	See Table 9-2
46H	HC1b	High cut1 coefficient for voice	See Table 9-2
47H	VnRpR	Pitch ratio for voice	See Table 7-2-4
53H	Krmd	High cut1 output mix for voice → Direct sound	See Table 7-2-9
54H	Krmpd	Pitch shifter output mix for voice → Direct sound	See Table 7-2-9
55H	Krme	High cut1 output mix for voice → Echo input	See Table 7-2-9
56H	Krmpe	Pitch shifter output mix for voice → Echo input	See Table 7-2-9
59H	Kdryd	Voice system direct sound DAC side mix	See Table 7-2-9
5AH	Keffd	Microphone echo sound DAC side mix	See Table 7-2-9
5CH	KLmd	Key control output DAC side Lch mix for accompaniment	See Table 7-2-9
5DH	KRmd	Key control output DAC side Rch mix for accompaniment	See Table 7-2-9
5EH	KLsd	Surround output DAC side Lch mix	See Table 7-2-9
5FH	KRsd	Surround output DAC side Rch mix	See Table 7-2-9
60H	KLod	System volume DAC side Lch	See Table 7-2-9
61H	KRod	System volume DAC side Rch	See Table 7-2-9
62H	Kdrys	Voice system direct sound serial out side mix	See Table 7-2-9
63H	Keffs	Microphone echo sound serial out side mix	See Table 7-2-9
65H	KLms	Key control output serial out side Lch mix for accompaniment	See Table 7-2-9
66H	KRms	Key control output serial out side Rch mix for accompaniment	See Table 7-2-9
67H	KLss	Surround output serial out side Lch mix	See Table 7-2-9
68H	KRss	Surround output serial out side Rch mix	See Table 7-2-9
69H	KLos	System volume serial out side Lch	See Table 7-2-9
6AH	KRos	System volume serial out side Rch	See Table 7-2-9
6EH	Tdoe	Microphone echo delay amount	See Table 7-2-6
6FH	Kre	Microphone echo read tap volume	See Table 7-2-9
71H	Tre	Microphone echo read tap address	See Table 7-2-6
73H	Krd	Microphone echo input sound mix	See Table 7-2-9
74H	Kfb	Microphone echo reverberation sound mix	See Table 7-2-9
75H	HC2a1	High cut2 coefficient for microphone echo	See Table 9-3
76H	HC2a0	High cut2 coefficient for microphone echo	See Table 9-3
77H	HC2b	High cut2 coefficient for microphone echo	See Table 9-3
78H	SW3	1/2, 1/3 decimation mode switch	1/2 mode = 0000H; 1/3 mode = 8000H
81H	KLri	Surround input Lch mix	See Table 7-2-9
82H	KRri	Surround input Rch mix	See Table 7-2-9
83H	Kfbs	Surround reverberation sound mix	See Table 7-2-9

Table 7-2-2 (2). Coefficient RAM Setting Data in Karaoke Mode (2/3)

Note) See "8. DSP Signal Flow" regarding the symbols.

Address	Symbol	Function	Setting value
84H	HDmp	High dump coefficient for surround	See Table 9-6
85H	KLtp1	Read tap volume Lch 1 for surround	See Tables 7-2-9 and 7-2-11
86H	KLtp2	Read tap volume Lch 2 for surround	See Tables 7-2-9 and 7-2-11
87H	KLtp3	Read tap volume Lch 3 for surround	See Tables 7-2-9 and 7-2-11
88H	KRtp1	Read tap volume Rch 1 for surround	See Tables 7-2-9 and 7-2-11
89H	KRtp2	Read tap volume Rch 2 for surround	See Tables 7-2-9 and 7-2-11
8AH	KRtp3	Read tap volume Rch 3 for surround	See Tables 7-2-9 and 7-2-11
8DH	Tdis	Delay RAM setting value for surround	See Table 7-2-7
8EH	TpL1	Read tap address Lch 1 for surround	See Table 7-2-8
8FH	TpL2	Read tap address Lch 2 for surround	See Table 7-2-8
90H	TpL3	Read tap address Lch 3 for surround	See Table 7-2-8
91H	TpR1	Read tap address Rch 1 for surround	See Table 7-2-8
92H	TpR2	Read tap address Rch 2 for surround	See Table 7-2-8
93H	TpR3	Read tap address Rch 3 for surround	See Table 7-2-8
94H	Tdos	Surround delay amount	See Table 7-2-8

Table 7-2-2 (3). Coefficient RAM Setting Data in Karaoke Mode (3/3)

Note) See "8. DSP Signal Flow" regarding the symbols.

7-2-1. Voice Canceller Settings

[Relevant coefficients] PL (address = 11H), PR (address = 12H), K_{VC} (address = 19H)

The vocal sound set at the center can be canceled by setting K_{VC} = 8000H and PL, PR = 7000H.
Voice cancelling at other than the center setting can be performed by the panpot volumes.
Panpot volume values are PL for CH1 and PR for CH2, and at the center position they are both 0.857. To turn off the voice canceller, set K_{VC} = 0000H and PL, PR = 0000H.

PL and PR setting values are hexadecimal notation with D15 as MSB and D0 as LSB.

PL	PR	Setting position	PL	PR	Setting position
7000H	7000H	Center	7000H	7000H	Center
7000H	6000H		6000H	7000H	
7000H	5000H		5000H	7000H	
7000H	4000H		4000H	7000H	
7000H	3000H		3000H	7000H	
7000H	2000H		2000H	7000H	
7000H	1000H		1000H	7000H	
7000H	0000H	CH2	0000H	7000H	CH1

Table 7-2-3. Settings for Voice Canceller Panpot Volumes

7-2-2. Key Controller Settings

[Relevant coefficients] TRi (address = 1BH), TVi (address = 1EH), nRpR (address = 22H), KWR (address = 23H), KRigh (address = 24H), KLeft (address = 25H), KWR-1 (address = 26H), Ks (address = 2EH), VnRpR (address = 47H), Krmpd (address = 55H), Krmpe (address = 56H)

(1) Key Controller Pitch Ratio

nRpR (D15, ..., D2) is 2's complement format with the decimal point between D14 and D13, and sets the desired pitch ratio directly. (VnRpR has the same type of setting as nRpR.)

$$nRpR = \sum_{n=2}^{15} Dn \times 2^{n-14}$$

The expression range for the pitch ratio is: $-2.0 \leq nRpR \leq 2.0 - 2^{-12}$

but for practical use it is: $-0.5 \leq nRpR \leq 1.0$
or ±1 octave

Use within a range of ± half an octave is recommended for quality of sound, although this depends on the aim and the source.
Also, the algorithm is such that allophones are not generated even when the nRpR setting value is changed.

(2) Notes on Key Controller OFF

The pitch does not change when nRpR and VnRpR are set to 0000H (OFF) when the key controller is OFF, but depending on the internal status during OFF, there is no guarantee that the input value will be output as is. During OFF, after setting nRpR and VnRpR to 0000H (OFF), set the pitch control section to through status with the following settings.

Accompaniment controller OFF: Ks = 0000H (OFF)

Voice key controller OFF : Krmpd = 0000H (OFF)
: Krmpe = 0000H (OFF)

(3) Pitch Ratio Setting Examples

Pitch ratio setting examples are illustrated below.

Setting values nRpR are hexadecimal notation with D15 as MSB and D2 as LSB for a total of 14 bits. (D1 and D0 can be optional data.)

CENT	nRpR	CENT	nRpR
0	0000H	0	0000H
+50	01E0H	–50	FE2EH
+100	03CEH	–100	FC69H
+150	05CAH	–150	FAB1H
+200	07D6H	–200	F905H
+250	09F1H	–250	F765H
+300	0C1BH	–300	F5D2H
+350	0E56H	–350	F44AH
+400	10A2H	–400	F2CCH
+450	12FFH	–450	F15AH
+500	156EH	–500	EFF3H
+550	17EEH	–550	EE95H
+600	1A82H	–600	ED42H
+650	1D29H	–650	EBF8H
+700	1FE4H	–700	EAB8H
+750	22B3H	–750	E980H
+800	2597H	–800	E852H
+850	2892H	–850	E72CH
+900	2BA2H	–900	E60EH
+950	2EC9H	–950	E4F9H
+1000	3208H	–1000	E3ECH
+1050	3560H	–1050	E2E6H
+1100	38D0H	–1100	E1E8H
+1150	3C5BH	–1150	E0F1H
+1200	4000H	–1200	E000H

Table 7-2-4. Pitch Ratio Setting Examples

The numeric representation format for pitch ratio here is:

$$nRpR = \sum_{n=2}^{15} Dn \times 2^{n-14}$$

The numeric representation range is: $-2.0 \leq nRpR \leq 2.0 - 2^{-12}$

Also, the relationship formula with music word cent value C is:

$$nRpR = 2^{\frac{C}{1200}} - 1,\ C = 1200 \log_2 [nRpR + 1]\ [cent]$$

The semitone at the average ratio is 100 [cent].

(4) Key Controller Settings for Each Karaoke Mode

The CXD2721Q-1 must perform the following coefficient settings for the Karaoke mode 0/1 selection.

Setting coefficient / Mode	SW1	SW2	TRi	TVi	KWR	KRigh	KLeft	KWR-1
Karaoke mode 0	0000H	0000H	2000H	4000H	4000H	1600H	2A00H	3FF0H
Karaoke mode 1	0000H	8000H	3800H	7000H	7000H	2C00H	4400H	6FF0H

Table 7-2-5. Key Controller Setting Values

7-2-3. Microphone Echo Delay Amount Setting

[Relevant coefficients] Tdoe (address = 6EH), Tre (address = 71H)

The microphone echo delay amount can be varied by setting the coefficient Tdoe (12 bits from D14 to D3) value. The relationships between the coefficient and the delay amount are shown in Table 7-2-6.

Coefficient Tre (12 bits from D14 to D3) is the microphone input echo initial delay time.
Set in the range of 0008H to Tdoe.

Setting value Tdoe	Delay (fs = 44.1kHz)	
	1/2 decimation	1/3 decimation
0008H 0010H 0018H · · · · 7FF0H 7FF8H 4095 steps	0.045ms · · · · · · · 185.714ms Approximately 0.045ms/step setting possible	0.068ms · · · · · · · 278.571ms Approximately 0.068ms/step setting possible

Table 7-2-6. Microphone Echo Delay Amount Setting

7-2-4. Surround (Karaoke Mode) Coefficient Settings

[Relevant coefficients] Tdoe (address = 6EH), Tdis (address = 8DH), TpL1 (address = 8EH), TpL2 (address = 8FH), TpL3 (address = 90H), TpR1 (address = 91H), TpR2 (address = 92H), TpR3 (address = 93H), Tdos (address = 94H)

(1) Karaoke Mode 0/1 Setting Values

The surround settings for Karaoke mode 0/1 are as follows.

Mode \ Setting coefficient	SW1	SW2	SW3	Tdis
Karaoke mode 0 (1/1 decimation)	0000H	0000H	—	5000H
Karaoke mode 1 (1/2 decimation)	0000H	8000H	0000H	Tdoe
Karaoke mode 1 (1/3 decimation)	0000H	8000H	8000H	Tdoe – 0008H

Table 7-2-7. Surround Karaoke Mode 0/1 Setting Values

(2) Delay Amount Setting

The surround (Karaoke mode) delay amount can be varied by setting the coefficient Tdos (12 bits from D14 to D3) value. However, the following restrictions apply according to the delay RAM assignment.

Karaoke mode 0: Tdis + Tdos ≤ 7FF8H

Karaoke mode 1 (1/2 decimation): Tdis + Tdos ≤ 7FF8H

Karaoke mode 1 (1/3 decimation): Tdis + Tdos ≤ 7FF0H

The relationships between the coefficient and the delay amount are shown in Table 7-2-8.

Coefficients TpL1 to 3 (12 bits from D14 to D3) and TpR1 to 3 (12 bits from D14 to D3) are the sound initial delay time. Set in the range of 0008H to Tdos.

Setting value Tdos			Delay (fs = 44.1kHz)		
	Karaoke mode 0	Karaoke mode 1	Karaoke mode 0	1/2 decimation	1/3 decimation
	1535 steps	4094 steps	1/fs per step setting possible	2/fs per step setting possible	3/fs per step setting possible
0008H	↕	↕	0.022ms	0.045ms	0.068ms
0010H			.	.	.
0018H			.	.	.
.			.	.	.
2FF8H			34.807ms	.	.
.				.	.
.				.	.
7FE8H				.	.
7FF0H				185.667ms	278.503ms

Table 7-2-8. Surround Karaoke Mode Delay Amount Setting

7-2-5. I/O Level Settings

[Relevant coefficients] Ki (address = 00H), KisLm (address = 08H), KisRc (address = 09H), KiaLm (address = 0AH), KiaRc (address = 0BH), KisRm (address = 0CH), KisLc (address = 0DH), KiaRm (address = 0EH), KiaLc (address = 0FH), Kimc (address = 3BH), Krmd (address = 53H), Krme (address = 54H), Krmpd (address = 55H), Krmpe (address = 56H), Kdryd (address = 59H), Keffd (address = 5AH), KLmd (address = 5CH), KRmd (address = 5DH), KLsd (address = 5EH), KRsd (address = 5FH), KLod (address = 60H), KRod (address = 61H), Kdrys (address = 62H), Keffs (address = 63H), KLms (address = 65H), KRms (address = 66H), KLss (address = 67H), KRss (address = 68H), KLos (address = 69H), KRos (address = 6AH), Kre (address = 6FH), Krd (address = 73H), Kfb (address = 74H), KLri (address = 81H), KRri (address = 82H), Kfbs (address = 83H), KLtp1 (address = 85H), KLtp2 (address = 86H), KLtp3 (address = 87H), KRtp1 (address = 88H), KRtp2 (address = 89H), KRtp3 (address = 8AH)

The I/O levels and volumes are 2's complement format with the decimal point between D15 and D14, and hexadecimal notation with D15 as MSB and D0 as LSB.
The coefficient and level relationships are as follows.

D15 to D0	Level
8000H	0dB
↓	↓
FFFFH	–90.31dB
0000H	–∞

Table 7-2-9. I/O Level Settings (other than Kre)

D15 to D0	Level
8000H	+12.04dB
↓	↓
FFFFH	–78.27dB
0000H	–∞

Table 7-2-10. I/O Level Settings (Kre)

The I/O levels for 8001H to FFFEH are determined by the following formulas.

$$\text{(Coefficient value)} = \left[(-1) \times D15 + \sum_{n=0}^{14} Dn \times 2^{n-15}\right] \times (-1) \text{ for other than Kre}$$

$$\text{(Coefficient value)} = \left[(-1) \times D15 + \sum_{n=0}^{14} Dn \times 2^{n-15}\right] \times (-4) \text{ for Kre}$$

$$\text{I/O level} = 20 \log [\text{coefficient value}] \text{ dB}$$

As an exception to the above I/O levels, the surround output level for Karaoke mode 1 with a decimation ratio of 1/2 is shown in Table 7-2-11.

D15 to D0	Level
8000H	+6.02dB
↓	↓
FFFFH	–84.29dB
0000H	–∞

Table 7-2-11. I/O Level Settings (exception)

Note) D15 to D0 are negative values, but the calculation is (–1) × (D15 to D0).
When you wish to invert the phase, make D15 to D0 positive values.

7-3. Music Mode

7-3-1. Fixed Values for System Initialization

When the system is initialized, the coefficient RAM must be set to the fixed values shown below for internal operation.

Address	Fixed value
01H	68A9H
02H	5121H
03H	0000H
10H	8000H
11H	82EAH
14H	8000H
20H	7FF7H
55H	0000H

Table 7-3-1.

Note) Consult your Sony representative with regard to use at other than fs = 44.1kHz, as the fixed values change.

7-3-2. Setting Data

The relationships between the coefficient RAM and each function during DSP operation are as follows.

Address	Symbol	Function	Setting value
00H	Ki	SI data input level control	See Table 7-3-5 (1)
04H	Ke	De-emphasis ON/OFF	ON/ac19H OFF/0000H
05H	DC1a1	DC cut1 coefficient	See Table 9-1
06H	DC1a0	DC cut1 coefficient	See Table 9-1
07H	DC1b	DC cut1 coefficient	See Table 9-1
08H	KisLm	SI CH1 data → Lch mix	See Table 7-3-5 (1)
09H	KisRc	SI CH2 data → Lch mix	See Table 7-3-5 (1)
0AH	KiaLm	ADC CH1 data → Lch mix	See Table 7-3-5 (1)
0BH	KiaRc	ADC CH2 data → Lch mix	See Table 7-3-5 (1)
0CH	KisRm	SI CH2 data → Rch mix	See Table 7-3-5 (1)
0DH	KisLc	SI CH1 data → Rch mix	See Table 7-3-5 (1)
0EH	LiaRm	ADC CH2 data → Rch mix	See Table 7-3-5 (1)
0FH	KiaLc	ADC CH1 data → Rch mix	See Table 7-3-5 (1)
15H	KLri	Surround input level control (Lch)	See Table 7-3-5 (1)
16H	KRri	Surround input level control (Rch)	See Table 7-3-5 (1)

Table 7-3-2 (1). Coefficient RAM Setting Data (1/4)

Note) See "8. DSP Signal Flow" regarding the symbols.

Address	Symbol	Function	Setting value
17H	k	Compressor coefficient	See Table 7-3-3
18H	XthP	Compressor coefficient	See Table 7-3-3
19H	XthM	Compressor coefficient	See Table 7-3-3
1AH	Ksd	Compressor ON/OFF	ON/8000H OFF/0000H
1BH	Kse	PEQ ON/OFF	ON/8000H OFF/0000H
1CH	Kdry	Direct sound mix	See Table 7-3-5 (1)
1DH	KLeff	Surround output (Lch) mix	See Table 7-3-5 (1)
1EH	KReff	Surround output (Rch) mix	See Table 7-3-5 (1)
1FH	Kst	Tone control ON/OFF	ON/8000H OFF/0000H
21H	Ap	Compressor coefficient	See Table 7-3-3
22H	Am	Compressor coefficient	See Table 7-3-3
23H	Bp	Compressor coefficient	See Table 7-3-3
24H	Bm	Compressor coefficient	See Table 7-3-3
25H	Cp	Compressor coefficient	See Table 7-3-3
26H	Cm	Compressor coefficient	See Table 7-3-3
27H	Khr	PEQ input level control	See Table 7-3-5 (1)
28H	a0/4	PEQ1 coefficient	See Table 9-7
29H	a1/4	PEQ1 coefficient	See Table 9-7
2AH	a2	PEQ1 coefficient	See Table 9-7
2BH	b1/4	PEQ1 coefficient	See Table 9-7
2CH	b2	PEQ1 coefficient	See Table 9-7
2DH	a0/4	PEQ2 coefficient	See Table 9-7
2EH	a1/4	PEQ2 coefficient	See Table 9-7
2FH	a2	PEQ2 coefficient	See Table 9-7
30H	b1/4	PEQ2 coefficient	See Table 9-7
31H	b2	PEQ2 coefficient	See Table 9-7
32H	a0/4	PEQ3 coefficient	See Table 9-7
33H	a1/4	PEQ3 coefficient	See Table 9-7
34H	a2	PEQ3 coefficient	See Table 9-7
35H	b1/4	PEQ3 coefficient	See Table 9-7
36H	b2	PEQ3 coefficient	See Table 9-7
38H	HDmp0	Surround hi-dump0 coefficient	See Table 9-6
39H	HDmp1	Surround hi-dump1 coefficient	See Table 9-6
3AH	KLe0	Surround Lch E/R tap0 volume	See Tables 7-3-5 (1) and (2)
3BH	KLe1	Surround Lch E/R tap1 volume	See Tables 7-3-5 (1) and (2)

Table 7-3-2 (2). Coefficient RAM Setting Data (2/4)

Note) See "8. DSP Signal Flow" regarding the symbols.

Address	Symbol	Function	Setting value
3CH	KRe0	Surround Rch E/R tap0 volume	See Tables 7-3-5 (1) and (2)
3DH	KRe1	Surround Rch E/R tap1 volume	See Tables 7-3-5 (1) and (2)
3EH	Kfb	Surround reverberation sound mix	See Tables 7-3-5 (1) and (2)
3FH	KLtp0	Surround Lch S/R tap0 volume	See Tables 7-3-5 (1) and (2)
40H	KLtp1	Surround Lch S/R tap1 volume	See Tables 7-3-5 (1) and (2)
41H	KLtp2	Surround Lch S/R tap2 volume	See Tables 7-3-5 (1) and (2)
42H	KLtp3	Surround Lch S/R tap3 volume	See Tables 7-3-5 (1) and (2)
43H	KLtp4	Surround Lch S/R tap4 volume	See Tables 7-3-5 (1) and (2)
44H	KLtp5	Surround Lch S/R tap5 volume	See Tables 7-3-5 (1) and (2)
45H	KLtp6	Surround Lch S/R tap6 volume	See Tables 7-3-5 (1) and (2)
46H	KLtp7	Surround Lch S/R tap7 volume	See Tables 7-3-5 (1) and (2)
47H	bL0	Surround Lch all pass F. coefficient	See Table 7-3-5 (2)
48H	bL1	Surround Lch all pass F. coefficient	See Table 7-3-5 (2)
49H	KLod	System volume (DAC) Lch	See Table 7-3-5 (1)
4AH	KRod	System volume (DAC) Rch	See Table 7-3-5 (1)
4BH	KRtp0	Surround Rch S/R tap0 volume	See Tables 7-3-5 (1) and (2)
4CH	KRtp1	Surround Rch S/R tap1 volume	See Tables 7-3-5 (1) and (2)
4DH	KRtp2	Surround Rch S/R tap2 volume	See Tables 7-3-5 (1) and (2)
4EH	KRtp3	Surround Rch S/R tap3 volume	See Tables 7-3-5 (1) and (2)
4FH	KRtp4	Surround Rch S/R tap4 volume	See Tables 7-3-5 (1) and (2)
50H	KRtp5	Surround Rch S/R tap5 volume	See Tables 7-3-5 (1) and (2)
51H	KRtp6	Surround Rch S/R tap6 volume	See Tables 7-3-5 (1) and (2)
52H	KRtp7	Surround Rch S/R tap7 volume	See Tables 7-3-5 (1) and (2)
53H	bR0	Surround Rch all pass F. coefficient	See Table 7-3-5 (2)
54H	bR1	Surround Rch all pass F. coefficient	See Table 7-3-5 (2)
56H	LER0	Surround Lch E/R read tap0 address	See Table 7-3-4
57H	LER1	Surround Lch E/R read tap1 address	See Table 7-3-4
58H	RER0	Surround Rch E/R read tap0 address	See Table 7-3-4
59H	RER1	Surround Rch E/R read tap1 address	See Table 7-3-4
5AH	TdoER	Surround E/R delay amount	See Table 7-3-4
5BH	TdiSR	Surround S/R write address	See Table 7-3-4
5CH	Ltp0	Surround Lch S/R read tap0 address	See Table 7-3-4
5DH	Ltp1	Surround Lch S/R read tap1 address	See Table 7-3-4
5EH	Ltp2	Surround Lch S/R read tap2 address	See Table 7-3-4
5FH	Ltp3	Surround Lch S/R read tap3 address	See Table 7-3-4

Table 7-3-2 (3). Coefficient RAM Setting Data (3/4)

Note) See "8. DSP Signal Flow" regarding the symbols.

Address	Symbol	Function	Setting value
60H	Ltp4	Surround Lch S/R read tap4 address	See Table 7-3-4
61H	Ltp5	Surround Lch S/R read tap5 address	See Table 7-3-4
62H	Ltp6	Surround Lch S/R read tap6 address	See Table 7-3-4
63H	Ltp7	Surround Lch S/R read tap7 address	See Table 7-3-4
64H	Lap0i	Surround Lch all pass F.0 write	See Table 7-3-4
65H	Lap0o	Surround Lch all pass F.0 read	See Table 7-3-4
66H	Lap1i	Surround Lch all pass F.1 write	See Table 7-3-4
67H	Lap1o	Surround Lch all pass F.1 read	See Table 7-3-4
68H	Rtp0	Surround Rch S/R read tap0 address	See Table 7-3-4
69H	Rtp1	Surround Rch S/R read tap1 address	See Table 7-3-4
6AH	Rtp2	Surround Rch S/R read tap2 address	See Table 7-3-4
6BH	Rtp3	Surround Rch S/R read tap3 address	See Table 7-3-4
6CH	Rtp4	Surround Rch S/R read tap4 address	See Table 7-3-4
6DH	Rtp5	Surround Rch S/R read tap5 address	See Table 7-3-4
6EH	Rtp6	Surround Rch S/R read tap6 address	See Table 7-3-4
6FH	Rtp7	Surround Rch S/R read tap7 address	See Table 7-3-4
70H	Rap0i	Surround Rch all pass F.0 write	See Table 7-3-4
71H	Rap0o	Surround Rch all pass F.0 read	See Table 7-3-4
72H	Rap1i	Surround Rch all pass F.1 write	See Table 7-3-4
73H	Rap1o	Surround Rch all pass F.1 read	See Table 7-3-4
74H	TdoSR	Surround S/R delay amount	See Table 7-3-4
75H	Kdsh	Tone control input level control	See Table 7-3-5 (1)
76H	bLB	Tone control (bass) Lch coefficient	See Table 9-8
77H	gLB	Tone control (bass) Lch gain	See Table 9-8
78H	bLT	Tone control (treble) Lch coefficient	See Table 9-9
79H	gLT	Tone control (treble) Lch gain	See Table 9-9
7AH	bRB	Tone control (bass) Rch coefficient	See Table 9-8
7BH	gRB	Tone control (bass) Rch gain	See Table 9-8
7CH	bRT	Tone control (treble) Rch coefficient	See Table 9-9
7DH	gRT	Tone control (treble) Rch gain	See Table 9-9
7EH	KLos	System volume (SO) Lch	See Table 7-3-5 (1)
7FH	KRos	System volume (SO) Rch	See Table 7-3-5 (1)

Table 7-3-2 (4). Coefficient RAM Setting Data (4/4)

Note) See "8. DSP Signal Flow" regarding the symbols.

7-3-3. Compressor

[Relevant coefficients] k (address = 17H), Xthp (address = 18H), XthM (address = 19H), Ksd (address = 1AH), Ap (address = 21H), Am (address = 22H), Bp (address = 23H), Bm (address = 24H), Cp (address = 25H), Cm (address = 26H)

The parameter table is shown in Table 7-3-3. The I/O characteristics for the various parameters in the table are as shown in Fig. 7-3-3.

	threshold		gain	coefficient					
	XthM	XthP	k	Ap	Am	Bp	Bm	Cp	Cm
Comp 5	–20 [dB]		6.0 [dB]						
	0 0000	0 0000	2.0 4000	–1.0 E000	1.0 2000	2.0 4000	2.0 4000	0 0000	0 0000
Comp 4	–20 [dB]		5.2 [dB]						
	–1/10 F334	1/10 0CCC	20/11 3A2E	–100/99 DFAE	100/99 2052	200/99 40A5	200/99 40A5	–1/99 FEB6	1/99 014A
Comp 3	–17 [dB]		4.4 [dB]						
	–1/7 EDB7	1/7 1249	5/3 3555	–49/54 E2F7	49/54 1D09	52/27 3DA1	52/27 3DA1	–1/54 FDA2	1/54 025E
Comp 2	–14 [dB]		2.9 [dB]						
	–1/5 E667	1/5 1999	7/5 2CCC	–5/8 EC00	5/8 1400	33/20 34CC	33/20 34CC	–1/40 FCCD	1/40 0333
Comp 1	–9.5 [dB]		1.6 [dB]						
	–1/3 D556	1/3 2AAA	6/5 2666	–9/20 F19A	9/20 0E66	3/2 3000	3/2 3000	–1/20 F99A	1/99 0666

Table 7-3-3. Compressor Parameter Table

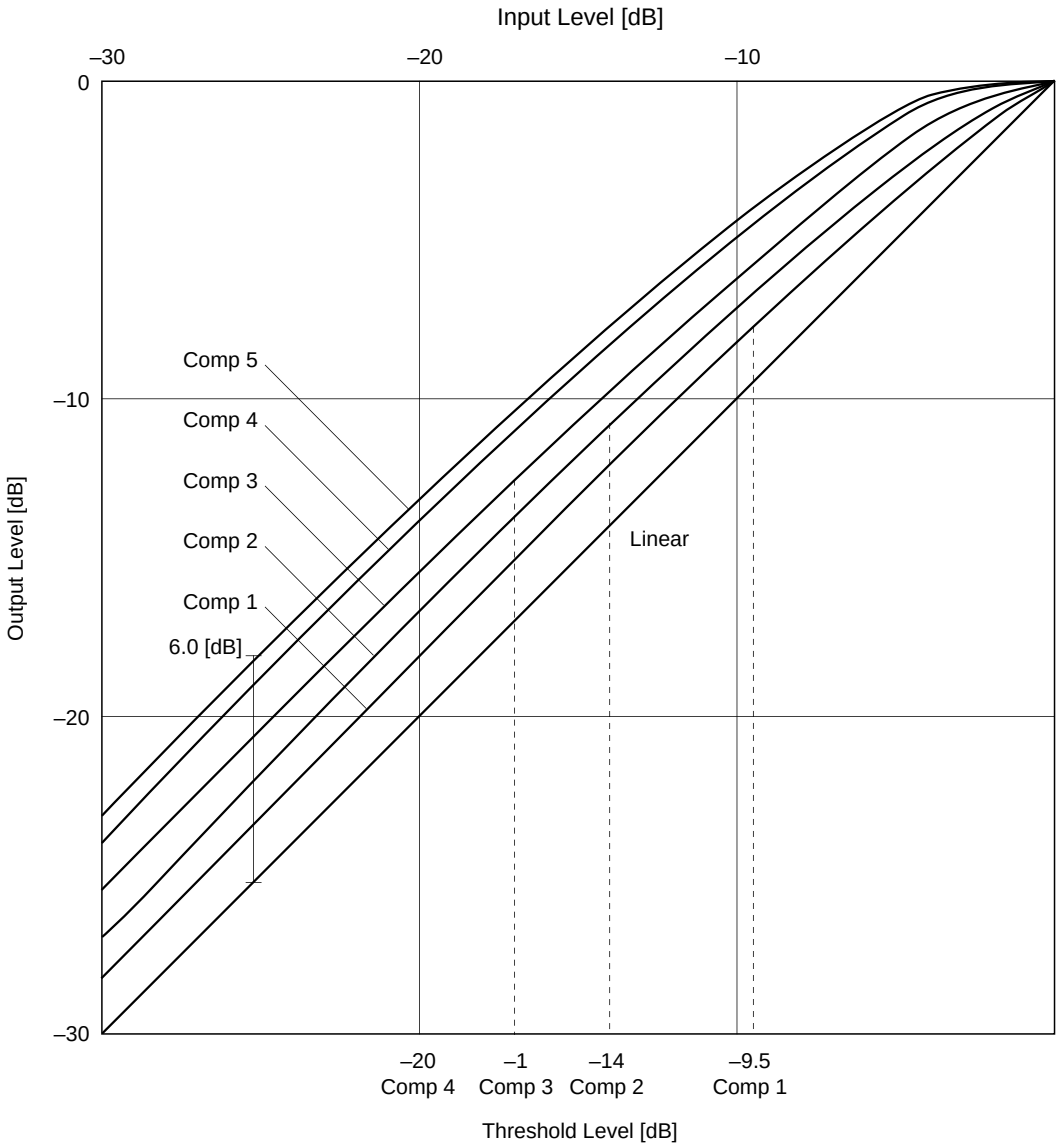


Fig. 7-3-3. Compressor I/O Characteristics

7-3-4. Surround

[Relevant coefficients] kLri (address = 15H), KRri (address = 16H), HDmp0 (address = 38H), HDmp1 (address = 39H), KLe0 (address = 3AH), KLe1 (address = 3BH), KRe0 (address = 3CH), KRe1 (address = 3DH), Kfb (address = 3EH), KLtp0 (address = 3FH), KLtp1 (address = 40H), KLtp2 (address = 41H), KLtp3 (address = 42H), KLtp4 (address = 43H), KLtp5 (address = 44H), KLtp6 (address = 45H), KLtp7 (address = 46H), bL0 (address = 47H), bL1 (address = 48H), KRtp0 (address = 4BH), KRtp1 (address = 4CH), KRtp2 (address = 4DH), KRtp3 (address = 4EH), KRtp4 (address = 4FH), KRtp5 (address = 50H), KRtp6 (address = 51H), KRtp7 (address = 52H), bR0 (address = 53H), bR1 (address = 54H), TdiER (address = 55H), LER0 (address = 56H), LER1 (address = 57H), RER0 (address = 58H), RER1 (address = 59H), TdoES (address = 5AH), TdiSR (address = 5BH), Ltp0 (address = 5CH), Ltp1 (address = 5DH), Ltp2 (address = 5EH), Ltp3 (address = 5FH), Ltp4 (address = 60H), Ltp5 (address = 61H), Ltp6 (address = 62H), Ltp7 (address = 63H), Lap0i (address = 64H), Lap0o (address = 65H), Lap1i (address = 66H), Lap1o (address = 67H), Rtp0 (address = 68H), Rtp1 (address = 69H), Rtp2 (address = 6AH), Rtp3 (address = 6BH), Rtp4 (address = 6CH), Rtp5 (address = 6DH), Rtp6 (address = 6EH), Rtp7 (address = 6FH), Rap0i (address = 70H), Rap0o (address = 71H), Rap1i (address = 72H), Rap1o (address = 73H), TdoSR (address = 74H)

• Delay amount setting

The built-in delay RAM capacity which can be used in music mode is 128K bits (approximately 185ms). The surround block has a number of delay lines for initial reverberation sound and higher-order reverberation sound, and the delay RAM can be assigned freely to these delay lines.
However, the following restrictions apply.

$0000H \leq TdoES \leq FFD0H$ → Determines the initial reverberation sound delay amount
$TdoES \leq TdiSR \leq FFD0H$
$TdiSR + TdoSR \leq FFD0H$ → Determines the higher-order reverberation sound delay amount
$TdiSR + Lap0i \leq FFD8H$ ($Lap0i \geq TdoSR + 0008H$)
$TdiSR + Lap0o \leq FFE0H$ ($Lap0o \geq 0008H$)
$TdiSR + Lap1i \leq FFE0H$ ($Lap1i \geq Lap0o$)
$TdiSR + Lap1o \leq FFE8H$ ($Lap1o \geq 0008H$)
$TdiSR + Rap0i \leq FFE8H$ ($Rap0i \geq Lap1o$)
$TdiSR + Rap0o \leq FFF0H$ ($Rap0o \geq 0008H$)
$TdiSR + Rap1i \leq FFF0H$ ($Rap1i \geq Rap0o$)
$TdiSR + Rap1o \leq FFF8H$ ($Rap1o \geq 0008H$)

(LER0, LER1, RER0, RER1) ≤ TdoER
(Ltp∗, Rtp∗) ≤ TdoSR

As shown above, the delay amount can be set to "0" for all delay lines other than the all-pass filter for through operation.
Fig. 7-3-4 shows the setting example where the delay RAM is used to the fullest extent.
Also, the relationships between the delay amount and coefficients are shown in Table 7-3-4.

Setting values TdoER, TdoSR	Delay (Fs = 44.1kHz)
	1Fs [ms] setting possible
0000H	0.023ms
0008H	0.045ms
0010H	0.068ms
.	.
.	.
.	.
FFF0H	185.71ms
FFF8H	185.73ms

Table 7-3-4. Music Mode Delay Amount Setting

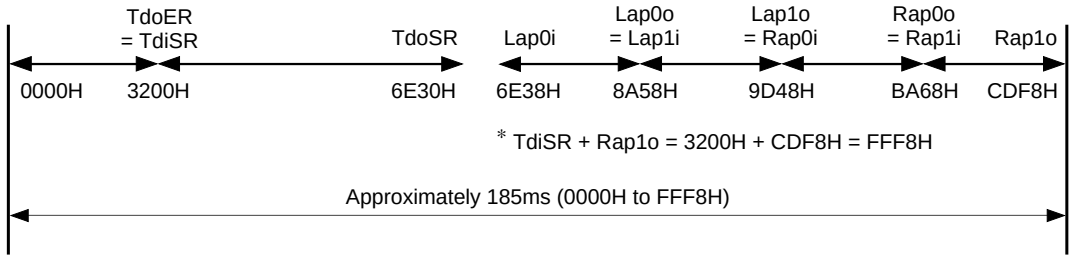


Fig. 7-3-4. Music Mode Delay RAM Setting Example

7-3-5. I/O Level Settings

[Relevant coefficients] (1) Ki (address = 00H), KisLm (address = 08H), KisRc (address = 09H), KiaLm (address = 0AH), KiaRc (address = 0BH), KisRm (address = 0CH), KisLc (address = 0DH), KiaRm (address = 0EH), KiaLc (address = 0FH), KLri (address = 15H), KRri (address = 16H), Kdry (address = 1CH), KLeff (address = 1DH), KReff (address = 1EH), Khr (address = 27H), KLe0 (address = 3AH)*, KLe1 (address = 3BH)*, KRe0 (address = 3CH)*, KRe1 (address = 3DH)*, KLod (address = 49H), KRod (address = 4AH), Kdsh (address = 75H), KLos (address = 7EH), KRos (address = 7FH)

(2) Kfb (address = 3EH)*, KLtp0 (address = 3FH)*, KLtp1 (address = 40H)*, KLtp2 (address = 41H)*, KLtp3 (address = 42H)*, KLtp4 (address = 43H)*, KLtp5 (address = 44H)*, KLtp6 (address = 45H)*, KLtp7 (address = 46H)*, bL0 (address = 47H), bL1 (address = 48H), KRtp0 (address = 4BH)*, KRtp1 (address = 4CH)*, KRtp2 (address = 4DH)*, KRtp3 (address = 4EH)*, KRtp4 (address = 4FH)*, KRtp5 (address = 50H)*, KRtp6 (address = 51H)*, KRtp7 (address = 52H)*, bR0 (address = 53H), bR1 (address = 54H)

The I/O levels and volumes are 2's complement format with the decimal point between D15 and D14, and hexadecimal notation with D15 as MSB and D0 as LSB.

The coefficient and level relationships differ for the relevant coefficients (1) and (2) above, with negative values specified for (1) and positive values for (2). These cases are shown in Tables 7-3-5 (1) and (2), respectively.

Also, phase inverted output is possible for relevant coefficients above which are marked with an asterisk (*) by reversing the positive/negative specification.

D15 to D0	Level
8000H	0dB
↓	↓
FFFFH	–90.31dB
0000H	–∞

Table 7-3-5 (1). I/O Level Settings (negative values)

D15 to D0	Level
7FFFH	Approximately 0dB
↓	↓
0001H	–90.31dB
0000H	–∞

Table 7-3-5 (2). I/O Level Settings (positive values)

The I/O levels for 8000H to FFFFH are determined by the following formulas.

$$\text{(Coefficient value)} = [(-1) \times D15 + \sum_{n=0}^{14} Dn \times 2^{n-15}] \times (-1)$$

I/O level = 20 log [coefficient value] dB

Note) D15 to D0 are negative values, but the calculation is (–1) × (D15 to D0).

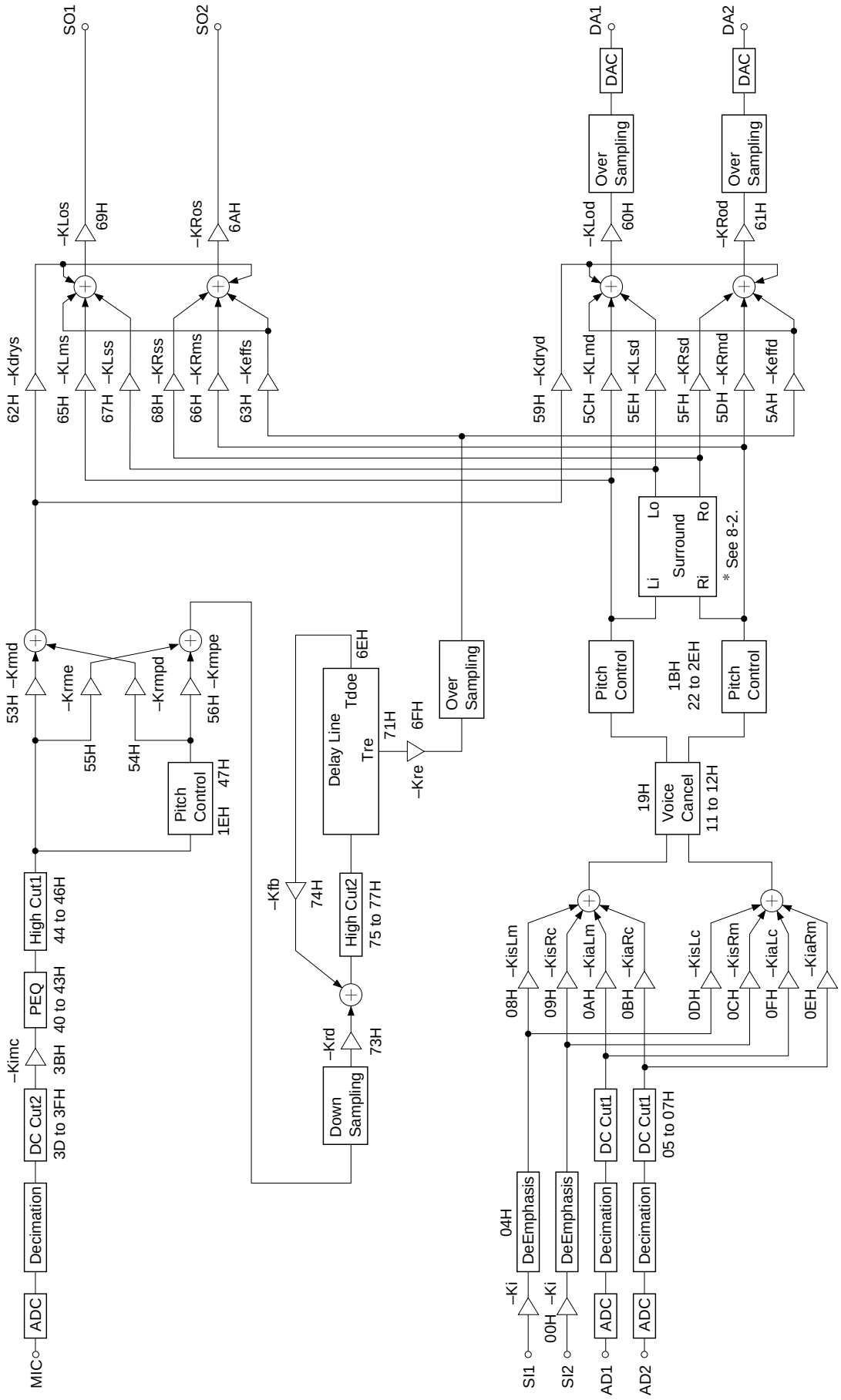
The I/O levels for 7FFFH to 0001H are determined by the following formulas.

$$\text{(Coefficient value)} = [D15 + \sum_{n=0}^{14} Dn \times 2^{n-15}]$$

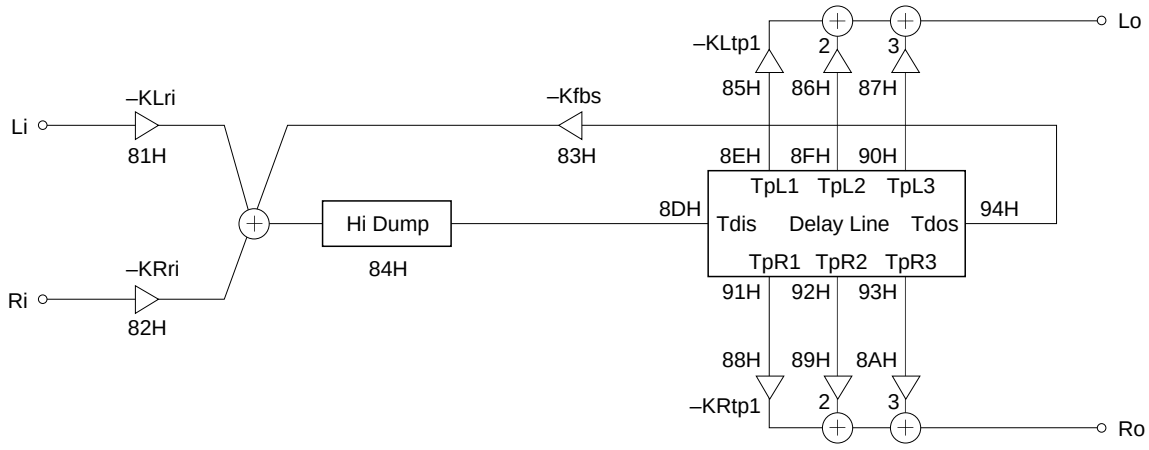
I/O level = 20 log [coefficient value] dB

8. DSP Signal Flow

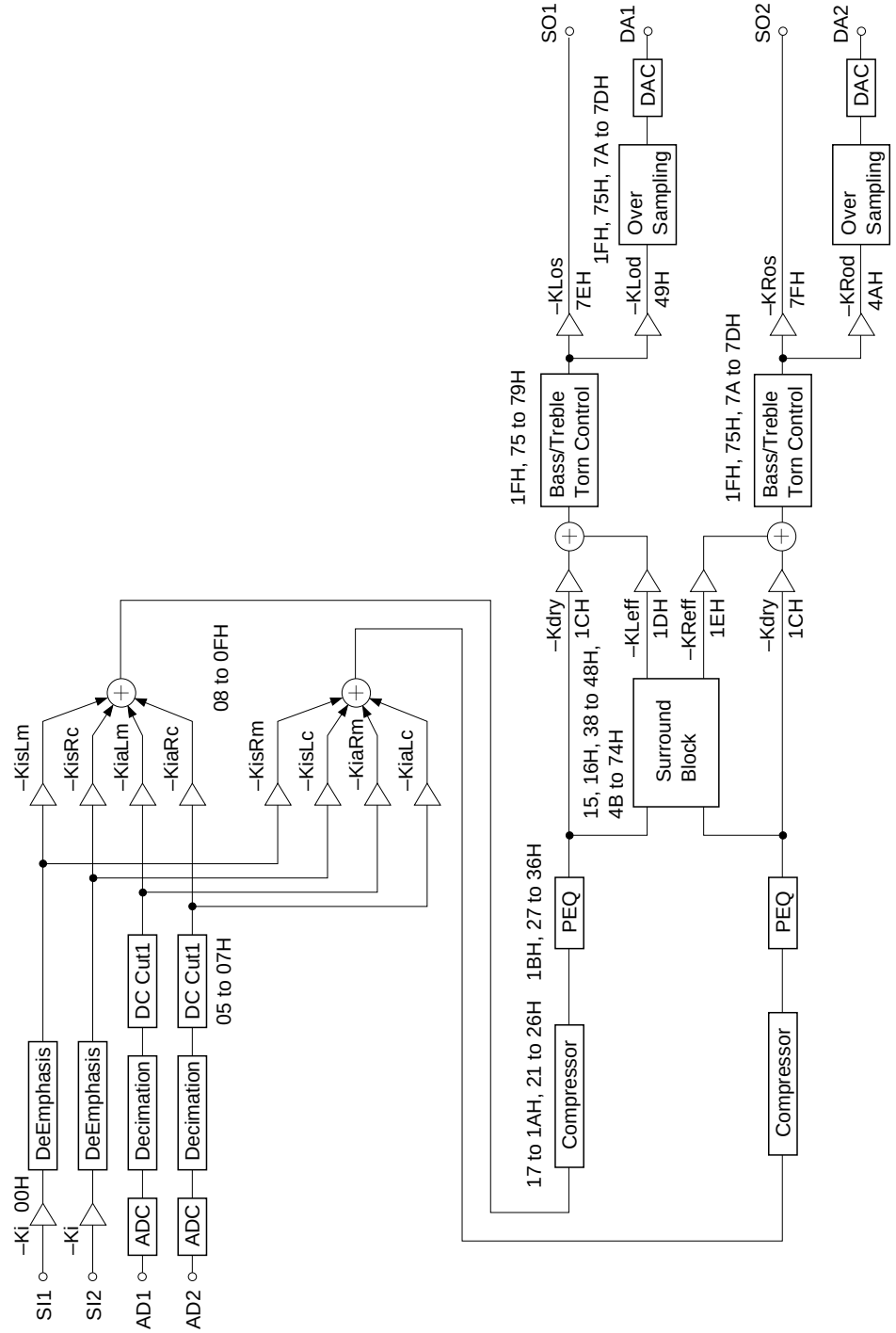
8-1. Karaoke Mode Overall



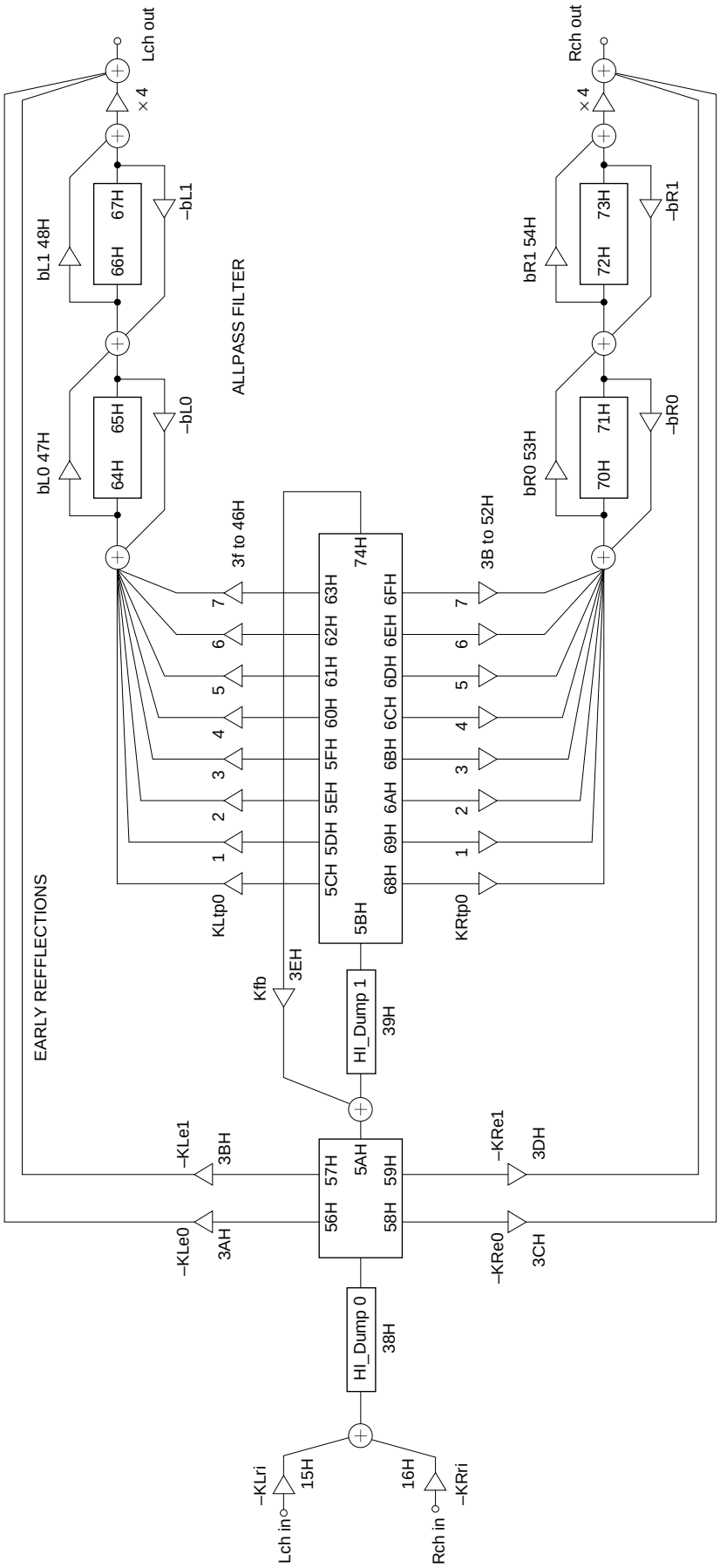
8-2. Karaoke Mode Surround



8-3. Music Mode Overall



8-4. Music Mode Surround



9. Filter Coefficient Tables

The cut-off frequencies and PEQ gain, Q, and center frequency settings for each signal flow filter are shown in Tables 9-1 to 9-9.

Note that if the above setting values are changed during DSP operation, the output level becomes unstable for several 1/fs.

Tables 9-1 to 9-5 and digital de-emphasis are given for fs = 44.1kHz. Consult your Sony representative with regard to use at other than this value.

(1) DC Cut1 for Karaoke Mode or Music Mode Accompaniment/DC Cut2 for Karaoke Mode Voice

[Relevant coefficients] DC1a1 (address = 05H), DC1a0 (address = 06H), DC1b (address = 07H), DC2a1 (address = 3DH), DC2a0 (address = 3EH), DC2b (address = 3FH)

Cut-off frequency [Hz]	DC1a1 DC2a1	DC1a0 DC2a0	DC1b DC2b	Cut-off frequency [Hz]	DC1a1 DC2a1	DC1a0 DC2a0	DC1b DC2b
20	7FD1	802F	7FA2	270	7D95	826B	7B2B
30	7FBA	8046	7F74	280	7D7F	8281	7AFE
40	7FA2	805E	7F45	290	7D68	8298	7AD1
50	7F8B	8075	7F17	300	7D52	82AE	7AA4
60	7F74	808C	7EE9	310	7D3B	82C5	7A77
70	7F5D	80A3	7EBA	320	7D25	82DB	7A4B
80	7F46	80BA	7E8C	330	7D0F	82F1	7A1E
90	7F2F	80D1	7E5E	340	7CF8	8308	79F1
100	7F18	80E8	7E30	350	7CE2	831E	79C5
110	7F01	80FF	7E02	360	7CCC	8334	7998
120	7EEA	8116	7DD4	370	7CB6	834A	796C
130	7ED3	812D	7DA6	380	7CA0	8360	7940
140	7EBC	8144	7D78	390	7C8A	8376	7914
150	7EA5	815B	7D4B	400	7C73	838D	78E7
160	7E8E	8172	7D1D	410	7C5D	83A3	78BB
170	7E77	8189	7CEF	420	7C47	83B9	788F
180	7E61	819F	7CC2	430	7C31	83CF	7863
190	7E4A	81B6	7C94	440	7C1B	83E5	7837
200	7E33	81CD	7C67	450	7C05	83FB	780B
210	7E1C	81E4	7C39	460	7BEF	8411	77DF
220	7E06	81FA	7C0C	470	7BDA	8426	77B4
230	7DEF	8211	7BDF	480	7BC4	843C	7788
240	7DD9	8227	7BB2	490	7BAE	8452	775C
250	7DC2	823E	7B85	500	7B98	8468	7731
260	7DAC	8254	7B58	OFF	0000	8000	0000

Table 9-1.

(2) High Cut1 for Karaoke Mode Voice

[Relevant coefficients] HC1a1 (address = 44H), HC1a0 (address = 45H), HC1b (address = 46H)

Cut-off frequency [Hz]	HC1b	HC1a1	HC1a0	Cut-off frequency [Hz]	HC1b	HC1a1	HC1a0
1000	6EF2	0886	F77A	5600	3416	25F4	DA0C
1100	6D5C	0951	F6AF	5700	3306	267C	D984
1200	6BCB	0A1A	F5E6	5800	31F9	2703	D8FD
1300	6A3E	0AE0	F520	5900	30EC	2789	D877
1400	68B6	0BA4	F45C	6000	2FE2	280E	D7F2
1500	6733	0C66	F39A	6100	2ED8	2893	D76D
1600	65B4	0D25	F2DB	6200	2DD0	2917	D6E9
1700	6439	0DE3	F21D	6300	2CCA	299A	D666
1800	62C3	0E9E	F162	6400	2BC4	2A1D	D5E3
1900	6150	0F57	F0A9	6500	2AC0	2A9F	D561
2000	5FE2	100E	EFF2	6600	29BD	2B21	D4DF
2100	5E77	10C4	EF3C	6700	28BC	2BA1	D45F
2200	5D11	1177	EE89	6800	27BB	2C22	D3DE
2300	5BAE	1228	EDD8	6900	26BC	2CA1	D35F
2400	5A4E	12D8	ED28	7000	25BD	2D21	D2DF
2500	58F2	1386	EC7A	7100	24C0	2D9F	D261
2600	579A	1432	EBCE	7200	23C4	2E1D	D1E3
2700	5645	14DD	EB23	7300	22C9	2E9B	D165
2800	54F3	1586	EA7A	7400	21CF	2F18	D0E8
2900	53A4	162D	E9D3	7500	20D5	2F95	D06B
3000	5259	16D3	E92D	7600	1FDD	3011	CFEF
3100	5110	1777	E889	7700	1EE6	308C	CF74
3200	4FCB	181A	E7E6	7800	1DEF	3108	CEF8
3300	4E88	18BB	E745	7900	1CF9	3183	CE7D
3400	4D48	195B	E6A5	8000	1C04	31FD	CE03
3500	4C0B	19FA	E606	8100	1B10	3277	CD89
3600	4AD0	1A97	E569	8200	1A1C	32F1	CD0F
3700	4998	1B33	E4CD	8300	192A	336A	CC96
3800	4863	1BCE	E432	8400	1838	33E3	CC1D
3900	4730	1C67	E399	8500	1746	345C	CBA4
4000	4600	1CFF	E301	8600	1655	34D5	CB2B
4100	44D2	1D96	E26A	8700	1565	354D	CAB3
4200	43A6	1E2C	E1D4	8800	1475	35C5	CA3B
4300	427C	1EC1	E13F	8900	1386	363C	C9C4
4400	4155	1F55	E0AB	9000	1298	36B3	C94D
4500	4030	1FE7	E019	9100	11A9	372B	C8D5
4600	3F0D	2079	DF87	9200	10BC	37A1	C85F
4700	3DEC	2109	DEF7	9300	0FCF	3818	C7E8
4800	3CCD	2199	DE67	9400	0EE2	388E	C772
4900	3BAF	2228	DDD8	9500	0DF5	3905	C6FB
5000	3A94	22B5	DD4B	9600	0D09	397B	C685
5100	397B	2342	DCBE	9700	0C1E	39F0	C610
5200	3863	23CE	DC32	9800	0B32	3A66	C59A
5300	374D	2459	DBA7	9900	0A47	3ADC	C524
5400	3639	24E3	DB1D	10000	095C	3B51	C4AF
5500	3527	256C	DA94	OFF	0000	0000	8000

Table 9-2.

(3) High Cut2 for Microphone Echo

[Relevant coefficients] HC2a1 (address = 75H), HC2a0 (address = 76H), HC2b (address = 77H)

Conditions: Microphone echo decimation ratio 1/2							
Cut-off frequency [Hz]	HC2b	HC2a1	HC2a0	Cut-off frequency [Hz]	HC2b	HC2a1	HC2a0
1000	5FE2	100E	EFF2	5600	FE68	40CC	BF34
1100	5D11	1177	EE89	5700	FC95	41B5	BE4B
1200	5A4E	12D8	ED28	5800	FAC2	429F	BD61
1300	579A	1432	EBCE	5900	F8EE	4389	BC77
1400	54F3	1586	EA7A	6000	F719	4473	BB8D
1500	5259	16D3	E92D	6100	F543	455E	BAA2
1600	4FCB	181A	E7E6	6200	F36C	464A	B9B6
1700	4D48	195B	E6A5	6300	F194	4736	B8CA
1800	4AD0	1A97	E569	6400	EFBB	4822	B7DE
1900	4863	1BCE	E432	6500	EDE0	4910	B6F0
2000	4600	1CFF	E301	6600	EC02	49FF	B601
2100	43A6	1E2C	E1D4	6700	EA23	4AEE	B512
2200	4155	1F55	E0AB	6800	E841	4BDF	B421
2300	3F0D	2079	DF87	6900	E65D	4CD1	B32F
2400	3CCD	2199	DE67	7000	E476	4DC5	B23B
2500	3A94	22B5	DD4B	7100	E28C	4EBA	B146
2600	3863	23CE	DC32	7200	E09F	4FB0	B050
2700	3639	24E3	DB1D	7300	DEAE	50A9	AF57
2800	3416	25F4	DA0C	7400	DCBA	51A3	AE5D
2900	31F9	2703	D8FD	7500	DAC1	529F	AD61
3000	2FE2	280E	D7F2	7600	D8C5	539D	AC63
3100	2DD0	2917	D6E9	7700	D6C4	549E	AB62
3200	2BC4	2A1D	D5E3	7800	D4BE	55A1	AA5F
3300	29BD	2B21	D4DF	7900	D2B3	56A6	A95A
3400	27BB	2C22	D3DE	8000	D0A3	57AE	A852
3500	25BD	2D21	D2DF	8100	CE8E	58B9	A747
3600	23C4	2E1D	D1E3	8200	CC72	59C7	A639
3700	21CF	2F18	D0E8	8300	CA50	5AD8	A528
3800	1FDD	3011	CFEF	8400	C828	5BEC	A414
3900	1DEF	3108	CEF8	8500	C5F9	5D03	A2FD
4000	1C04	31FD	CE03	8600	C3C2	5E1F	A1E1
4100	1A1C	32F1	CD0F	8700	C184	5F3E	A0C2
4200	1838	33E3	CC1D	8800	BF3E	6061	9F9F
4300	1655	34D5	CB2B	8900	BCEF	6188	9E78
4400	1475	35C5	CA3B	9000	BA98	62B4	9D4C
4500	1298	36B3	C94D	9100	B837	63E4	9C1C
4600	10BC	37A1	C85F	9200	B5CC	651A	9AE6
4700	0EE2	388E	C772	9300	B357	6654	99AC
4800	0D09	397B	C685	9400	B0D7	6794	986C
4900	0B32	3A66	C59A	9500	AE4C	68DA	9726
5000	095C	3B51	C4AF	9600	ABB5	6A25	95DB
5100	0788	3C3B	C3C5	9700	A911	6B77	9489
5200	05B3	3D26	C2DA	9800	A660	6CD0	9330
5300	03E0	3E0F	C1F1	9900	A3A1	6E2F	91D1
5400	020D	3EF9	C107	10000	A0D4	6F96	906A
5500	003A	3FE2	C01E	OFF	0000	0000	8000

Table 9-3 (1).

Conditions: Microphone echo decimation ratio 1/3							
Cut-off frequency [Hz]	HC1b	HC1a1	HC1a0	Cut-off frequency [Hz]	HC1b	HC1a1	HC1a0
1000	5259	16D3	E92D	3600	020D	3EF9	C107
1100	4E88	18BB	E745	3700	FF51	4057	BFA9
1200	4AD0	1A97	E569	3800	FC95	41B5	BE4B
1300	4730	1C67	E399	3900	F9D8	4314	BCEC
1400	43A6	1E2C	E1D4	4000	F719	4473	BB8D
1500	4030	1FE7	E019	4100	F458	45D4	BA2C
1600	3CCD	2199	DE67	4200	F194	4736	B8CA
1700	397B	2342	DCBE	4300	EECD	4899	B767
1800	3639	24E3	DB1D	4400	EC02	49FF	B601
1900	3306	267C	D984	4500	E932	4B67	B499
2000	2FE2	280E	D7F2	4600	E65D	4CD1	B32F
2100	2CCA	299A	D666	4700	E381	4E3F	B1C1
2200	29BD	2B21	D4DF	4800	E09F	4FB0	B050
2300	26BC	2CA1	D35F	4900	DDB4	5126	AEDA
2400	23C4	2E1D	D1E3	5000	DAC1	529F	AD61
2500	20D5	2F95	D06B	5100	D7C5	541D	ABE3
2600	1DEF	3108	CEF8	5200	D4BE	55A1	AA5F
2700	1B10	3277	CD89	5300	D1AC	572A	A8D6
2800	1838	33E3	CC1D	5400	CE8E	58B9	A747
2900	1565	354D	CAB3	5500	CB62	5A4F	A5B1
3000	1298	36B3	C94D	5600	C828	5BEC	A414
3100	0FCF	3818	C7E8	5700	C4DE	5D91	A26F
3200	0D09	397B	C685	5800	C184	5F3E	A0C2
3300	0A47	3ADC	C524	5900	BE18	60F4	9F0C
3400	0788	3C3B	C3C5	6000	BA98	62B4	9D4C
3500	04CA	3D9A	C266	OFF	0000	0000	8000

Table 9-3 (2).

(4) PEQ for Voice

[Relevant coefficients] PEQa (address = 40H), PEQb1 (address = 41H), PEQb2 (address = 42H), PEQg (address = 43H)

Center frequency [Hz]	PEQa	PEQb1	PEQb2
250.0	023D	7DAE	847B
280.6	0282	7D64	8505
315.0	02CF	7D10	859F
353.6	0325	7CB2	864B
396.9	0385	7C47	870B
445.4	03F0	7BCF	87E1
500.0	0467	7B48	88CF
561.2	04EC	7AAE	89D9
630.0	0580	7A01	8B01
707.1	0624	793D	8C4A
793.7	06DB	785E	8DB7
890.9	07A6	7762	8F4D
1000.0	0886	7643	910E
1122.5	097E	74FD	92FE
1259.9	0A91	738B	9524
1414.2	0BC0	71E5	9781
1587.4	0D0D	7004	9A1C
1781.8	0E7C	6DE0	9CFA
2000.0	100E	6B6D	A01E
2244.9	11C7	68A1	A38F
2519.8	13A8	656E	A752
2828.4	15B5	61C6	AB6C
3174.8	17F1	5D97	AFE4
3563.6	1A5E	58CF	B4BE
4000.0	1CFF	535A	BA00
4489.8	1FD8	4D24	BFB2
5039.7	22ED	4617	C5DC
5656.9	2642	3E23	CC85
6349.6	29DB	353B	D3B8
7127.2	2DC1	2B5C	DB84
8000.0	31FD	2097	E3FC

Table 9-4.

Gain [dB]	PEQg
0.0	0000
0.5	01E5
1.0	03E7
1.5	0608
2.0	0849
2.5	0AAC
3.0	0D33
3.5	0FE1
4.0	12B7
4.5	15B8
5.0	18E7
5.5	1C46
6.0	1FD9
6.5	23A1
7.0	27A3
7.5	2BE2
8.0	3061
8.5	3524
9.0	3A30
9.5	3F88
10.0	4531
10.5	4B30
11.0	518A
11.5	5844
12.0	5F64

Table 9-5.

(5) Hi-dump F. for Karaoke Mode/Music Mode

[Relevant coefficients] HDmp (address = 84H): Karaoke mode
HDmp0 (address = 38H), HDmp1 (address = 39H): Music mode

* Use 1/1 for music mode.

fc [Hz]	–HDmp			fc [Hz]	–HDmp		
	1/1	1/2	1/3		1/1	1/2	1/3
40	FF46	FE8D	FDD5	1k	EF08	E073	D404
60	FEEA	FDD5	FCC3	2k	E073	C97A	B91E
80	FE8D	FD1E	FBB3	4k	C97A	AD94	9FC6
100	FE31	FC68	FAA6	6k	B91E	9FC6	974D
200	FC68	F8EA	F585	8k	AD94	9912	
400	F8EA	F23A	EBEE	10k	A578		
600	F585	EBEE	E32F	12k	9FC6		
800	F23A	E603	DB3B	14k	9BCC		

Table 9-6.

(6) PEQ for Music Mode

[Relevant coefficients] Kse (address = 1BH), Khr (address = 27H), a0/4 (address = 28H, 2DH, 32H), a1/4 (address = 29H, 2EH, 33H), a2 (address = 2AH, 2FH, 34H), b1/4 (address = 2BH, 30H, 35H), b2 (address = 2CH, 31H, 36H)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	2037	C025	7E92	3FDB	8093
+10	2028	C025	7ECE	3FDB	8093
+8	201C	C025	7EFE	3FDB	8093
+6	2012	C025	7F24	3FDB	8093
+4	200B	C025	7F42	3FDB	8093
+2	2005	C025	7F5A	3FDB	8093
0	2000	C025	7F6D	3FDB	8093
–2	1FFB	C02E	7F5A	3FD2	80B9
–4	1FF5	C03A	7F42	3FC6	80E9
–6	1FEE	C049	7F24	3FB7	8125
–8	1FE4	C05C	7EFF	3FA4	8170
–10	1FD8	C074	7ECF	3F8C	81CF
–12	1FCA	C091	7E94	3F6F	8246

Table 9-7 (1). PEQ Parameter Table (f0 = 22.1 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	204E	C034	7DFA	3FCC	80D0
+10	2038	C034	7E4F	3FCC	80D0
+8	2027	C034	7E93	3FCC	80D0
+6	201A	C034	7EC8	3FCC	80D0
+4	200F	C034	7EF3	3FCC	80D0
+2	2007	C034	7F15	3FCC	80D0
0	2000	C034	7F30	3FCC	80D0
–2	1FF9	C042	7F15	3FBE	8106
–4	1FF1	C052	7EF4	3FAE	8149
–6	1FE6	C068	7EC9	3F98	819E
–8	1FD9	C082	7E94	3F7E	8208
–10	1FC8	C0A4	7E52	3F5C	828E
–12	1FB3	C0CD	7DFF	3F33	8335

Table 9-7 (2). PEQ Parameter Table (f0 = 31.3 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	206D	C04A	7D25	3FB6	8125
+10	204F	C04A	7D9D	3FB6	8125
+8	2037	C04A	7DFD	3FB6	8125
+6	2025	C04A	7E48	3FB6	8125
+4	2015	C04A	7E85	3FB6	8125
+2	2009	C04A	7EB5	3FB6	8125
0	2000	C04A	7EDB	3FB6	8125
–2	1FF7	C05D	7EB5	3FA3	8171
–4	1FEB	C074	7E86	3F8C	81D0
–6	1FDC	C092	7E4A	3F6E	8247
–8	1FC9	C0B7	7E00	3F49	82DC
–10	1FB1	C0E6	7DA3	3F1A	8397
–12	1F94	C121	7D2F	3EDF	8481

Table 9-7 (3). PEQ Parameter Table (f0 = 44.2 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	209A	C068	7BF8	3F98	819E
+10	2070	C068	7CA2	3F98	819E
+8	204E	C068	7D29	3F98	819E
+6	2034	C068	7D94	3F98	819E
+4	201E	C068	7DE9	3F98	819E
+2	200D	C068	7E2C	3F98	819E
0	2000	C068	7E62	3F98	819E
–2	1FF3	C083	7E2D	3F7D	8209
–4	1FE2	C0A4	7DEB	3F5C	828E
–6	1FCD	C0CE	7D98	3F32	8335
–8	1FB2	C102	7D30	3EFE	8407
–10	1F92	C144	7CAE	3EBC	850C
–12	1F69	C195	7C0B	3E6B	8652

Table 9-7 (4). PEQ Parameter Table (f0 = 62.5 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	20DA	C093	7A51	3F6D	8248
+10	209E	C093	7B40	3F6D	8248
+8	206E	C093	7BFE	3F6D	8248
+6	2049	C093	7C95	3F6D	8248
+4	202B	C093	7D0D	3F6D	8248
+2	2013	C093	7D6C	3F6D	8248
0	2000	C093	7DB8	3F6D	8248
–2	1FED	C0B9	7D6E	3F47	82DE
–4	1FD6	C0E8	7D11	3F18	8399
–6	1FB8	C122	7C9D	3EDE	8484
–8	1F93	C16B	7C0C	3E95	85A8
–10	1F65	C1C6	7B57	3E3A	8715
–12	1F2C	C238	7A76	3DC8	88DA

Table 9-7 (5). PEQ Parameter Table (f0 = 88.4 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	2133	C0D0	77FE	3F30	8337
+10	20DE	C0D0	794F	3F30	8337
+8	209C	C0D0	7A5B	3F30	8337
+6	2066	C0D0	7B2F	3F30	8337
+4	203C	C0D0	7BD8	3F30	8337
+2	201B	C0D0	7C5E	3F30	8337
0	2000	C0D0	7CC9	3F30	8337
–2	1FE5	C105	7C61	3EFB	8409
–4	1FC4	C146	7BE0	3EBA	850F
–6	1F9B	C198	7B3E	3E68	8656
–8	1F67	C1FE	7A75	3E02	87ED
–10	1F27	C27C	797C	3D84	89E6
–12	1ED8	C318	7848	3CE8	8C57

Table 9-7 (6). PEQ Parameter Table (f0 = 125.0 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	21B0	C127	74BB	3ED9	8486
+10	2139	C127	7696	3ED9	8486
+8	20DB	C127	780E	3ED9	8486
+6	2090	C127	7939	3ED9	8486
+4	2055	C127	7A27	3ED9	8486
+2	2025	C127	7AE4	3ED9	8486
0	2000	C127	7B7A	3ED9	8486
–2	1FDB	C170	7AEA	3E90	85AB
–4	1FAC	C1CB	7A36	3E35	8719
–6	1F72	C23D	7957	3DC3	88DF
–8	1F2B	C2C9	7843	3D37	8B12
–10	1ED2	C377	76EE	3C89	8DC8
–12	1E66	C44C	754C	3BB4	911C

Table 9-7 (7). PEQ Parameter Table (f0 = 176.8 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	225E	C1A1	702F	3E5F	865A
+10	21B7	C1A1	72C9	3E5F	865A
+8	2133	C1A1	74D9	3E5F	865A
+6	20CA	C1A1	767D	3E5F	865A
+4	2077	C1A1	77CB	3E5F	865A
+2	2035	C1A1	78D4	3E5F	865A
0	2000	C1A1	79A6	3E5F	865A
–2	1FCC	C206	78E0	3DFA	87F2
–4	1F8B	C285	77E9	3D7B	89EC
–6	1F3B	C321	76B8	3CDF	8C5D
–8	1ED8	C3E2	7541	3C1E	8F60
–10	1E5F	C4CD	7375	3B33	930F
–12	1DCC	C5EC	7146	3A14	978A

Table 9-7 (8). PEQ Parameter Table (f0 = 250.0 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	2350	C24D	69DD	3DB3	88E3
+10	2267	C24D	6D80	3DB3	88E3
+8	21AE	C24D	7064	3DB3	88E3
+6	211B	C24D	72B0	3DB3	88E3
+4	20A6	C24D	7483	3DB3	88E3
+2	204A	C24D	75F6	3DB3	88E3
0	2000	C24D	771D	3DB3	88E3
–2	1FB7	C2DA	760D	3D26	8B17
–4	1F5D	C387	74BE	3C79	8DCF
–6	1EEE	C45D	7322	3BA3	9125
–8	1E67	C561	712C	3A9F	9537
–10	1DC4	C69C	6ECB	3964	9A25
–12	1D00	C816	6BF0	37EA	A011

Table 9-7 (9). PEQ Parameter Table (f0 = 353.6 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	249E	C340	6127	3CC0	8C63
+10	2359	C340	6639	3CC0	8C63
+8	2257	C340	6A40	3CC0	8C63
+6	218A	C340	6D73	3CC0	8C63
+4	20E8	C340	6FFE	3CC0	8C63
+2	2067	C340	7203	3CC0	8C63
0	2000	C340	739D	3CC0	8C63
–2	1F9B	C401	722F	3BFF	8F66
–4	1F1F	C4EC	706F	3B14	9317
–6	1E88	C60B	6E4E	39F5	9794
–8	1DD2	C764	6BBC	389C	9CFE
–10	1CF8	C901	68AA	36FF	A375
–12	1BF7	CAE9	650B	3517	AB18

Table 9-7 (10). PEQ Parameter Table (f0 = 500.0 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	2665	C498	5544	3B68	9128
+10	24A3	C498	5C4B	3B68	9128
+8	233E	C498	61DF	3B68	9128
+6	2222	C498	664E	3B68	9128
+4	2141	C498	69D3	3B68	9128
+2	208E	C498	6C9F	3B68	9128
0	2000	C498	6ED8	3B68	9128
–2	1F74	C59B	6CF3	3A65	953B
–4	1ECB	C6D5	6AA9	392B	9A2B
–6	1E00	C84F	67E9	37B1	A018
–8	1D0E	CA0F	64A5	35F1	A722
–10	1BF3	CC1D	60D0	33E3	AF64
–12	1AAC	CE7C	5C62	3184	B8EF

Table 9-7 (11). PEQ Parameter Table (f0 = 707.1 [Hz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	28C9	C67B	454A	3985	9793
+10	265F	C67B	4EF1	3985	9793
+8	2475	C67B	569B	3985	9793
+6	22EF	C67B	5CB2	3985	9793
+4	21B9	C67B	6188	3985	9793
+2	20C3	C67B	6560	3985	9793
0	2000	C67B	686D	3985	9793
–2	1F41	C7D2	65FF	382E	9CFD
–4	1E5D	C96C	6317	3694	A374
–6	1D50	CB50	5FA9	34B0	AB16
–8	1C17	CD83	5BAA	327D	B3FA
–10	1AB0	D008	5716	2FF8	BE2B
–12	191C	D2DF	51EF	2D21	C9A3

Table 9-7 (12). PEQ Parameter Table (f0 = 1.0 [kHz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	2BD4	C90C	30F3	36F4	9FBD
+10	2894	C90C	3DF2	36F4	9FBD
+8	2600	C90C	4844	36F4	9FBD
+6	23F3	C90C	5077	36F4	9FBD
+4	2252	C90C	56FA	36F4	9FBD
+2	2107	C90C	5C27	36F4	9FBD
0	2000	C90C	6043	36F4	9FBD
–2	1F01	CAC2	5D44	353E	A6B7
–4	1DD6	CCC3	59C0	333D	AEE7
–6	1C7C	CF15	55B0	30EB	B860
–8	1AF3	D1B9	5110	2E47	C324
–10	193C	D4AA	4BE9	2B56	CF27
–12	175D	D7E0	4648	2820	DC43

Table 9-7 (13). PEQ Parameter Table (f0 = 1.4 [kHz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	2FF4	CCDA	1563	3326	AACF
+10	2B92	CCDA	26E9	3326	AACF
+8	2817	CCDA	34D5	3326	AACF
+6	2553	CCDA	3FE4	3326	AACF
+4	2321	CCDA	48AC	3326	AACF
+2	2163	CCDA	4FA6	3326	AACF
0	2000	CCDA	5531	3326	AACF
–2	1EAC	CEF9	51A8	3107	B3A8
–4	1D26	D168	4D9A	2E98	BDCD
–6	1B6F	D426	490A	2BDA	C93A
–8	198B	D72C	4400	28D4	D5D4
–10	1781	DA6F	3E92	2591	E36C
–12	155B	DDDE	38DA	2222	F1BA

Table 9-7 (14). PEQ Parameter Table (f0 = 2.0 [kHz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	34B8	D1D6	F586	2E2A	B79A
+10	2F07	D1D6	0C49	2E2A	B70A
+8	2A82	D1D6	1E5E	2E2A	B70A
+6	26EB	D1D6	2CBB	2E2A	B79A
+4	2411	D1D6	3823	2E2A	B79A
+2	21CD	D1D6	4133	2E2A	B79A
0	2000	D1D6	4866	2E2A	B79A
–2	1E4C	D44B	448B	2BB5	C245
–4	1C65	D70A	403D	28F6	CE30
–6	1A50	DA0A	3B88	25F6	DB38
–8	1817	DD3F	3680	22C1	E924
–10	15C6	E096	3143	1F6A	F7A4
–12	136C	E3FA	2BF2	1C06	065C

Table 9-7 (15). PEQ Parameter Table (f0 = 2.8 [kHz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	3A89	D91B	CEA3	26E5	C737
+10	3340	D91B	EBCB	26E5	C737
+8	2D75	D91B	02F3	26E5	C737
+6	28DC	D91B	1559	26E5	C737
+4	2535	D91B	23F5	26E5	C737
+2	224E	D91B	2F91	26E5	C737
0	2000	D91B	38C9	26E5	C737
–2	1DDA	DBB8	34F8	2448	D3A1
–4	1B86	DE8C	30D7	2174	E113
–6	1910	E18A	2C79	1E76	EF48
–8	1687	E49F	27F9	1B61	FDEC
–10	13FB	E7B7	2375	1849	0C9E
–12	117E	EABD	1F0B	1543	1AFC

Table 9-7 (16). PEQ Parameter Table (f0 = 4.0 [kHz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	4091	E301	A654	1CFF	D766
+10	379F	E301	CA1C	1CFF	D766
+8	3084	E301	E688	1CFF	D766
+6	2AE0	E301	FD1B	1CFF	D766
+4	2664	E301	0F0A	1CFF	D766
+2	22D4	E301	1D49	1CFF	D766
0	2000	E301	289A	1CFF	D766
–2	1D67	E55B	254D	1AA5	E518
–4	1AAC	E7D4	21D8	182C	F377
–6	17E2	EA5B	1E4E	15A5	0229
–8	151B	ECE0	1AC7	1320	10CC
–10	1269	EF51	175B	10AF	1F01
–12	0FDC	F1A1	141F	0E5F	2C71

Table 9-7 (17). PEQ Parameter Table (f0 = 5.7 [kHz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	458B	EFC9	8513	1037	E4C0
+10	3B3B	EFC9	AE53	1037	E4C0
+8	330A	EFC9	CF16	1037	E4C0
+6	2C89	EFC9	E91D	1037	E4C0
+4	275E	EFC9	FDC9	1037	E4C0
+2	2343	EFC8	0E35	1037	E4C0
0	2000	EFC9	1B40	1037	E4C0
–2	1D0A	F149	18BB	0EB7	F31C
–4	1A03	F2D2	1626	0D2E	01CD
–6	16FE	F459	1394	0BA7	1072
–8	1410	F5D6	1115	0A2A	1EAB
–10	114A	F73D	0EB9	08C3	2C20
–12	0EBA	F88A	0C8A	0776	3890

Table 9-7 (18). PEQ Parameter Table (f0 = 8.0 [kHz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	47BB	0176	7676	FE8A	EA9E
+10	3CD1	0176	A21C	FE8A	EA9E
+8	3426	0176	C4C9	FE8A	EA9E
+6	2D44	0176	E053	FE8A	EA9E
+4	27CC	0176	F633	FE8A	EA9E
+2	2373	0176	0794	FE8A	EA9E
0	2000	0176	1562	FE8A	EA9E
–2	1CE3	0152	134D	FEAE	F929
–4	19BB	012D	1131	FED3	07E1
–6	169F	0109	0F1E	FEF7	1665
–8	13A3	00E6	0D1F	FF1A	2456
–10	10D6	00C5	0B40	FF3B	3167
–12	0E47	00A7	098A	FF59	3D5C

Table 9-7 (19). PEQ Parameter Table (f0 = 11.3 [kHz], Q = 0.7)

Gain [dB]	a0/4	a1/4	a2	b1/4	b2
+12	418A	1B03	9FD5	E4FD	DA02
+10	3854	1B03	C4AF	E4FD	DA02
+8	3103	1B03	E1F4	E4FD	DA02
+6	2B33	1B03	F934	E4FD	DA02
+4	2695	1B03	0BAC	E4FD	DA02
+2	22EA	1B03	1A57	E4FD	DA02
0	2000	1B03	25FE	E4FD	DA02
–2	1D54	18C2	22D3	E73E	E7DC
–4	1A8B	1668	1F83	E998	F652
–6	17B4	1403	1C25	EBFD	0509
–8	14E5	11A3	18CE	EE5D	139E
–10	122E	0F59	1595	F0A7	21B3
–12	0FA0	0D30	128D	F2D0	2EF4

Table 9-7 (20). PEQ Parameter Table (f0 = 16.0 [kHz], Q = 0.7)

(7) Music Mode Bass Shelving Filter

[Relevant coefficients] bLB (address = 76H), gLB (address = 77H), bRB (address = 7AH), gRB (address = 7BH)

Gain [dB]	gLB/gRB	bLB/bRB	
		fT = 200Hz	fT = 400Hz
+12	5F65	7F18	7E33
+10	4531	7EDD	7DBD
+8	3061	7E92	7D29
+6	1FD9	7E33	7C6F
+4	12B7	7DBD	7B87
+2	0849	7D29	7A65
0	0000	7C6F	78FC
–2	F96B	7C6F	78FC
–4	F431	7C6F	78FC
–6	F00A	7C6F	78FC
–8	ECBD	7C6F	78FC
–10	EA1F	7C6F	78FC
–12	E80A	7C6F	78FC

Table 9-8.

(8) Music Mode Treble Shelving Filter

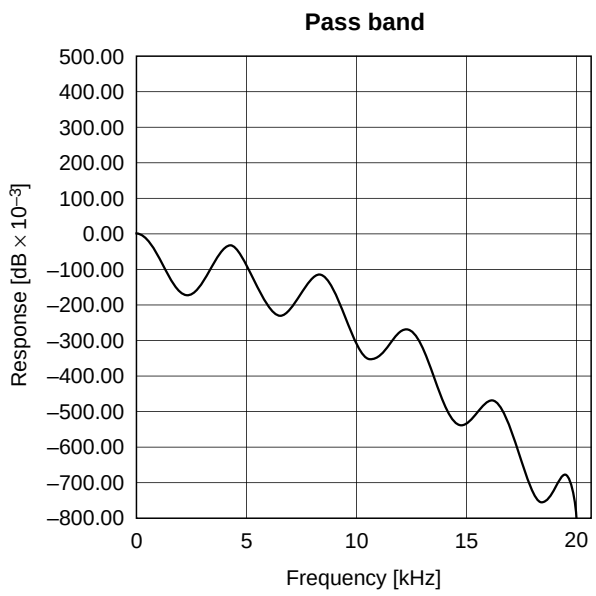
[Relevant coefficients] bLT (address = 78H), gLT (address = 79H), bRT (address = 7CH), gRT (address = 7DH)

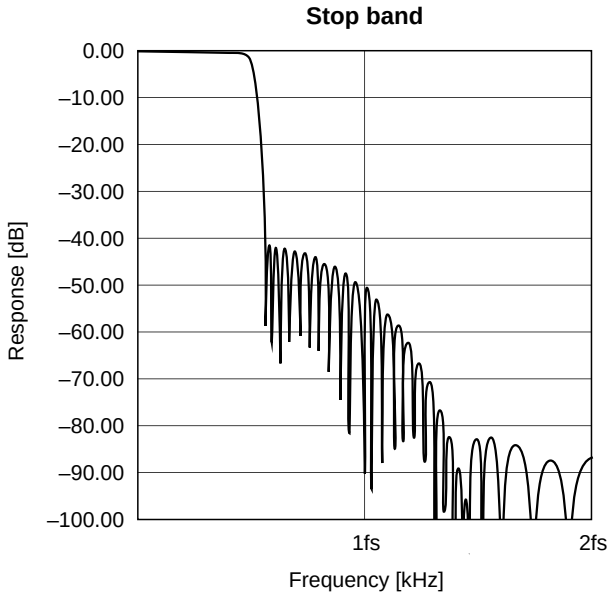
Gain [dB]	gLT/gRT	bLT/bRT	
		fT = 200Hz	fT = 400Hz
+12	5F65	0EAC	DF91
+10	4531	1CF7	EDB5
+8	3061	2A88	FC51
+6	1FD9	371B	0B06
+4	12B7	427F	1972
+2	0849	4C9B	2739
0	0000	556B	3411
–2	F96B	556B	3411
–4	F431	556B	3411
–6	F00A	556B	3411
–8	ECBD	556B	3411
–10	EA1F	556B	3411
–12	E80A	556B	3411

Table 9-9.

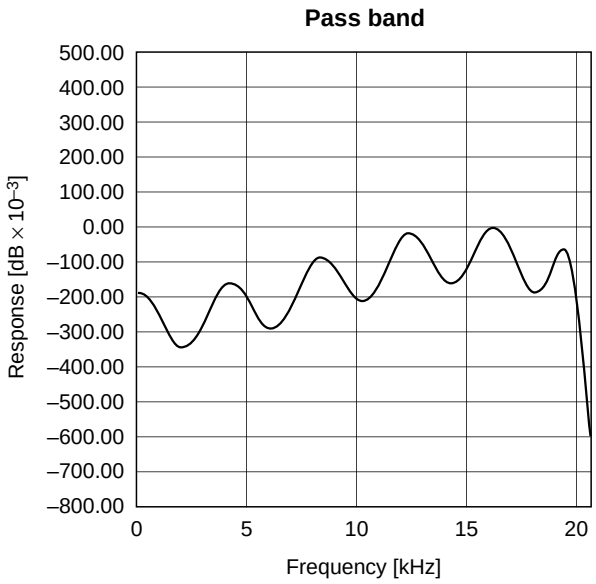
Filter Characteristics

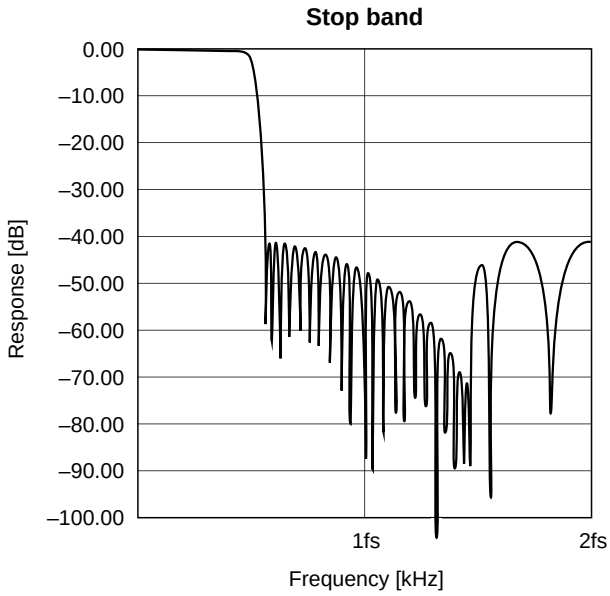
ADC Filter Characteristics (43rd + 15th FIR)



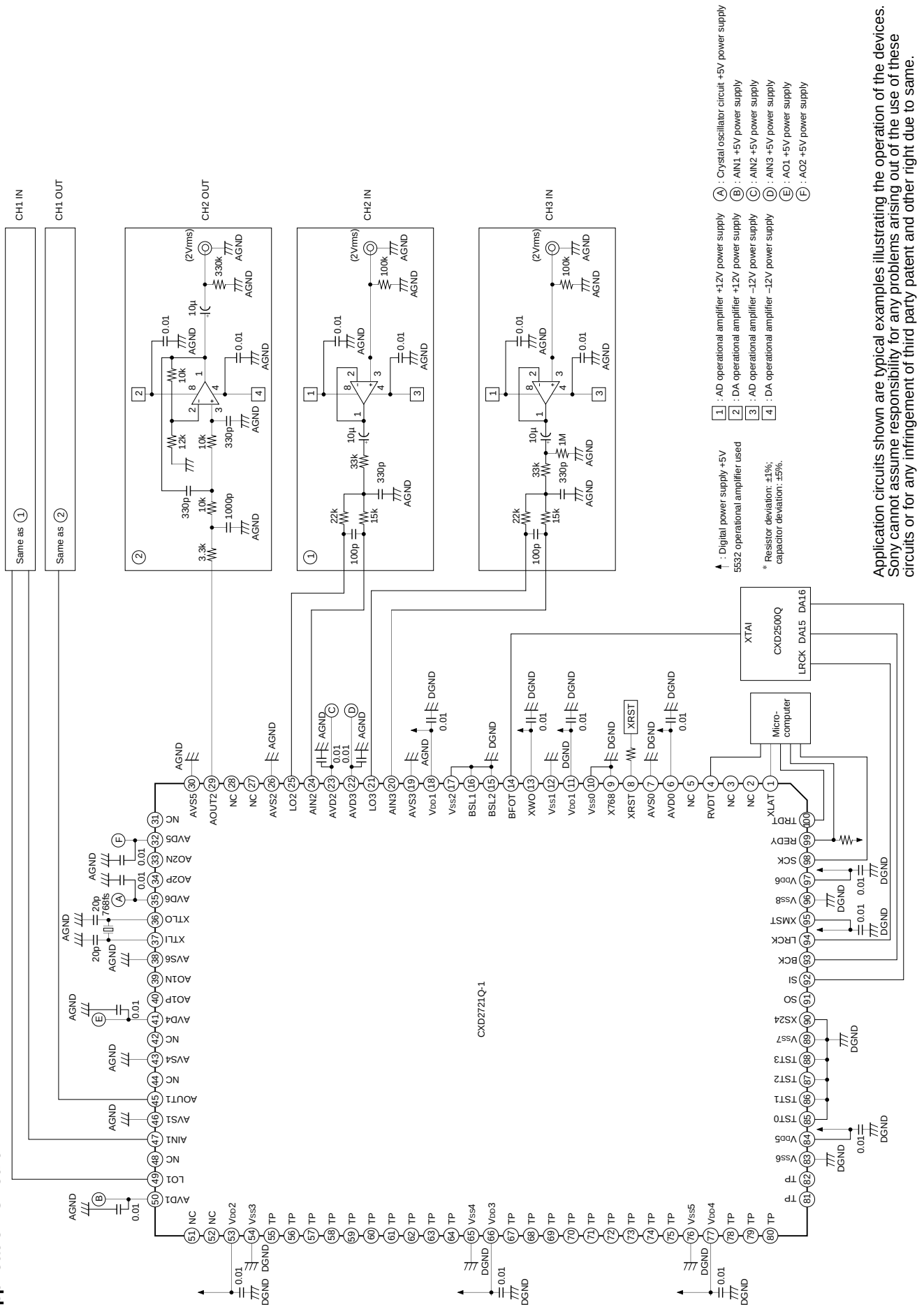


DAC Filter Characteristics (43rd + 7th FIR)





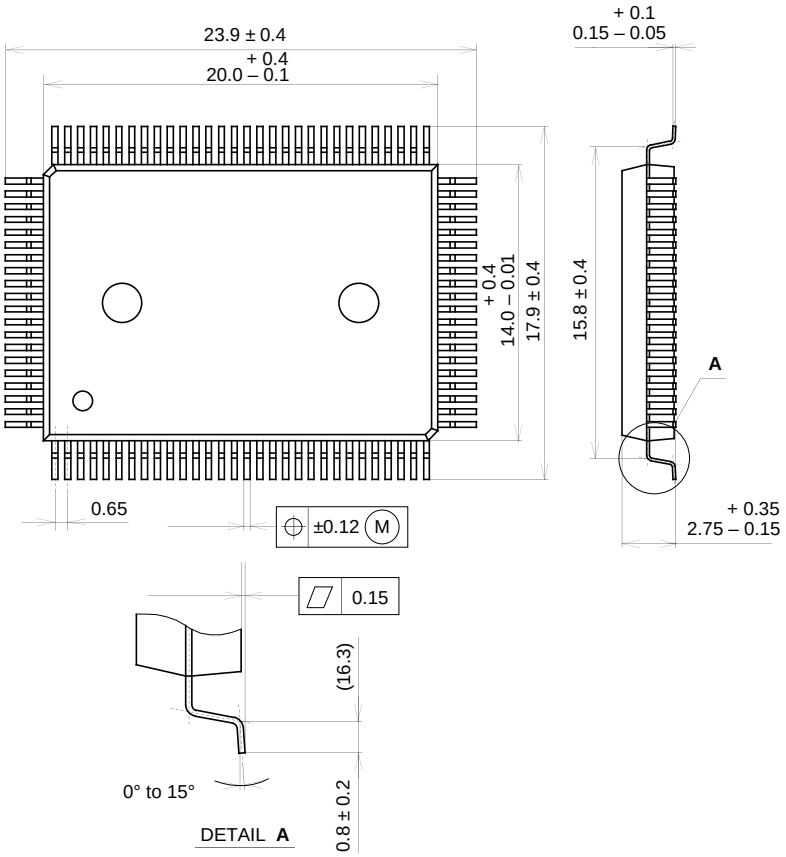
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g