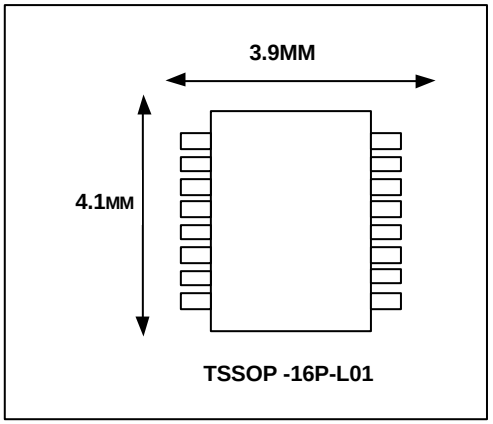
CXG1121TN

DESCRIPTION



The CXG1121TN is one of a range of **low insertion loss**, high power MMIC antenna switches for GSM / GPRS Dualband, Tripleband (CXG1122EN) and Dualmode GSM/UMTS (CXG1114EN) applications. The low insertion loss on transmit means **increased talk time** as the Tx power amplifier can be operated at a lower output level. **On chip logic** reduces component count and **simplifies PCB layout** by allowing direct connection of the switch to digital baseband control lines with **CMOS logic levels**.

This switch is an **SP4T**, one antenna can be routed to either of the 2 Tx or 2 Rx ports. It requires 3 CMOS control lines (Tx/Rx, GSM900/1800 and Standby).

The **Sony GaAs JFET** process is used for low insertion loss.

An evaluation PCB is available.

Features

- Insertion Loss (Tx) 0.5dB typical at 34dBm (GSM 900)
- 3 CMOS compatible Control Lines
- Low second harmonic, -40dBm typical, at 34dBm (GSM 900)
- Small package Size: TSSOP-16 pin (3.9mm x 4.1mm x 1.2mm)

Applications

- Dualband Handsets using combinations of GSM900/GSM1800/GSM1900.
- GPRS Class 12 Handsets

Structure

GaAs J-FET MMIC

GaAs MMIC's are ESD sensitive devices. Special handling precautions are required. The IC will be damaged in the range from 100V to 200V @200pF 0Ω and below 500V @ 100pF 1500Ω The actual ESD test data will be available later.

Truth Table

On Path	Band Select	Tx(H)/Rx(L)	Standby
ANT – Tx1 DCS 1800	H	H	H
ANT – Tx2 GSM 900	L	H	H
ANT – Rx1 GSM 900/DCS1800	L	L	H
ANT – Rx2 GSM 900/DCS1800	H	L	H
OFF	-	-	L

Other frequency assignments upon request. See last page for contact details.

Electrical Characteristics

(T_{amb} = 25°C)

	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	Tx2 - ANT	*1		0·5	0.7	dB
		Tx1 - ANT	*2		0·6	0.8	dB
		ANT – Rx1	*3		0.55	0.75	dB
		ANT – Rx2	*4		0.7	0.9	dB
Isolation	ISO	ANT – Tx1	*3		20		dB
		ANT – Tx2	*4		17		dB
		Tx2 – Rx1,Rx2	*1		20		dB
		Tx1 – Rx1,Rx2	*2		20		dB
VSWR	VSWR				1.2		
Harmonics +	2fo	GSM Tx – ANT	*1		-40	-36	dBm
	3fo		*1		-34	-30	dBm
	2fo	DCS TX – ANT	*2		-40	-36	dBm
	3fo		*2		-34	-30	
P_{1dB} Compression Input Power	P_{1dB}	GSM Tx – ANT	*1		36		dBm
		DCS TX – ANT	*2		36		dBm
Control Current	I_{ctl}		Vdd =3V		80	120	µ A
Supply Current	I_{DD}		STBY=H		0.5	1.0	mA
Leakage Current	I_{lk}		STBY=L		90		µ A

Electrical characteristics are measured with all RF ports terminated in 50 Ohms.

+ Harmonics measured with Tx inputs harmonically matched. We recommend the use of harmonic matching to ensure optimum performance.

* 1 Power incident on GSM Tx, Pin =34dBm, 880 to 915 MHz,Vdd=5.0V, GSM Tx enabled

* 2 Power incident on DCS Tx, Pin =32dBm, 1710 to 1785 MHz, Vdd=5.0V, DCS Tx enabled

* 3 Power incident on ANT, Pin =10dBm, 925 to 960 MHz, Vdd=5.0V, GSM Rx enabled

* 4 Power incident on ANT, Pin = 10dBm, 1805 to 1880 MHz, Vdd=5.0V, DCS Rx enabled

Supply voltage value (Vdd):

Mode	Minimum	Typical	Maximum
GSM/DCS Tx	4.5V	5V	5.7V
GSM/DCS Rx	2.7V	3V	4V

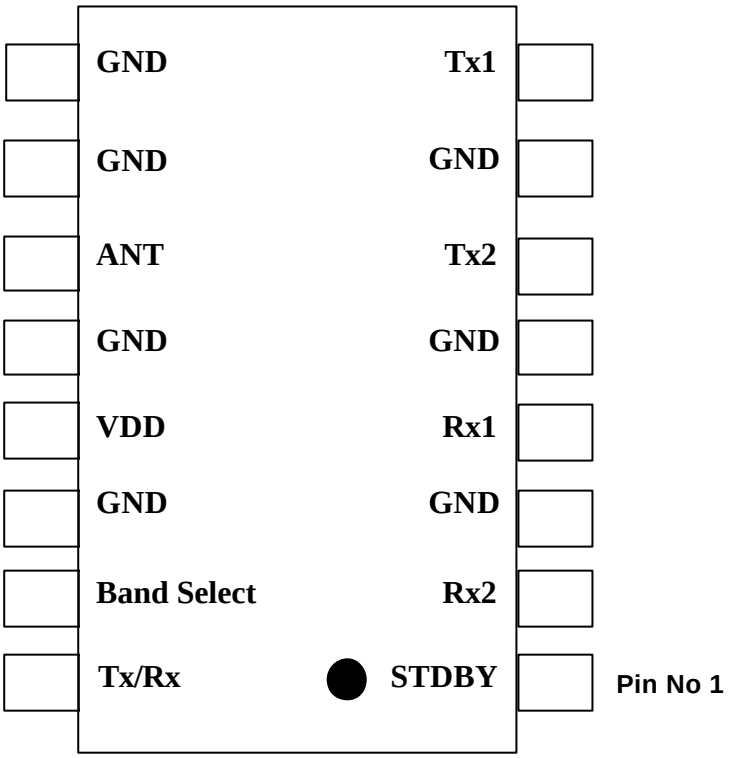
CMOS logic value:

	Minimum	Typical	Maximum
High	2.4V	2.8V	3.2V
Low	0V		0.4V

Absolute Maximum Ratings (Ta = 25°C)

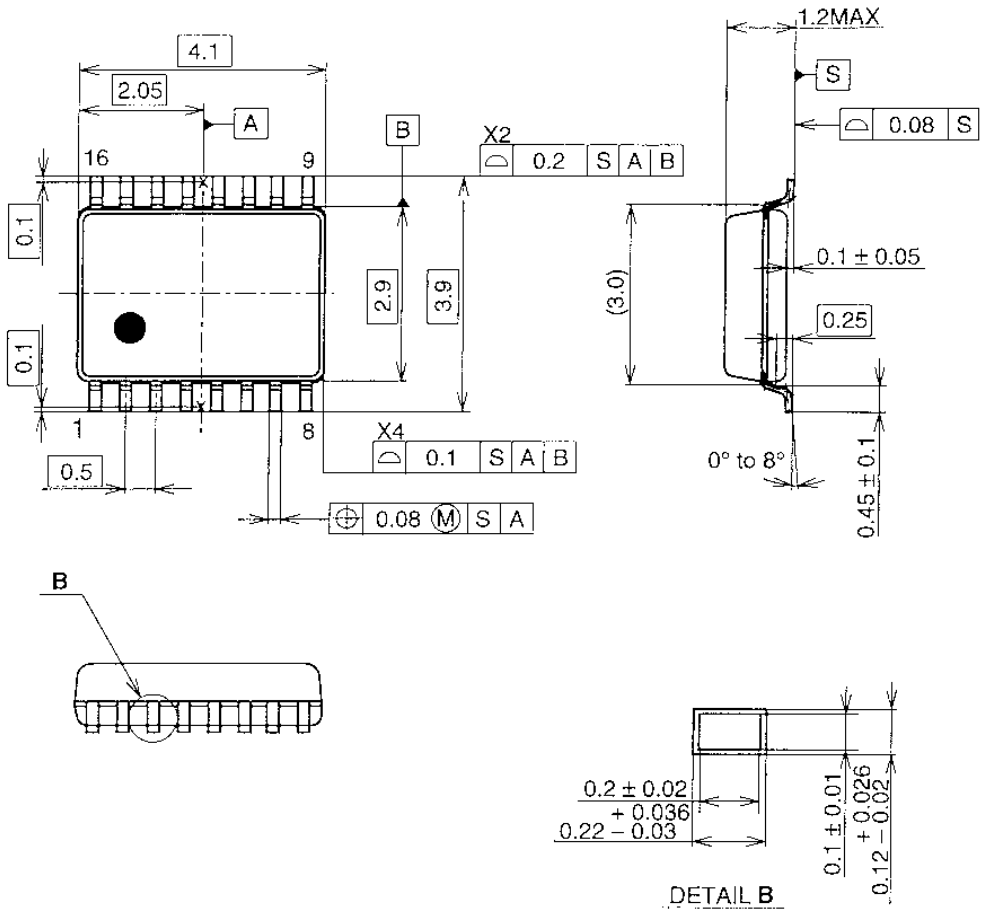
- Bias Voltage Vdd 7V
- Control Voltage Vctl 5V
- Operating Temperature -20°C to +80°C

Pin Out



TSSOP-16P-L01

16PIN TSSOP(PLASTIC)

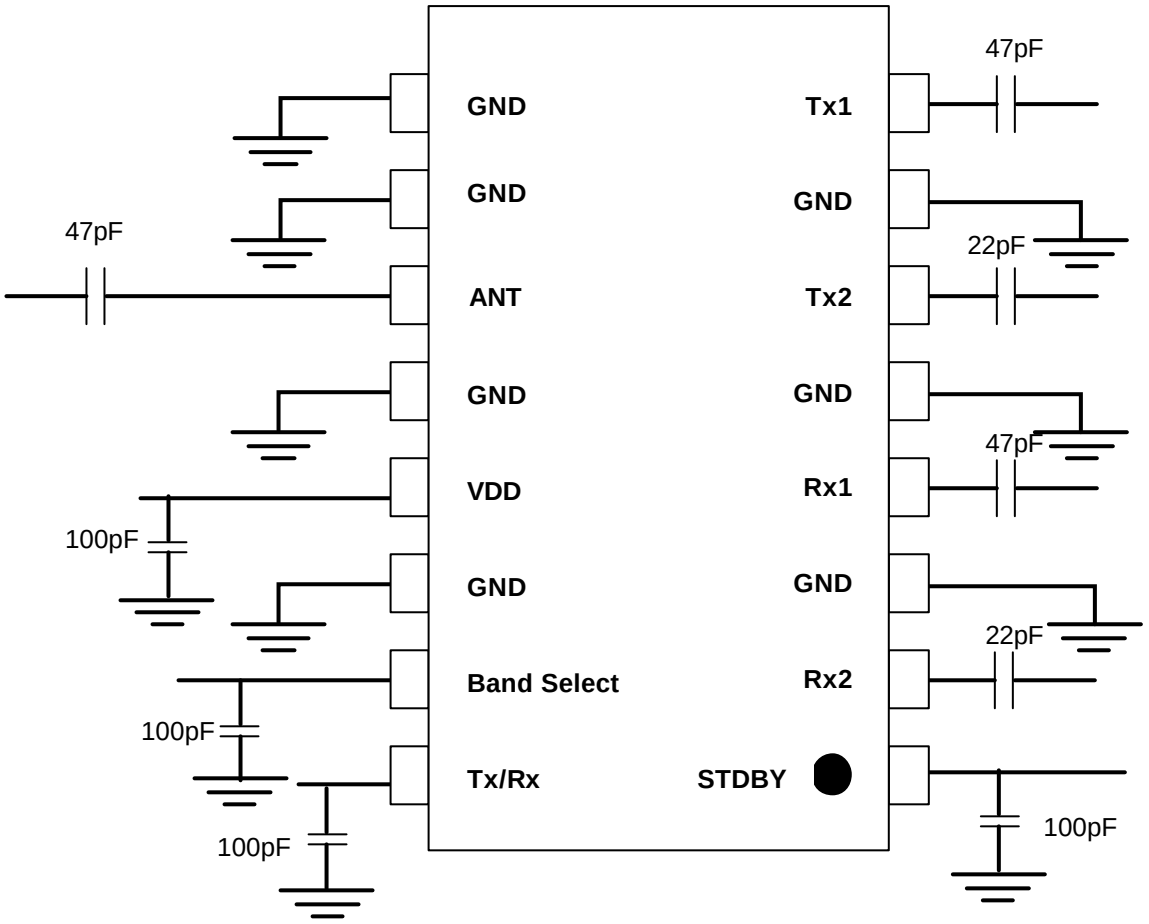


PACKAGE STRUCTURE

SONY CODE	TSSOP-16P-L01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g

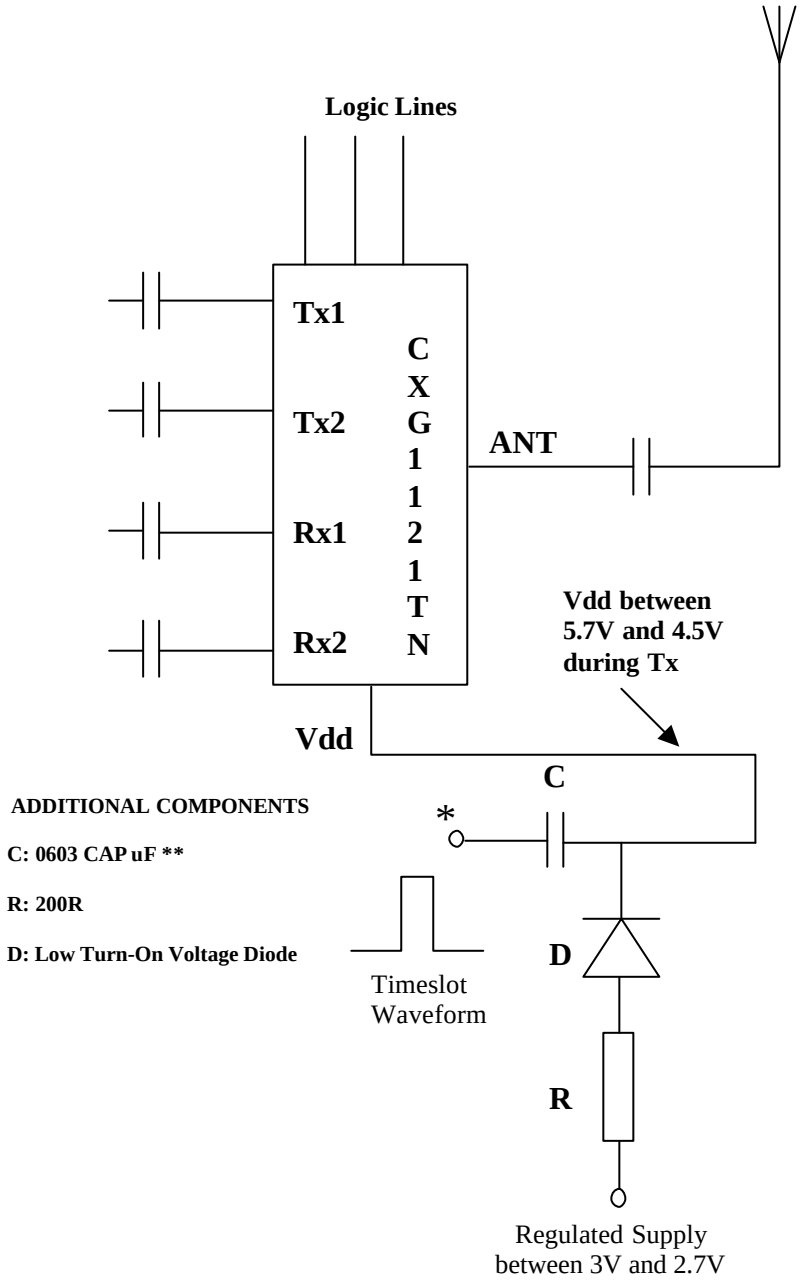
DC Blocking Capacitors and Decoupling Capacitors



Note: Capacitors are required on all RF ports for DC blocking (22pF – 47pF). Decoupling capacitors are required on Vdd and on control lines (100pF).

Application Note 1

Operating the CXG1121TN from Regulated Supplies between 3V and 2.7V



Technique

Allows use of CXG1121TN SP4T in handsets with regulated supplies between 3V and 2.7V.

The CXG1121TN is for 5V nominal battery voltage but works well down to a Vdd of 4.5V.

This technique is only necessary for Tx modes.

Fundamentally, the time slot waveform is added to the supply voltage to give a Vdd between 5.7V and 4.5V (depending on supply) during Tx modes.

This technique is suitable for up to 4 consecutive Tx timeslots (i.e. GPRS Class 12).

***This waveform may be taken from the PA ramping input (or drain supply in case of drain power control) or via the Tx ON/OFF Logic.**

****Minimum and recommended value of capacitance, C, depends on GPRS class and is given by the following table.**

Number of Consecutive Tx Timeslots	Minimum and Recommended Value of Capacitance, C, (uF)
1	1.0
2	2.0
4	2.0

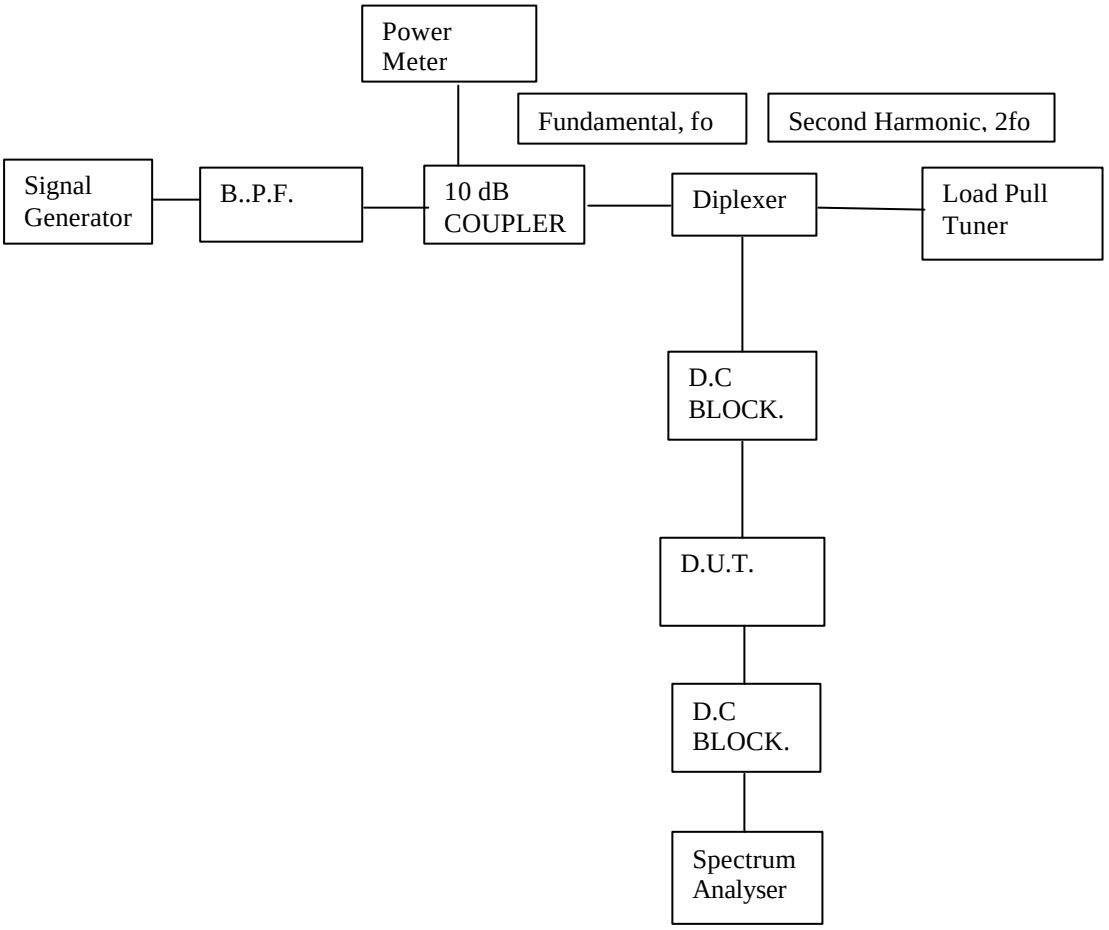
Application Note 2

Impedance Matching for Harmonic Minimisation

This note outlines the method used to find the source impedance to present to a transmit port at the second harmonic frequency (2fo) to reduce the second harmonic level at the antenna.

This should be carried out for a set of devices that represent the process variants. This way a compromise can be found that suits all variants.

The necessary equipment is shown immediately below.



The device should be mounted on a PCB with 50Ω tracks running from all RF pins to SMA connectors on the PCB edge (DUT). All ports should be externally DC blocked and unused ports should be terminated in 50Ω. All measurements should be performed at the incident powers for which the harmonic levels are specified in this document.

The 2nd Harmonic level at the Antenna Port is measured using the Spectrum Analyser and the Vertical and Horizontal position of the Load Pull Stub adjusted such that this level is minimised.

The device should then be removed from the board and an SMA connector mounted such that the source impedance seen by the transmit port at 2fo can be measured using a VNA.

Measurements should be de-embedded to the end of the SMA centre pin.

A network should then be designed to match the impedance of the low pass filter (LPF), which usually comes in front of the device, to the 2fo source impedance that gives sufficiently reduced 2fo levels for all devices measured.

The network should be designed to maintain a good match and insertion loss at the fundamental frequency.

SONY SEMICONDUCTOR AND DEVICES EUROPE SALES OFFICES

Europe

European Design Center:

The Cresent, Jays Close, Basingstoke,

Hampshire, RG22 4DE, United Kingdom

Tel: +44-1256-388883 Fax: +44-1256-388705

Email : thomas.eichhorst@sde.eu.sony.com

US, Canada

SONY Electronics Inc.

16450 West Bernardo Drive / MZ5100

San Diego, California 92127-1804

Tel: +1-858-942-5193 Fax: +1-858-942-9197

Email : nobuyasu.matsuoka@am.sony.com

Others

Semiconductor & Network Company

Gate City Osaki East Tower Osaki East Tec.

1-11-1 Osaki Shinagawa-ku, Tokyo, 141-0032 Japan

Tel: +81-3-5435-3522 Fax: +81-3-5435-3586

Email: seiji.yagawa@jp.sony.com