SONY

SP5T Antenna Switch

CXG1235XR

Description

The CXG1235XR is an SP5T antenna switch.
On chip logic reduces component count and simplifies PCB layout by allowing direct connection of the switch to digital baseband control lines with the CMOS logic levels. It requires 3 CMOS control lines.
The Sony GaAs JPHEMT MMIC Process is used for low insertion loss.

Features

- Insertion loss: 0.40dB (Typ.) @960MHz
  0.50dB (Typ.) @2170MHz
- Lead-Free and RoHS compliant

Package

Small package size: 16-pin XQFN (2.3mm × 2.3mm × 0.35mm) (Typ.)

Structure

GaAs JPHEMT MMIC

Absolute Maximum Ratings

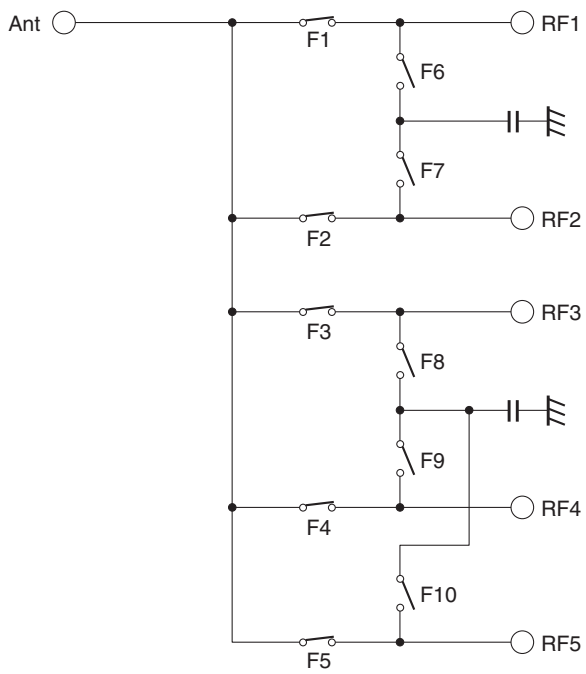
◆ Bias voltage	V_{DD}	7	V	(Ta = 25℃)
◆ Control voltage	Vctl	5	V	(Ta = 25℃)
◆ Input power max.		27	dBm	(824 to 915MHz, Ta = 25℃)
◆ Input power max.		24	dBm	(1710 to 1980MHz, Ta = 25℃)
◆ Operating temperature		–35 to +85	℃	
◆ Storage temperature		–65 to +150	℃	
◆ Allowable power dissipation	P_D	100	mW	*1

*1 25mm × 25mm × t: 0.8mm, Mounted on standard board (FR-4)

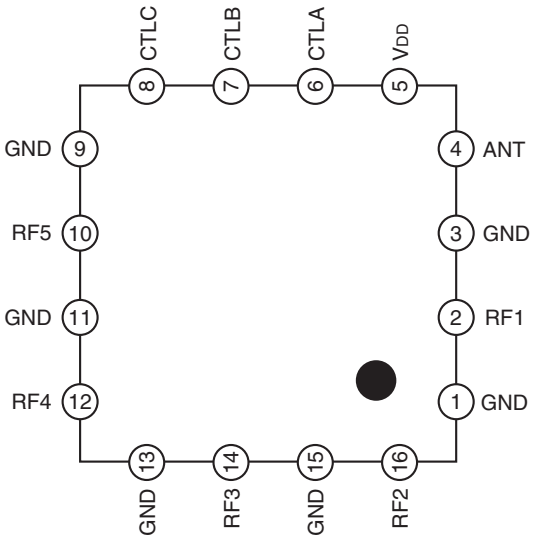
This IC is ESD sensitive device. Special handling precautions are required.

E08227B2Y

Block Diagram



Pin Configuration



16-pin XQFN
2.3mm × 2.3mm × 0.35mm (Typ.)

Truth Table

Port	A	B	C	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
ANT – RF1	H	L	H	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON
ANT – RF2	H	H	L	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON
ANT – RF3	H	L	L	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON
ANT – RF4	L	L/H	L	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON
ANT – RF5	L	L/H	H	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF

DC Bias Condition

(Ta = +25℃)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	1.5	1.8	3.6	V
Vctl (L)	0	—	0.3	
V_{DD}	2.6	2.8	3.6	

Electrical Characteristics

(Ta = +25℃, V_{DD} = 2.8V, Vctl = 0V/1.8V)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Ant – RF1, 2, 3, 4, 5	*1	—	0.40	0.55	dB
			*2	—	0.50	0.65	
VSWR	VSWR		869 to 2170MHz	—	1.2	1.5	—
Harmonics	2fo	Ant – RF1, 2, 3, 4, 5	*3	—	–50	–35	dBm
	3fo			—	–45	–35	
	2fo		*4	—	–50	–35	
	3fo			—	–50	–35	
IMD2	IMD2	Ant – RF1, 2, 3, 4, 5	*5	—	–94	–84	dBm
Input IP2	IIP2			89	99	—	dBm
IMD3	IMD3	Ant – RF1, 2, 3, 4, 5	*6	—	–91	–81	dBm
Input IP3	IIP3			53	58	—	dBm
Control current	Ictl		Vctl = 1.8V	—	10	25	μA
Supply current	Idd		V_{DD} = 2.8V (state: HLH)	—	160	260	μA
Switching speed	Swt		50% Ctl to 90% RF	—	3	6	μs

Electrical characteristics are measured with all RF ports terminated in 50Ω.

*1 Power incident on Ant, Pin = 0dBm, 869 to 960MHz.

*2 Power incident on Ant, Pin = 0dBm, 1805 to 2170MHz.

*3 Power incident on RFx, Pin = 24dBm, 824 to 915MHz.

*4 Power incident on RFx, Pin = 21dBm, 1710 to 1980MHz.

*5 Pin = 20dBm, Ftx = 1950MHz, $P_{Blocker}$ = –15dBm, $F_{Blocker}$ = 190MHz, Fim = 2140MHz, IIP2 = Pin + ($P_{Blocker}$ – IMD2)

*6 Pin = 20dBm, Ftx = 1950MHz, $P_{Blocker}$ = –15dBm, $F_{Blocker}$ = 1760MHz, Fim = 2140MHz, IIP3 = Pin + ($P_{Blocker}$ – IMD3)/2

(Ta = +25°C, V_{DD} = 2.8V, Vctl = 0V/1.8V)

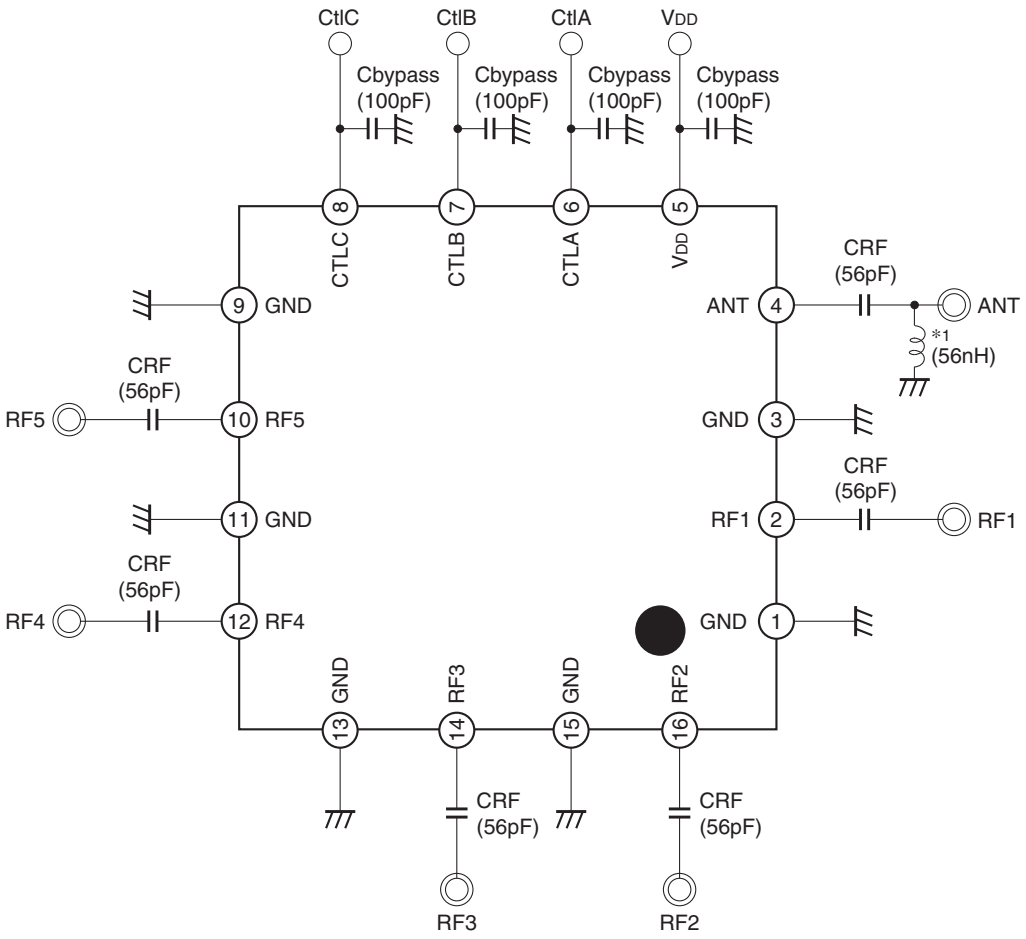
Item	Symbol	Port		Condition	Min.	Typ.	Max.	Unit
		Active	Port					
Isolation	ISO.	RF1	Ant – RF2	*1	20	35	—	dB
			Ant – RF3		20	33	—	
			Ant – RF4		20	33	—	
			Ant – RF5		20	33	—	
			Ant – RF2	*2	20	32	—	
			Ant – RF3		20	38	—	
			Ant – RF4		20	34	—	
			Ant – RF5		20	31	—	
		RF2	Ant – RF1	*1	20	31	—	
			Ant – RF3		20	35	—	
			Ant – RF4		20	32	—	
			Ant – RF5		20	31	—	
			Ant – RF1	*2	20	24	—	
			Ant – RF3		20	40	—	
			Ant – RF4		20	33	—	
			Ant – RF5		20	29	—	
		RF3	Ant – RF1	*1	20	30	—	
			Ant – RF2		20	35	—	
			Ant – RF4		20	34	—	
			Ant – RF5		20	30	—	
			Ant – RF1	*2	20	26	—	
			Ant – RF2		20	36	—	
			Ant – RF4		20	28	—	
			Ant – RF5		20	24	—	
		RF4	Ant – RF1	*1	20	31	—	
			Ant – RF2		20	35	—	
			Ant – RF3		20	32	—	
			Ant – RF5		20	32	—	
			Ant – RF1	*2	20	27	—	
			Ant – RF2		20	42	—	
			Ant – RF3		20	28	—	
			Ant – RF5		20	28	—	
		RF5	Ant – RF1	*1	20	31	—	
			Ant – RF2		20	35	—	
			Ant – RF3		20	31	—	
			Ant – RF4		20	34	—	
			Ant – RF1	*2	20	27	—	
			Ant – RF2		20	40	—	
			Ant – RF3		20	32	—	
			Ant – RF4		20	35	—	

Electrical characteristics are measured with all RF ports terminated in 50Ω.

*1 Power incident on Ant, Pin = 0dBm, 869 to 960MHz.

*2 Power incident on Ant, Pin = 0dBm, 1805 to 2170MHz.

Recommended Circuit



When using this IC, the following external components should be used:

CRF: This capacitor is used for RF decoupling and must be used all applications.
Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

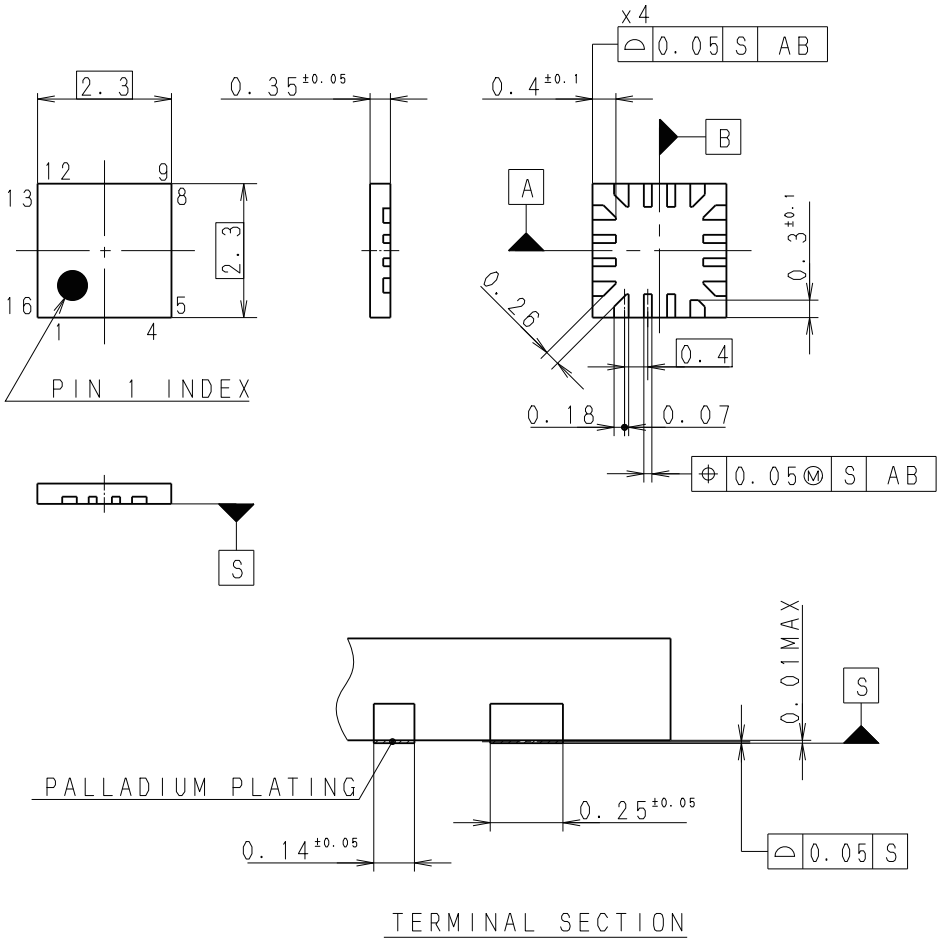
*1 Inductor (56nH) is recommended on Ant port for ESD protection.
Capacitors are required on all RF ports for DC blocking.

Package Outline

(Unit: mm)

Product Code: 75341019 (Renesas)

16PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	XQFN-16P-051
JEITA CODE	————
JEDEC CODE	————

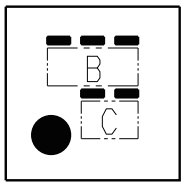
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

PART No. AP-2000-16XND1	Rev. 0
ISSUED 11.12.01	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:XR-16-DD	

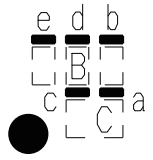
Marking

Product Code: 75341019 (Renesas)



MARKING C: G3

注１）　Ｂ部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
　　（規定文字数未満につき省略は省略規定に従う。
　　製造年は下記２進法ビット方式により表示する。）
　　ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
　　ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
　　ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
　　ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注２）　Ｃ部は製品名（Ｍａｘ２文字）を配置する。
　　（２文字を超える場合は製品名省略標示規定に従う。）
注３）　マーク深さは，Ｍａｘ０．０５ｍｍの事。
注４）　ｅ部は組立場所表記を配置する。



DETAIL B

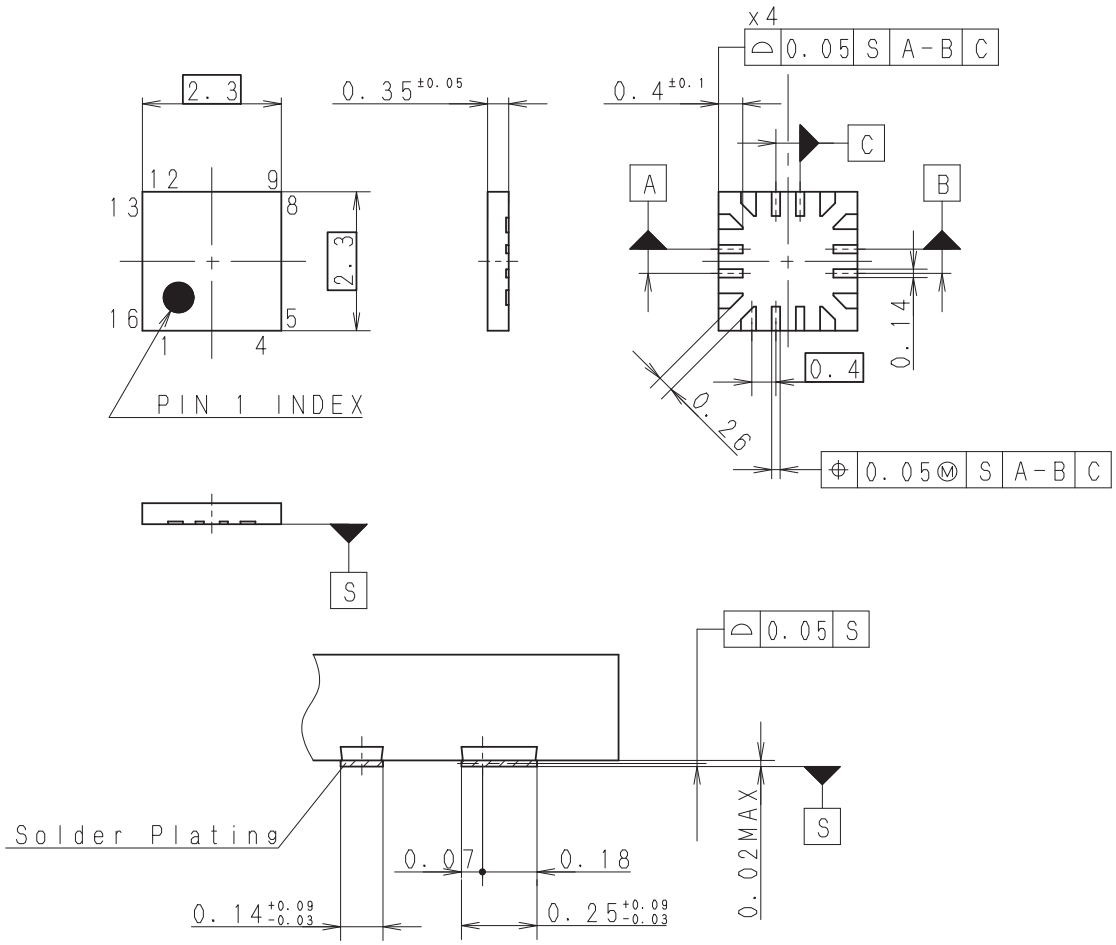
< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION d.
2) TYPE NO.(MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm.
4) ASSEMBLY PLACE IN SECTION e.

Package Outline

(Unit: mm)

Product Code: 75342686 (SDT)/75340779 (Kagoshima)

16PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	XQFN-16P-01
JEITA CODE	————
JEDEC CODE	————

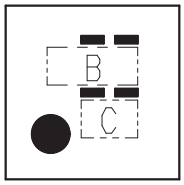
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

AP-4000-16033BS Rev. 0

Marking

Product Code: 75342686(SDT)/75340779 (Kagoshima)



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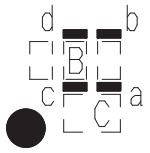
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ２文字）を配置する。
（２文字を超える場合は製品名省略標示規定に従う。）
注3） マーク深さは，ＭａｘＯ．０５ｍｍの事。



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