

**262144-word × 8-bit High Speed CMOS Static RAM Preliminary****Description**

The CXK582000TM/YM/M is a high speed CMOS static RAM organized as 262144-words by 8 bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Special feature are low power consumption and high speed and board package line-up.

The CXK582000TM/YM/M is a suitable RAM for portable equipment with battery back up.

**Features**

- Fast access time                         (Access time)
  - 85LL                                     85ns (Max.)
  - 10LL                                     100ns (Max.)
- Low standby current                     40µA (Max.)
- Low data retention current            24µA (Max.)
- Single +5V supply: 4.5V to 5.5V.
- Low voltage date retention : 2.0V (Min.)
- Broad package line-up

CXK582000TM/YM                         8mm × 20mm 32 pin  
  TSOP Package

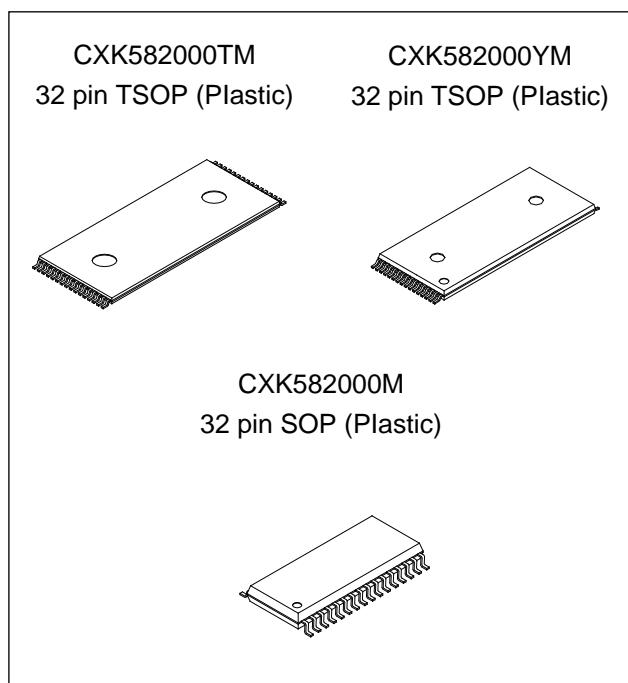
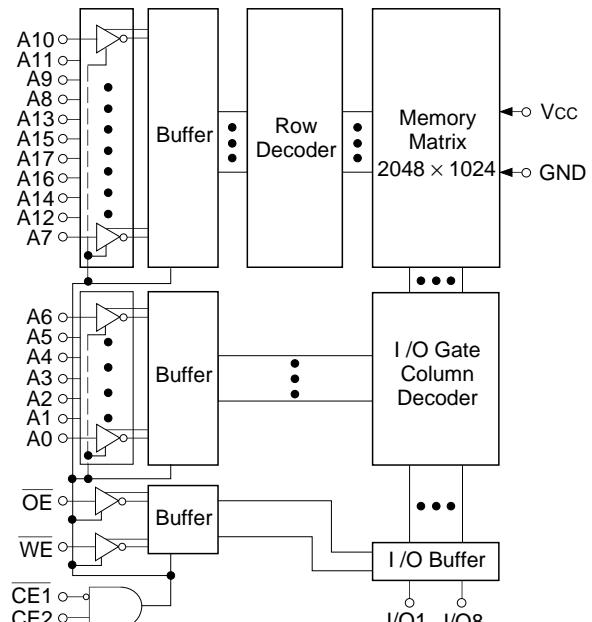
CXK582000M                                525mil 32 pin  
  SOP Package

**Function**

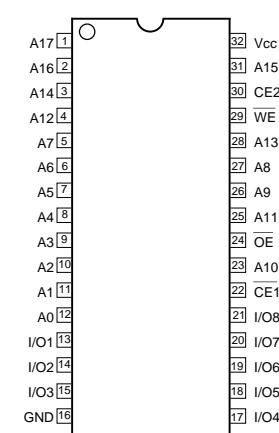
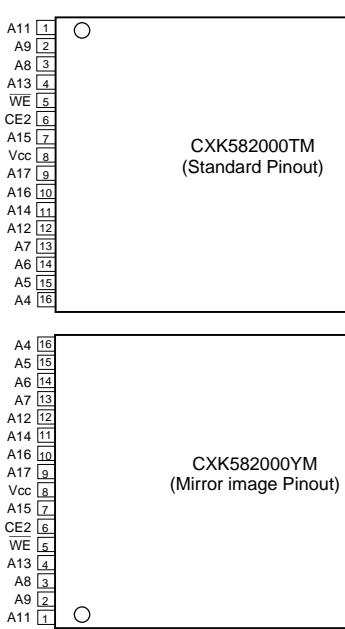
262144 word x 8 bit static RAM

**Structure**

Silicon gate CMOS IC

**Block Diagram**

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**Pin Configuration (Top View)****Pin Description**

Symbol	Description
A0 to A17	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground

**Absolute Maximum Ratings**

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5* to Vcc + 0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P <sub>D</sub>	0.7	W
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature · time	T <sub>solder</sub>	235 · 10	°C · s

\* V<sub>IN</sub>, V<sub>I/O</sub> = -3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O pin	Vcc Current
H	x	x	x	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
x	L	x	x	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	H	Output disable	High Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	L	H	Read	Data out	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	x	L	Write	Data in	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>

x: "H" or "L"

**DC Recommended Operating Conditions** (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	-0.3*	—	0.8	V

\* V<sub>IL</sub> = -3.0V Min. for pulse width less than 50ns.

**Electrical Characteristics**
**• DC Characteristics**
(V<sub>CC</sub> = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		Min.	Typ.*	Max.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>		-1	—	+1	µA
Output leakage current	I <sub>LO</sub>	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or OE = V <sub>IH</sub> or WE = V <sub>IL</sub> V <sub>I/O</sub> = GND to V <sub>CC</sub>		-1	—	+1	µA
Operating power supply current	I <sub>CC1</sub>	CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OUT</sub> = 0mA		—	7	15	mA
Average operating current	I <sub>CC2</sub>	Min. cycle duty = 100% I <sub>OUT</sub> = 0mA	-85LLX	—	45	80	mA
			-10LLX	—	40	70	
	I <sub>CC3</sub>	Cycle time 1µs duty = 100% I <sub>OUT</sub> = 0mA CE1 ≤ 0.2V CE2 ≥ V <sub>CC</sub> - 0.2V V <sub>IL</sub> ≤ 0.2V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V		—	12	24	mA
Standby current	I <sub>SB1</sub>	CE2 ≤ 0.2V or { CE1 ≥ V <sub>CC</sub> - 0.2V CE2 ≥ V <sub>CC</sub> - 0.2V	0 to +70°C	—	—	40	µA
			0 to +40°C	—	—	8	
	I <sub>SB2</sub>	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>		+25°C	—	1.4	4
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA		2.4	—	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.0mA		—	—	0.4	V

\* V<sub>CC</sub> = 5V, Ta = 25°C

**I/O capacitance**

(Ta = 25°C, f = 1MHz)

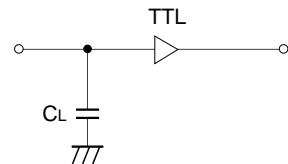
Item	Symbol	Test conditons	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	7	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	8	pF

**Note)** This parameter is sampled and is not 100% tested.**AC Characteristics**

- **AC test conditions** (V<sub>CC</sub> = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V <sub>IH</sub> = 2.2V
Input pulse low level	V <sub>IL</sub> = 0.8V
Input rise time	t <sub>r</sub> = 5ns
Input fall time	t <sub>f</sub> = 5ns
Input and output reference level	1.5V
Output load conditions	C <sub>L*</sub> = 100pF, 1TTL

\* CL includes scope and jig capacitances.



• Read cycle ( $\overline{WE}$  = "H")

(Ta = 0 to +70°C)

Item	Symbol	-85LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	$t_{RC}$	85	—	100	—	ns
Address access time	$t_{AA}$	—	85	—	100	ns
Chip enable access time ( $\overline{CE1}$ )	$t_{CO1}$	—	85	—	100	ns
Chip enable access time ( $CE2$ )	$t_{CO2}$	—	85	—	100	ns
Output enable to output valid	$t_{OE}$	—	45	—	50	ns
Output hold from address change	$t_{OH}$	15	—	15	—	ns
Chip enable to output in low Z ( $\overline{CE1}, CE2$ )	$t_{LZ1}, t_{LZ2}$	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	$t_{OLZ}$	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{CE1}, CE2$ )	$t_{HZ1}, t_{HZ2*}$	—	25	—	35	ns
Output disable to output in high Z ( $\overline{OE}$ )	$t_{OHZ*}$	—	25	—	35	ns

\*  $t_{HZ1}$ ,  $t_{HZ2}$  and  $t_{OHZ}$  are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

## • Write cycle

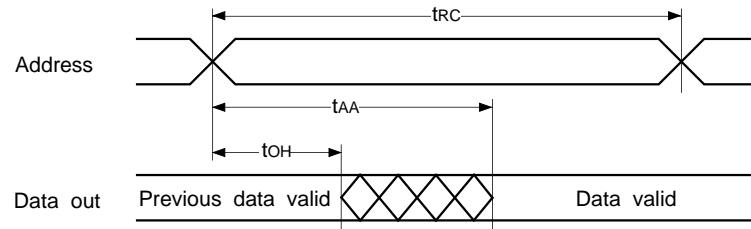
(Ta = 0 to +70°C)

Item	Symbol	-85LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	$t_{WC}$	85	—	100	—	ns
Address valid to end of write	$t_{AW}$	65	—	70	—	ns
Chip enable to end of write	$t_{CW}$	65	—	70	—	ns
Data to write time overlap	$t_{DW}$	35	—	45	—	ns
Data hold from write time	$t_{DH}$	0	—	0	—	ns
Write pulse width	$t_{WP}$	60	—	70	—	ns
Address setup time	$t_{AS}$	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	$t_{WR}$	5	—	5	—	ns
Write recovery time ( $CE1, CE2$ )	$t_{WR1}$	5	—	5	—	ns
Output active from end of write	$t_{OW}$	10	—	10	—	ns
Write to output in high Z	$t_{WHZ*}$	—	25	—	30	ns

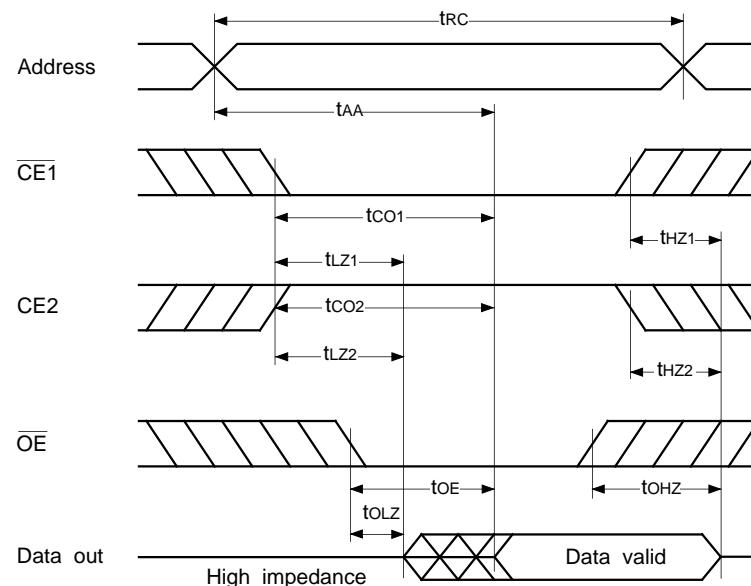
\*  $t_{WHZ}$  is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

**Timing Waveform**

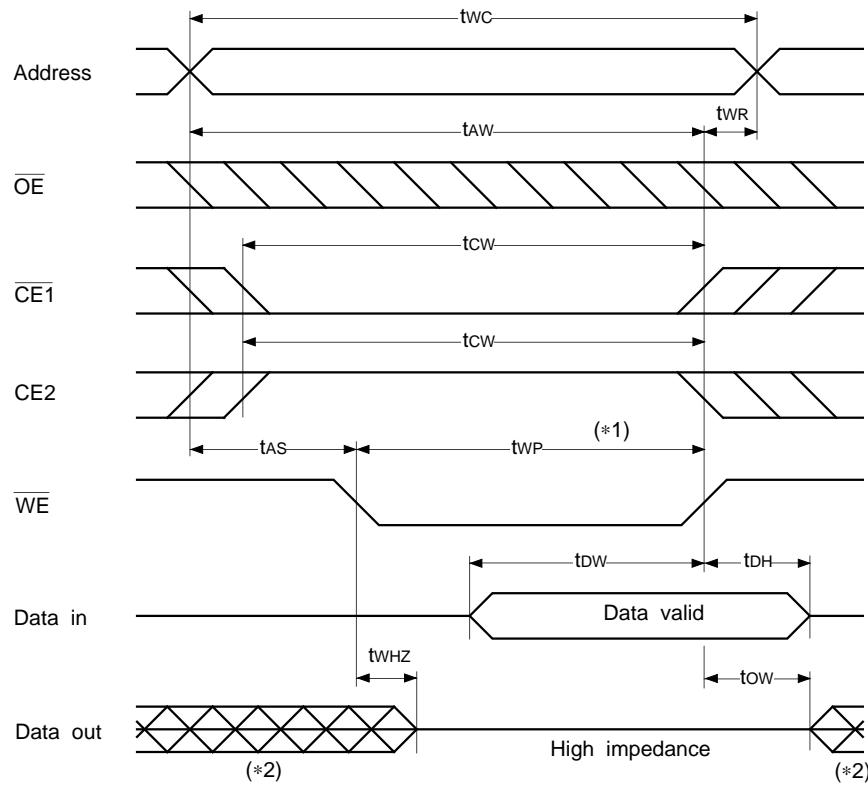
- Read cycle (1) :  $\overline{CE1} = \overline{OE} = V_{IL}$ ,  $CE2 = V_{IH}$ ,  $\overline{WE} = V_{IH}$



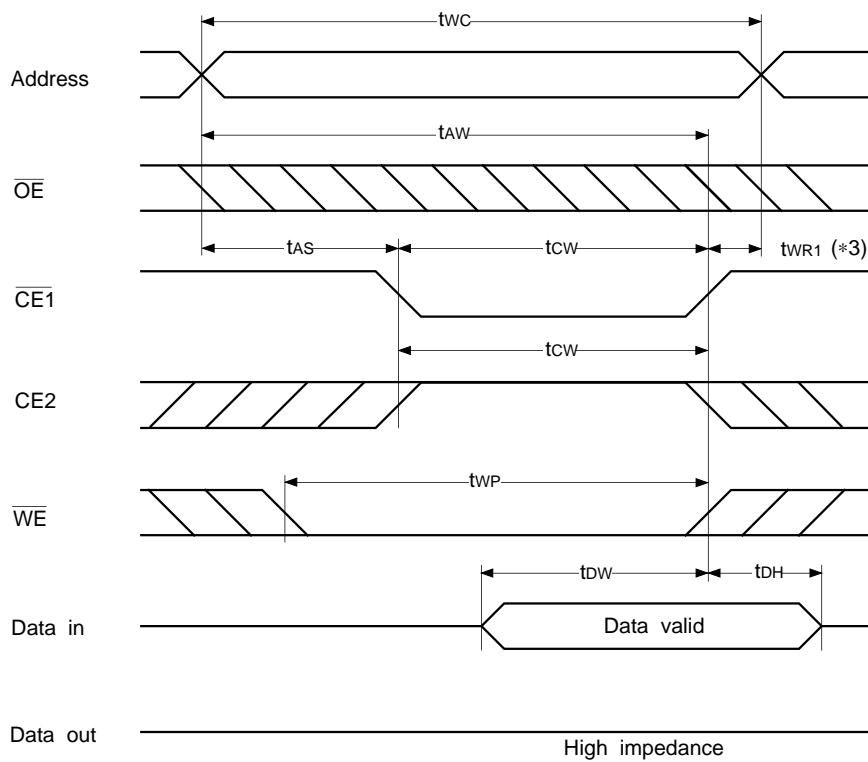
- Read cycle (2) :  $\overline{WE} = V_{IH}$



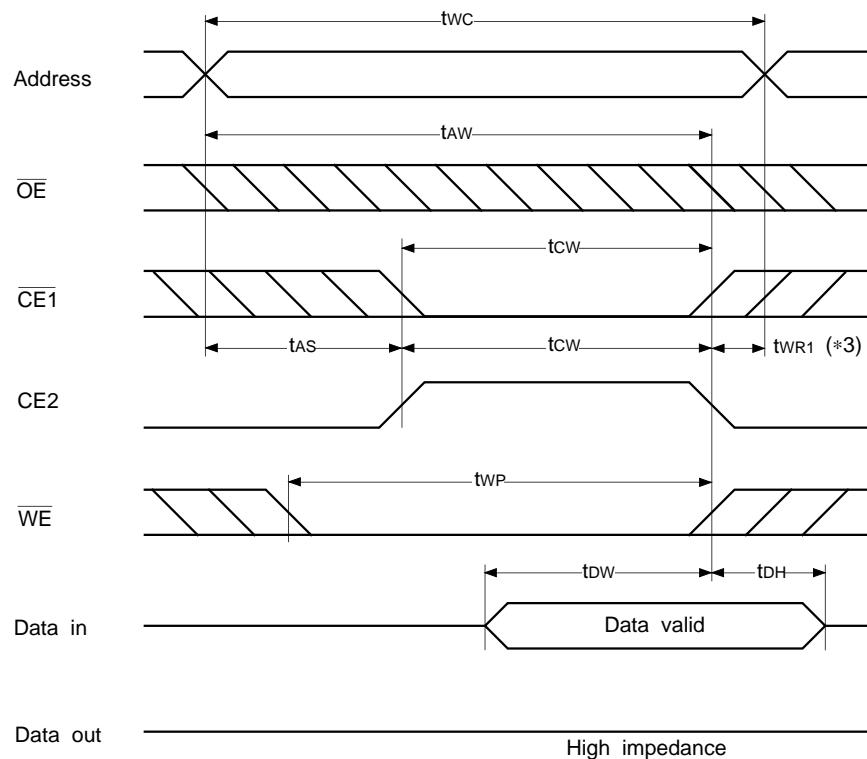
- Write cycle (1) :  $\overline{WE}$  control



- Write cycle (2) :  $\overline{CE1}$  control



- Write cycle (3) : CE2 control



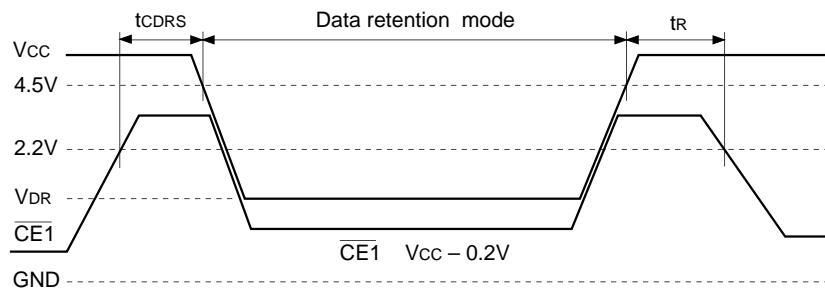
\*1 Write is executed when both  $\overline{CE1}$  and  $\overline{WE}$  are at low and  $CE2$  is at high simultaneously.

\*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

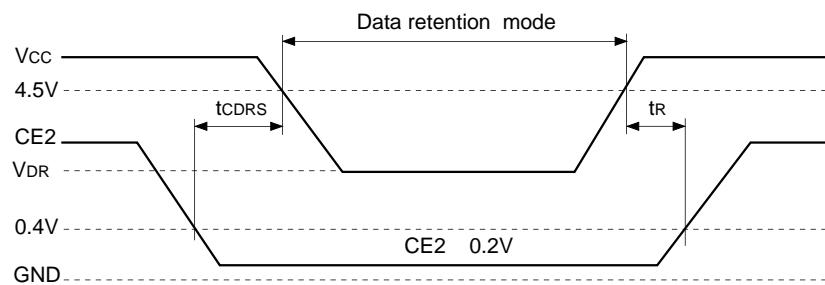
\*3  $t_{WR1}$  is tested from either the rising edge of  $\overline{CE1}$  or the falling edge of  $CE2$ , whichever comes earlier, until the end of the write cycle.

**Data retention waveform**

- Low supply voltage data retention waveform (1) ( $\overline{CE1}$  control)



- Low supply voltage data retention waveform (2) (CE2 control)

**Data Retention Characteristics**

(Ta = 0 to +70°C)

Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V <sub>DR</sub>	*		2.0	—	5.5	V
Data retention current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3.0V* <sup>1</sup>	0 to +70°C	—	—	24	μA
			0 to +40°C	—	—	4.8	
			+25°C	—	0.8	2.4	
	I <sub>CCDR2</sub>	V <sub>CC</sub> = 2.0 to 5.5V*		—	1.4	40	μA
Data retention setup time	t <sub>CDRS</sub>	Chip disable to data retention mode		0	—	—	ns
Recovery time	t <sub>R</sub>			5	—	—	ms

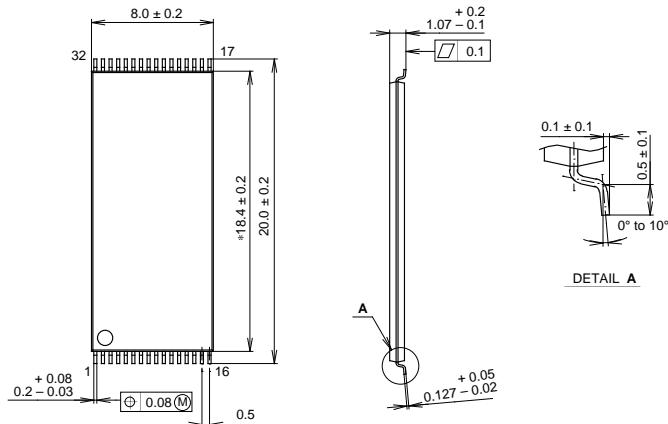
\*  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $CE2 \geq V_{CC} - 0.2V$  ( $\overline{CE1}$  control) or  $CE2 \leq 0.2V$  (CE2 control)

## Package Outline

Unit: mm

## CXK582000TM

32PIN TSOP (I) (PLASTIC)



NOTE : \*NOT INCLUDE MOLD FINS.

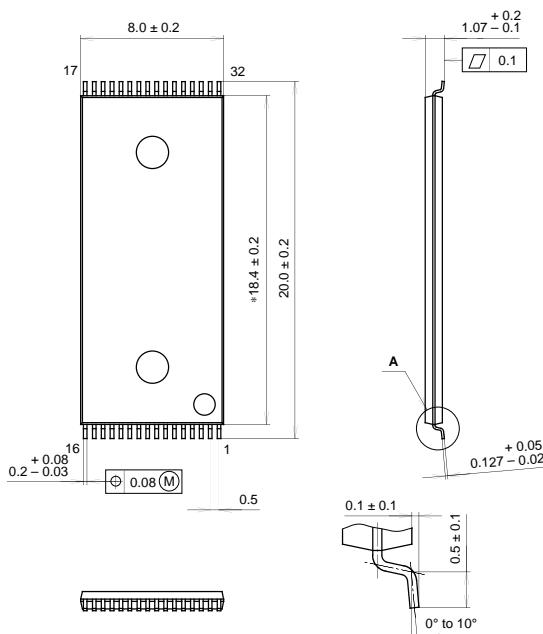
## PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01
EIAJ CODE	TSOP032-P-0820-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	_____

## CXK582000YM

32PIN TSOP (PLASTIC)



NOTE &gt; Dimension "s" does not include mold protrusion.

## DETAIL A

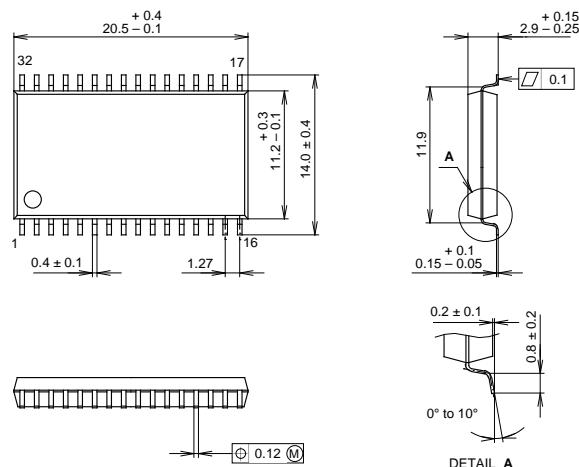
## PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01R
EIAJ CODE	TSOP032-P-0820-B
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

## CXK582000M

32PIN SOP (PLASTIC) 525mil



## PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	*SOP032-P-0525-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	_____