16Mb 1x1Dp HSTL High Speed Synchronous SRAMs (256Kb x 72 or 512Kb x 36 or 1Mb x 18) **Preliminary**

Description

The CXK79M72C164GB (organized as 262,144 words by 72 bits), CXK79M36C164GB (organized as 524,288 words by 36 bits), and the CXK79M18C164GB (organized as 1,048,576 words by 18 bits) are high speed CMOS synchronous static RAMs with common I/O pins. They are manufactured in compliance with the JEDEC-standard 209 pin BGA package pinouts defined for SigmaRAMs. They integrate input registers, high speed RAM, output registers, and a two-deep write buffer onto a single monolithic IC. Single Data Rate (SDR) Pipelined (PL) read operations and Double Late Write (DLW) write operations are supported, providing a high-performance user interface. Positive and negative output clocks are provided for applications requiring source-synchronous operation.

All address and control input signals are registered on the rising edge of the CK differential input clock.

During read operations, output data is driven valid once, from the rising edge of CK, one full cycle after the address and control signals are registered.

During write operations, input data is registered once, on the rising edge of CK, two full cycles after the address and control signals are registered.

Output drivers are series-terminated, and output impedance is programmable via the ZQ control pin. When an external resistor RQ is connected between ZQ and V_{SS}, the impedance of the SRAM's output drivers is set to ~RQ/5.

300 MHz operation (300 Mbps) is obtained from a single 1.8V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

Features

- 3 Speed Bins

	Cycle Time / Data Access Time
-33	3.3ns / 1.8ns
-4	4.0ns / 2.1ns
-44	4.4ns / 2.3ns

- Single 1.8V power supply (V_{DD}): 1.7V (min) to 1.95V (max)
- Dedicated output supply voltage (V_{DDQ}): 1.8V or 1.5V typical
- HSTL-compatible I/O interface with dedicated input reference voltage (V_{REF}): $V_{DDQ}/2$ typical
- Common I/O
- Single Data Rate (SDR) data transfers
- Pipelined (PL) read operations
- Double Late Write (DLW) write operations
- Burst capability with internally controlled Linear Burst address sequencing
- Burst length of two, three, or four, with automatic address wrap
- Full read/write data coherency
- Byte write capability
- Slow down mode via dedicated control pin ($\overline{SD}$)
- Two cycle deselect
- Differential input clocks (CK/$\overline{CK}$)
- Data-referenced output clocks (CQ/$\overline{CQ}$)
- Programmable output driver impedance via dedicated control pin (ZQ)
- Depth expansion capability (2 or 4 banks) via programmable chip enables (E2, E3, EP2, EP3)
- JTAG boundary scan (subset of IEEE standard 1149.1)
- 209 pin (11x19), 1mm pitch, 14mm x 22mm Ball Grid Array (BGA) package

256Kb x 72 Pin Assignment (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	E2	A (16M)	ADV	A (8M)	E3	A	DQb	DQb
B	DQg	DQg	$\overline{BW}$c	$\overline{BW}$g	NC	$\overline{W}$	A	$\overline{BW}$b	$\overline{BW}$f	DQb	DQb
C	DQg	DQg	$\overline{BW}$h	$\overline{BW}$d	NC (128M)	$\overline{E1}$	NC	$\overline{BW}$e	$\overline{BW}$a	DQb	DQb
D	DQg	DQg	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	DQb	DQb
E	DQg	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	M4	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	CQ	$\overline{CQ}$	CK	$\overline{CK}$	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ}$	CQ
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	M2	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	M3	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{SD}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQd	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQe
T	DQd	DQd	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	DQe	DQe
U	DQd	DQd	NC	A	NC (64M)	A	NC (32M)	A	NC	DQe	DQe
V	DQd	DQd	A (2M)	A	A	A1	A	A	A (4M)	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

512Kb x 36 Pin Assignment (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	A	E2	A (16M)	ADV	A (8M)	E3	A	DQb	DQb
B	NC	NC	$\overline{BW}$c	NC	A (x36)	$\overline{W}$	A	$\overline{BW}$b	NC	DQb	DQb
C	NC	NC	NC	$\overline{BW}$d	NC (128M)	$\overline{E1}$	NC	NC	$\overline{BW}$a	DQb	DQb
D	NC	NC	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	DQb	DQb
E	NC	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	DQb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	M4	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ	$\overline{CQ}$	CK	$\overline{CK}$	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ}$	CQ
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	M2	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	M3	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{SD}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQd	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	NC
T	DQd	DQd	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	NC	NC
U	DQd	DQd	NC	A	NC (64M)	A	NC (32M)	A	NC	NC	NC
V	DQd	DQd	A (2M)	A	A	A1	A	A	A (4M)	NC	NC
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	NC	NC

1Mb x 18 Pin Assignment (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	A	E2	A (16M)	ADV	A (8M)	E3	A	NC	NC
B	NC	NC	$\overline{BW}$b	NC	A (x36)	$\overline{W}$	A	NC	NC	NC	NC
C	NC	NC	NC	NC	NC (128M)	$\overline{E1}$	A (x18)	NC	$\overline{BW}$a	NC	NC
D	NC	NC	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	NC	NC
E	NC	DQb	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
F	DQb	DQb	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	DQb	DQb	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	DQb	DQb	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	DQb	DQb	V_{DDQ}	V_{DDQ}	V_{DD}	M4	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ	$\overline{CQ}$	CK	$\overline{CK}$	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ}$	CQ
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	M2	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	M3	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{SD}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	NC
T	NC	NC	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	NC	NC
U	NC	NC	NC	A	NC (64M)	A	NC (32M)	A	NC	NC	NC
V	NC	NC	A (2M)	A	A	A1	A	A	A (4M)	NC	NC
W	NC	NC	TMS	TDI	A	A0	A	TDO	TCK	NC	NC

Pin Description

Symbol	Type	Description
A	Input	Address Inputs - Registered on the rising edge of CK.
A1, A0	Input	Address Inputs 1,0 - Registered on the rising edge of CK. Initialize burst counter.
DQa, DQb DQc, DQd DQe, DQf DQg, DQh	I/O	Data Inputs / Outputs - Registered on the rising edge of CK during write operations. Driven from the rising edge of CK during read operations. DQa - indicates Data Byte a DQb - indicates Data Byte b DQc - indicates Data Byte c DQd - indicates Data Byte d DQe - indicates Data Byte e DQf - indicates Data Byte f DQg - indicates Data Byte g DQh - indicates Data Byte h
CK, $\overline{CK}$	Input	Differential Input Clocks
CQ, $\overline{CQ}$	Output	Output Clocks
$\overline{E1}$	Input	Chip Enable Control Input - Registered on the rising edge of CK. $\overline{E1}$ = 0 enables the device to accept read and write commands. $\overline{E1}$ = 1 disables the device. See the Clock Truth Table section for further information.
E2, E3	Input	Programmable Chip Enable Control Inputs - Registered on the rising edge of CK. See the Clock Truth Table and Depth Expansion sections for further information.
EP2, EP3	Input	Programmable Chip Enable Active-Level Select Inputs - These pins must be tied “high” or “low” at power-up. See the Clock Truth Table and Depth Expansion sections for further information.
ADV	Input	Address Advance Control Input - Registered on the rising edge of CK. ADV = 0 loads a new address and begins a new operation when the device is enabled. ADV = 1 increments the address and continues the previous operation when the device is enabled. See the Clock Truth Table section for further information.
$\overline{W}$	Input	Write Enable Control Input - Registered on the rising edge of CK. $\overline{W}$ = 0 specifies a write operation when ADV = 0 and the device is enabled. $\overline{W}$ = 1 specifies a read operation when ADV = 0 and the device is enabled. See the Clock Truth Table section for further information.
$\overline{BW}$a, $\overline{BW}$b $\overline{BW}$c, $\overline{BW}$d $\overline{BW}$e, $\overline{BW}$f $\overline{BW}$g, $\overline{BW}$h	Input	Byte Write Enable Control Inputs - Registered on the rising edge of CK. $\overline{BW}$a = 0 specifies write Data Byte a during a write operation $\overline{BW}$b = 0 specifies write Data Byte b during a write operation $\overline{BW}$c = 0 specifies write Data Byte c during a write operation $\overline{BW}$d = 0 specifies write Data Byte d during a write operation $\overline{BW}$e = 0 specifies write Data Byte e during a write operation $\overline{BW}$f = 0 specifies write Data Byte f during a write operation $\overline{BW}$g = 0 specifies write Data Byte g during a write operation $\overline{BW}$h = 0 specifies write Data Byte h during a write operation See the Clock Truth Table section for further information.
$\overline{SD}$	Input	Slow Down Output Control Input - This pin must be tied “high” or “low” at power-up. $\overline{SD}$ = 1 selects fast Input Clock to Output Data and Output Clock Valid/Hold times. $\overline{SD}$ = 0 selects slow Input Clock to Output Data and Output Clock Valid/Hold times. See the AC Electrical Characteristics section for further information.
M2, M3, M4	Input	Operation Protocol Control Inputs - These pins must be tied “high”, “low”, and “high” respectively, at power-up, to select Single Data Rate Pipelined Read / Double Late Write operation protocol.

Symbol	Type	Description
ZQ	Input	Output Impedance Control Resistor Input - This pin must be tied to V_{SS} through an external impedance matching resistor RQ at power-up. Output driver impedance is set to one-fifth the value of the RQ resistor, nominally. See the Output Driver Impedance Control section for further information.
V_{DD}		1.8V Core Power Supply - Core supply voltage.
V_{DDQ}		Output Power Supply - Output buffer supply voltage.
V_{REF}		Input Reference Voltage - Input buffer threshold voltage.
V_{SS}		Ground
TCK	Input	JTAG Clock
TMS	Input	JTAG Mode Select
TDI	Input	JTAG Data In
TDO	Output	JTAG Data Out
MCL	*Input*	Must Connect “Low” - May not be actual input pins.
MCH	*Input*	Must Connect “High” - May not be actual input pins.
NC		No Connect - These pins are true no-connects, i.e. there is no internal chip connection to these pins. They can be left unconnected or tied directly to V_{DD}, V_{DDQ}, or V_{SS}.

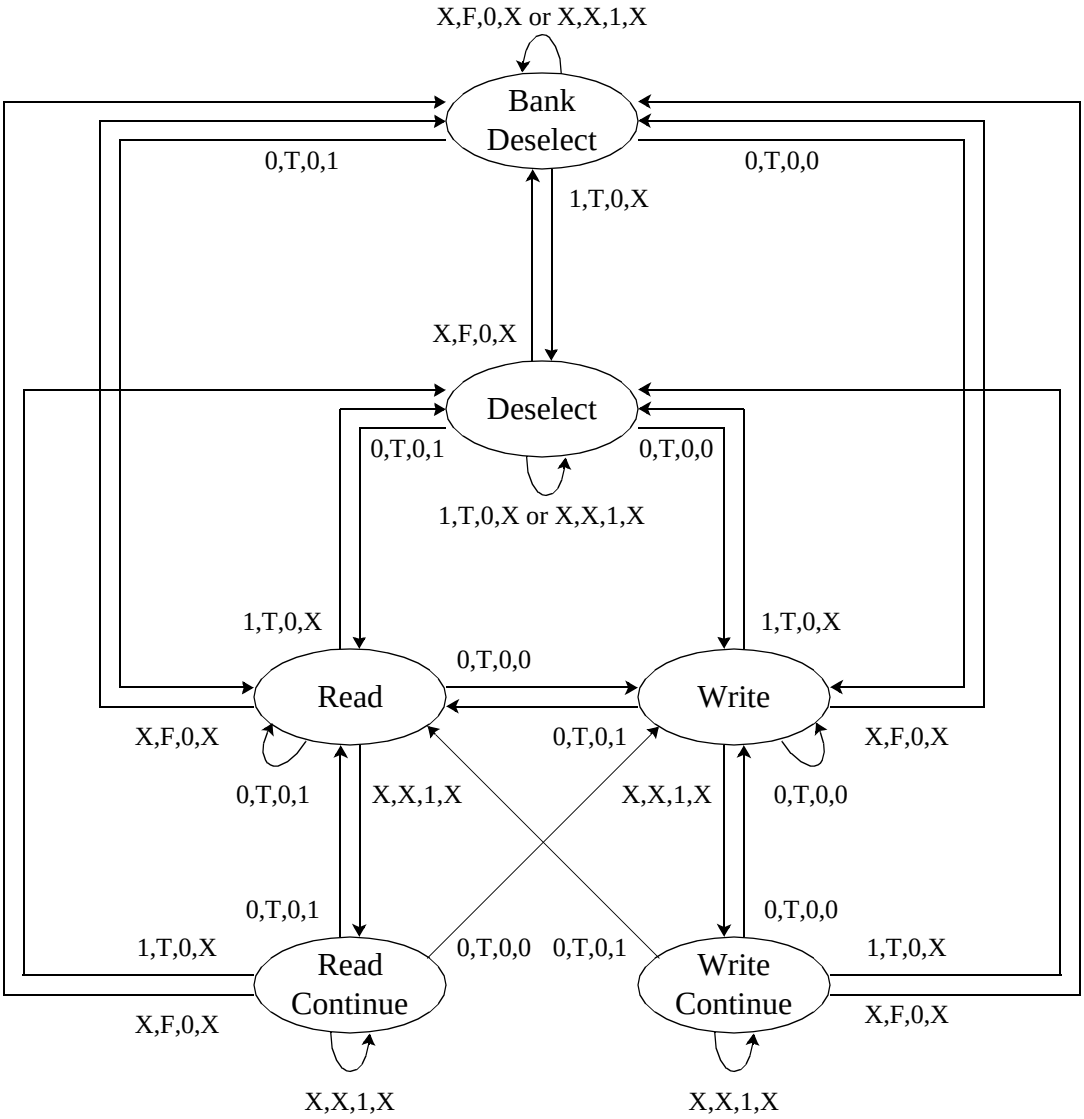
Clock Truth Table

CK	$\overline{E1}$ (t_n)	E (t_n)	ADV (t_n)	$\overline{W}$ (t_n)	BW (t_n)	Previous Operation	Current Operation	DQ(t_n) / CQ(t_n)	DQ(t_{n+1}) / CQ(t_{n+1})	DQ(t_{n+2}) / CQ(t_{n+2})
0→1	X	F	0	X	X	X	Bank Deselect	***	Hi-Z	---
								***	Hi-Z	---
0→1	X	X	1	X	X	Bank Deselect	Bank Deselect (Continue)	Hi-Z	Hi-Z	---
								Hi-Z	Hi-Z	---
0→1	1	T	0	X	X	X	Deselect	***	Hi-Z	---
								***	CQ	---
0→1	X	X	1	X	X	Deselect	Deselect (Continue)	Hi-Z	Hi-Z	---
								CQ	CQ	---
0→1	0	T	0	0	T	X	Write Loads new address Stores DQx if $\overline{BW}$x = 0	***	***	D1(t_n)
								***	CQ	---
0→1	0	T	0	0	F	X	Write (Abort) Loads new address No data stored	***	***	Hi-Z
								***	CQ	---
0→1	X	X	1	X	T	Write	Write Continue Increments address by 1 Stores DQx if $\overline{BW}$x = 0	***	D1(t_{n-1})	D2(t_n)
								CQ	CQ	---
0→1	X	X	1	X	F	Write	Write Continue (Abort) Increments address by 1 No data stored	***	D1(t_{n-1})	Hi-Z
								CQ	CQ	---
0→1	0	T	0	1	X	X	Read Loads new address	***	Q1(t_n)	---
								***	CQ	---
0→1	X	X	1	X	X	Read	Read Continue Increments address by 1	Q1(t_{n-1})	Q2(t_n)	---
								CQ	CQ	---

Notes:

1. If E2 = EP2 and E3 = EP3 then E = “T” else E = “F”.
2. If one or more $\overline{BW}$x = 0 then BW = “T” else BW = “F”.
3. “1” = input “high”; “0” = input “low”; “X” = input “don’t care”; “T” = input “true”; “F” = input “false”.
4. “***” indicates that the DQ input requirement / output state and CQ output state are determined by the previous operation.
5. “---” indicates that the DQ input requirement / output state and CQ output state are determined by the next operation.
6. DQs are tri-stated in response to Bank Deselect, Deselect, and Write commands, one full cycle after the command is sampled.
7. CQs are tri-stated in response to Bank Deselect commands only, one full cycle after the command is sampled.
8. Up to three (3) Continue operations may be initiated after a Read or Write operation is initiated to burst transfer up to four (4) distinct pieces of data per single external address input. If a fourth (4th) Continue operation is initiated, the internal address wraps back to the initial external (base) address.

State Diagram



Notes:

1. The notation "X,X,X,X" controlling the state transitions above indicate the states of inputs $\overline{E1}$, E, ADV, and $\overline{W}$ respectively.
2. If (E2 = EP2 and E3 = EP3) then E = "T" else E = "F".
3. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".

•Burst (Continue) Operations

Burst operations follow the **Linear Burst** address sequence depicted in the table below:

	A(1:0)				Sequence Key
1st (Base) Address	00	01	10	11	A1, A0
2nd Address	01	10	11	00	(A1 xor A0), $\overline{A0}$
3rd Address	10	11	00	01	$\overline{A1}$, A0
4th Address	11	00	01	10	$\overline{(A1 \text{ xor } A0)}$, $\overline{A0}$

Up to three (3) Continue operations may be initiated after a Read or Write operation is initiated to burst transfer up to four (4) distinct pieces of data per single external address input. If a fourth (4th) Continue operation is initiated, the internal address wraps back to the initial external (base) address.

•Depth Expansion

Depth expansion in these devices is supported via programmable chip enables E2 and E3. The active levels of E2 and E3 are programmable through the static inputs EP2 and EP3 respectively. When EP2 is tied “high”, E2 functions as an active-high input. When EP2 is tied “low”, E2 functions as an active-low input. Similarly, when EP3 is tied “high”, E3 functions as an active-high input. And, when EP3 is tied “low”, E3 functions as an active-low input.

The programmability of E2 and E3 allows four banks of depth expansion to be accomplished with no additional logic. By programming E2 and E3 of four devices in a binary sequence (00, 01, 10, 11), and by driving E2 and E3 with external address signals, the four devices can be made to look like one larger device.

When these devices are deselected via chip enable $\overline{E1}$, the output clocks continue to toggle. However, when these devices are deselected via programmable chip enables E2 or E3, the output clocks are forced to a Hi-Z state. See the Clock Truth Table for further information.

•Output Driver Impedance Control

The impedance of the data and clock output drivers in these devices can be controlled via the static input ZQ. When an external impedance matching resistor (RQ) is connected between ZQ and V_{SS}, output driver impedance is set to one-fifth the value of the resistor, nominally. See the DC Electrical Characteristics section for further information.

Output driver impedance is updated whenever the data output drivers are in an inactive (High-Z) state. See the Clock Truth Table section for information concerning which commands deactivate the data output drivers.

At power up, 8192 clock cycles followed by any command that deactivates the data output drivers are required to ensure that the output impedance has reached the desired value.

Note: The impedance of the output drivers will drift somewhat due to changes in temperature and voltage. Consequently, during operation, the output drivers should be deactivated periodically in order to update the output impedance and ensure that it remains within specified tolerances.

•Power-Up Sequence

For reliability purposes, Sony recommends that power supplies power up in the following sequence: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, and Inputs. V_{DDQ} should never exceed V_{DD}. If this power supply sequence cannot be met, a large bypass diode may be required between V_{DD} and V_{DDQ}. Please contact Sony Memory Application Department for further information.

•Absolute Maximum Ratings(1)

Item	Symbol	Rating	Units
Supply Voltage	V_{DD}	-0.5 to +2.5	V
Output Supply Voltage	V_{DDQ}	-0.5 to +2.3	V
Input Voltage (Address, Control, Data, Clock)	V_{IN}	-0.5 to V_{DDQ}+0.5 (2.3V max)	V
Input Voltage (EP(2:3), $\overline{SD}$, M(2:4))	V_{MIN}	-0.5 to V_{DD}+0.5 (2.5V max)	V
Input Voltage (TCK, TMS, TDI)	V_{TIN}	-0.5 to V_{DD}+0.5 (2.5V max)	V
Operating Temperature	T_A	0 to 85	°C
Junction Temperature	T_J	0 to 110	°C
Storage Temperature	T_{STG}	-55 to 150	°C

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

•DC Recommended Operating Conditions

(V_{SS} = 0V, T_A = 0 to 85°C)

Item	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
Output Supply Voltage	$V_{DDQ-1.8}$	1.7	1.8	V_{DD}	V	1
	$V_{DDQ-1.5}$	1.4	1.5	1.6	V	2
Input Reference Voltage	$V_{REF-1.8}$	0.8	0.9	1.0	V	1,3
	$V_{REF-1.5}$	0.65	0.75	0.85	V	2,3
Input High Voltage (Address, Control, Data)	V_{IH}	V_{REF} + 0.2	---	V_{DDQ} + 0.3	V	4
Input Low Voltage (Address, Control, Data)	V_{IL}	-0.3	---	V_{REF} - 0.2	V	5
Input High Voltage (EP(2:3), $\overline{SD}$, M(2:4))	V_{MIH}	V_{REF} + 0.3	---	V_{DD} + 0.3	V	
Input Low Voltage (EP(2:3), $\overline{SD}$, M(2:4))	V_{MIL}	-0.3	---	V_{REF} - 0.3	V	
Clock Input Signal Voltage	V_{KIN}	-0.3	---	V_{DDQ} + 0.3	V	
Clock Input Differential Voltage	V_{DIF}	0.4	---	V_{DDQ} + 0.6	V	
Clock Input Common Mode Voltage	$V_{CM-1.8}$	0.8	0.9	1.0	V	1
	$V_{CM-1.5}$	0.65	0.75	0.85	V	2

1. Parameter applies when V_{DDQ} = 1.8V nominally (for 1.8V HSTL I/O).
2. Parameter applies when V_{DDQ} = 1.5V nominally (for 1.5V HSTL I/O).
3. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component.
4. V_{IH} (max) AC = +1.5*V_{DDQ} for pulse widths less than one-quarter of the cycle time (t_{CYC}/4).
5. V_{IL} (min) AC = -0.5*V_{DDQ} for pulse widths less than one-quarter of the cycle time (t_{CYC}/4).

•DC Electrical Characteristics

(V_{DD} = 1.8V ± 0.1V, V_{SS} = 0V, T_A = 0 to 85°C)

Item	Symbol	Test Conditions	Min	Typ	Max	Units
Input Leakage Current (Address, Control, Clock)	I_{LI}	V_{IN} = V_{SS} to V_{DDQ}	-5	---	5	uA
Input Leakage Current (EP2, EP3, M2, M3, M4)	I_{MLI}	V_{MIN} = V_{SS} to V_{DD}	-10	---	10	uA
Input Leakage Current (Data)	I_{DLI}	V_{DIN} = V_{SS} to V_{DDQ}	-10	---	10	uA
Average Power Supply Operating Current (x72)	I_{DD-33} I_{DD-4} I_{DD-44}	I_{OUT} = 0 mA V_{IN} = V_{IH} or V_{IL}	--- --- ---	--- --- ---	850 750 700	mA
Average Power Supply Operating Current (x36)	I_{DD-33} I_{DD-4} I_{DD-44}	I_{OUT} = 0 mA V_{IN} = V_{IH} or V_{IL}	--- --- ---	--- --- ---	630 550 510	mA
Average Power Supply Operating Current (x18)	I_{DD-33} I_{DD-4} I_{DD-44}	I_{OUT} = 0 mA V_{IN} = V_{IH} or V_{IL}	--- --- ---	--- --- ---	510 450 420	mA
Power Supply Deselect Operating Current (NOP Current)	I_{DD2}	I_{OUT} = 0 mA V_{IN} = V_{IH} or V_{IL}	---	---	250	mA
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA RQ = 250Ω	V_{DDQ}-0.4	---	---	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA RQ = 250Ω	---	---	0.4	V
Output Driver Impedance	R_{OUT}	V_{OH}, V_{OL} = V_{DDQ}/2 150Ω ≤ RQ ≤ 300Ω	(RQ/5)* 0.85	RQ/5	(RQ/5)* 1.15	Ω

•I/O Capacitance

(T_A = 25°C, f = 1 MHz)

Item		Symbol	Test conditions	Min	Max	Units
Input Capacitance	Address	C_A	V_{IN} = 0V	---	3.5	pF
	Control	C_B	V_{IN} = 0V	---	3.5	pF
	CK Clock	C_{CK}	V_{IN} = 0V	---	3.5	pF
Output Capacitance	Data	C_{DQ}	V_{OUT} = 0V	---	4.5	pF
	CQ Clock	C_{CQ}	V_{OUT} = 0V	---	4.5	pF

Note: These parameters are sampled and are not 100% tested.

•AC Electrical Characteristics

(T_A = 0 to 85°C)

Parameter	Symbol	-33		-4		-44		Units	Notes
		Min	Max	Min	Max	Min	Max		
Input Clock Cycle Time	t_{KHKH}	3.3	---	4.0	---	4.4	---	ns	
Input Clock High Pulse Width	t_{KHKL}	1.3	---	1.5	---	1.5	---	ns	
Input Clock Low Pulse Width	t_{KLKH}	1.3	---	1.5	---	1.5	---	ns	
Address Input Setup Time	t_{AVKH}	0.7	---	0.8	---	0.8	---	ns	
Address Input Hold Time	t_{KHAX}	0.4	---	0.5	---	0.5	---	ns	
Control Input Setup Time	t_{BVKH}	0.7	---	0.8	---	0.8	---	ns	1
Control Input Hold Time	t_{KHBX}	0.4	---	0.5	---	0.5	---	ns	1
Data Input Setup Time	t_{DVKH}	0.7	---	0.8	---	0.8	---	ns	
Data Input Hold Time	t_{KHDX}	0.4	---	0.5	---	0.5	---	ns	
Input Clock High to Output Data Valid $\overline{SD}$ = 1 $\overline{SD}$ = 0	t_{KHQV}	--- ---	1.8 2.7	--- ---	2.1 3.0	--- ---	2.3 3.2	ns	
Input Clock High to Output Data Hold $\overline{SD}$ = 1 $\overline{SD}$ = 0	t_{KHQX}	0.5 1.1	---	0.5 1.1	---	0.5 1.1	---	ns	2
Input Clock High to Output Data Low-Z $\overline{SD}$ = 1 $\overline{SD}$ = 0	t_{KHQX1}	0.5 1.1	---	0.5 1.1	---	0.5 1.1	---	ns	2,3
Input Clock High to Output Data High-Z $\overline{SD}$ = 1 $\overline{SD}$ = 0	t_{KHQZ}	0.5 1.1	1.8 2.7	0.5 1.1	2.1 3.0	0.5 1.1	2.3 3.2	ns	2,3
Input Clock High to Output Clock High $\overline{SD}$ = 1 $\overline{SD}$ = 0	t_{KHCH}	0.5 1.1	1.7 2.6	0.5 1.1	2.0 2.9	0.5 1.1	2.2 3.1	ns	
Input Clock High to Output Clock Low-Z $\overline{SD}$ = 1 $\overline{SD}$ = 0	t_{KHCX1}	0.5 1.1	---	0.5 1.1	---	0.5 1.1	---	ns	2,3
Input Clock High to Output Clock High-Z $\overline{SD}$ = 1 $\overline{SD}$ = 0	t_{KHCZ}	0.5 1.1	1.7 2.6	0.5 1.1	2.0 2.9	0.5 1.1	2.2 3.1	ns	2,3
Output Clock High to Output Data Valid	t_{CHQV}	---	0.4	---	0.5	---	0.5	ns	2
Output Clock High to Output Data Hold	t_{CHQX}	-0.4	---	-0.5	---	-0.5	---	ns	2
Output Clock High Pulse Width	t_{CHCL}	$t_{KHKL} \pm 0.2$		$t_{KHKL} \pm 0.25$		$t_{KHKL} \pm 0.25$		ns	2
Output Clock Low Pulse Width	t_{CLCH}	$t_{KLKH} \pm 0.2$		$t_{KLKH} \pm 0.25$		$t_{KLKH} \pm 0.25$		ns	2

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal, unless otherwise noted.

1. These parameters apply to control inputs $\overline{E1}$, E2, E3, ADV, $\overline{W}$, and $\overline{BW}$x.
2. These parameters are verified through device characterization, and are not 100% tested.
3. These parameters are measured at ± 50mV from steady state voltage.

•AC Electrical Characteristics (Note)

The two AC timing parameters listed below are tested according to specific combinations of Output Clocks (CQs) and Output Data (DQs):

1. t_{CHQV} - Output Clock High to Output Data Valid (max)
2. t_{CHQX} - Output Clock High to Output Data Hold (min)

The specific CQ / DQ combinations are defined as follows:

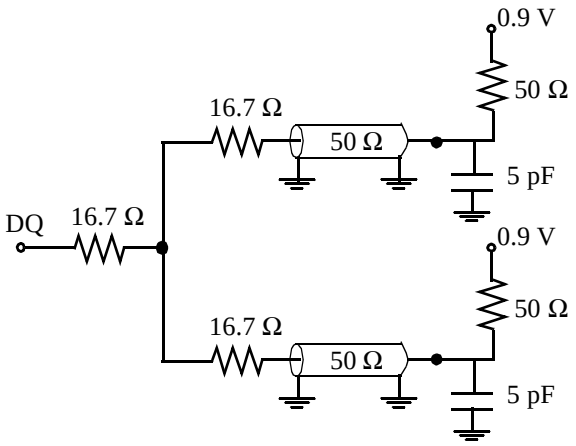
256Kb x 72		512Kb x 36		1Mb x 18	
CQs	DQs	CQs	DQs	CQs	DQs
1K, 2K	1A, 2A, 1B, 2B, 1C, 2C, 1D, 2D, 1E, 2E, 1F, 2F, 1G, 2G, 1H, 2H, 1J, 2J, 1L, 2L, 1M, 2M, 1N, 2N, 1P, 2P, 2R, 1R, 1T, 2T, 1U, 2U, 1V, 2V, 1W, 2W	1K, 2K	2E, 1F, 2F, 1G, 2G, 1H, 2H, 1J, 2J, 1R, 1T, 2T, 1U, 2U, 1V, 2V, 1W, 2W	1K, 2K	2E, 1F, 2F, 1G, 2G, 1H, 2H, 1J, 2J
10K, 11K	10A, 11A, 10B, 11B, 10C, 11C, 10D, 11D, 11E, 10E, 10F, 11F, 10G, 11G, 10H, 11H, 10J, 11J, 10L, 11L, 10M, 11M, 10N, 11N, 10P, 11P, 10R, 11R, 10T, 11T, 10U, 11U, 10V, 11V, 10W, 11W	10K, 11K	10A, 11A, 10B, 11B, 10C, 11C, 10D, 11D, 11E, 10L, 11L, 10M, 11M, 10N, 11N, 10P, 11P, 10R	10K, 11K	10L, 11L, 10M, 11M, 10N, 11N, 10P, 11P, 10R

•AC Test Conditions (V_{DDQ} = 1.8V)

(V_{DD} = 1.8V ± 0.1V, V_{DDQ} = 1.8V ± 0.1V, T_A = 0 to 85°C)

Item	Symbol	Conditions	Units	Notes
Input Reference Voltage	V_{REF}	0.9	V	
Input High Level	V_{IH}	1.4	V	
Input Low Level	V_{IL}	0.4	V	
Input Rise & Fall Time		2.0	V/ns	
Input Reference Level		0.9	V	
Clock Input High Voltage	V_{KIH}	1.4	V	V_{DIF} = 1.0V
Clock Input Low Voltage	V_{KIL}	0.4	V	V_{DIF} = 1.0V
Clock Input Common Mode Voltage	V_{CM}	0.9	V	
Clock Input Rise & Fall Time		2.0	V/ns	
Clock Input Reference Level		CK/$\overline{CK}$ cross	V	
Output Reference Level		0.9	V	
Output Load Conditions		RQ = 250Ω		See Figure 1 below

Figure 1: AC Test Output Load (V_{DDQ} = 1.8V)

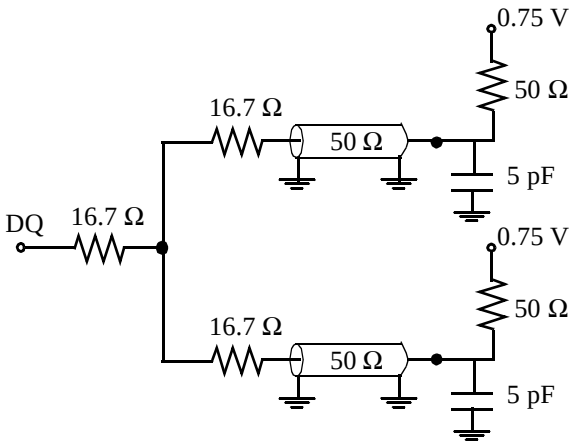


•AC Test Conditions (V_{DDQ} = 1.5V)

(V_{DD} = 1.8V ± 0.1V, V_{DDQ} = 1.5V ± 0.1V, T_A = 0 to 85°C)

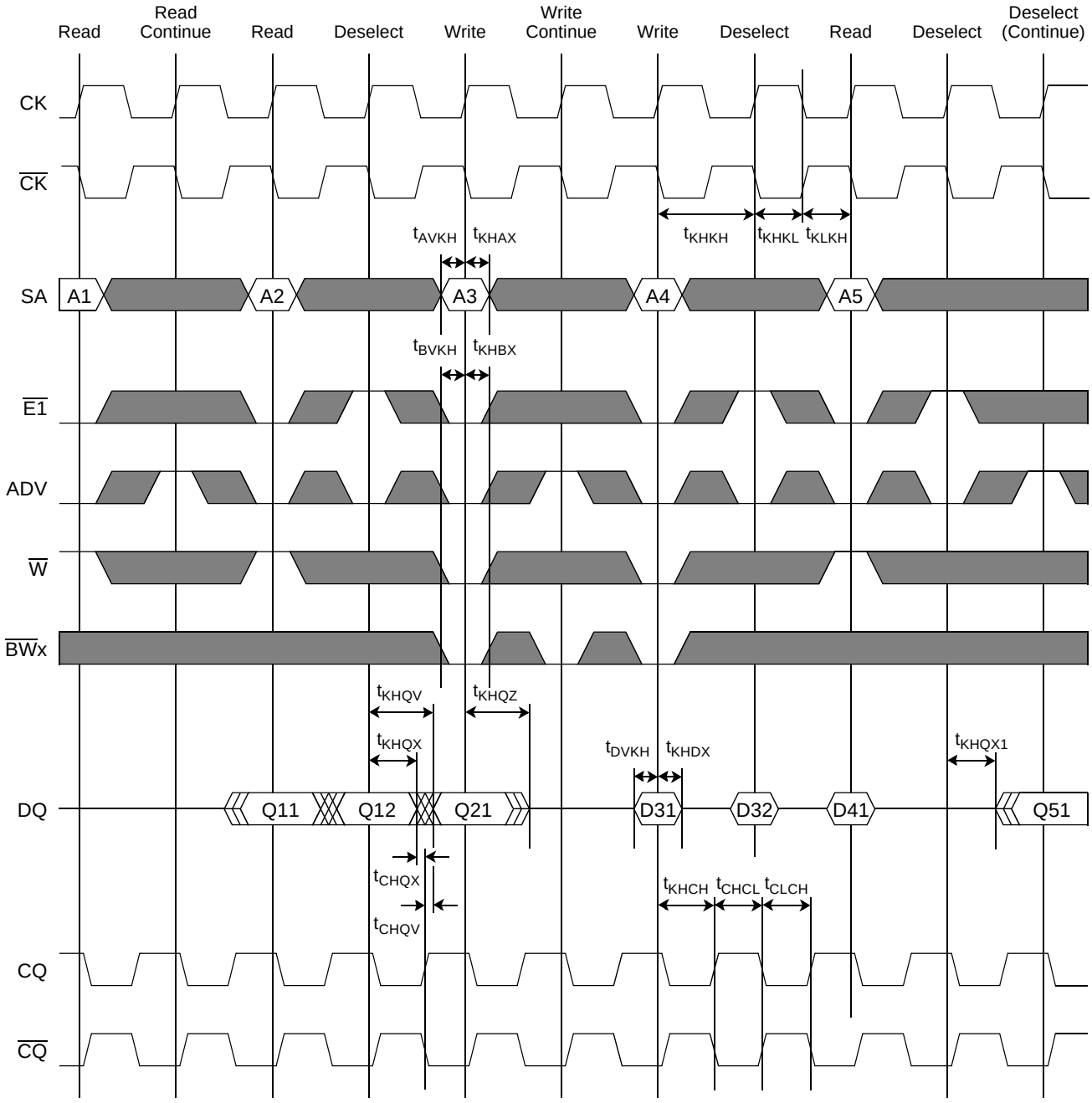
Item	Symbol	Conditions	Units	Notes
Input Reference Voltage	V_{REF}	0.75	V	
Input High Level	V_{IH}	1.25	V	
Input Low Level	V_{IL}	0.25	V	
Input Rise & Fall Time		2.0	V/ns	
Input Reference Level		0.75	V	
Clock Input High Voltage	V_{KIH}	1.25	V	V_{DIF} = 1.0V
Clock Input Low Voltage	V_{KIL}	0.25	V	V_{DIF} = 1.0V
Clock Input Common Mode Voltage	V_{CM}	0.75	V	
Clock Input Rise & Fall Time		2.0	V/ns	
Clock Input Reference Level		CK/$\overline{CK}$ cross	V	
Output Reference Level		0.75	V	
Output Load Conditions		RQ = 250Ω		See Figure 2 below

Figure 2: AC Test Output Load (V_{DDQ} = 1.5V)



Timing Diagram of Read-Write-Read Operations
One Bank Example
(E2 = EP2 and E3 = EP3)

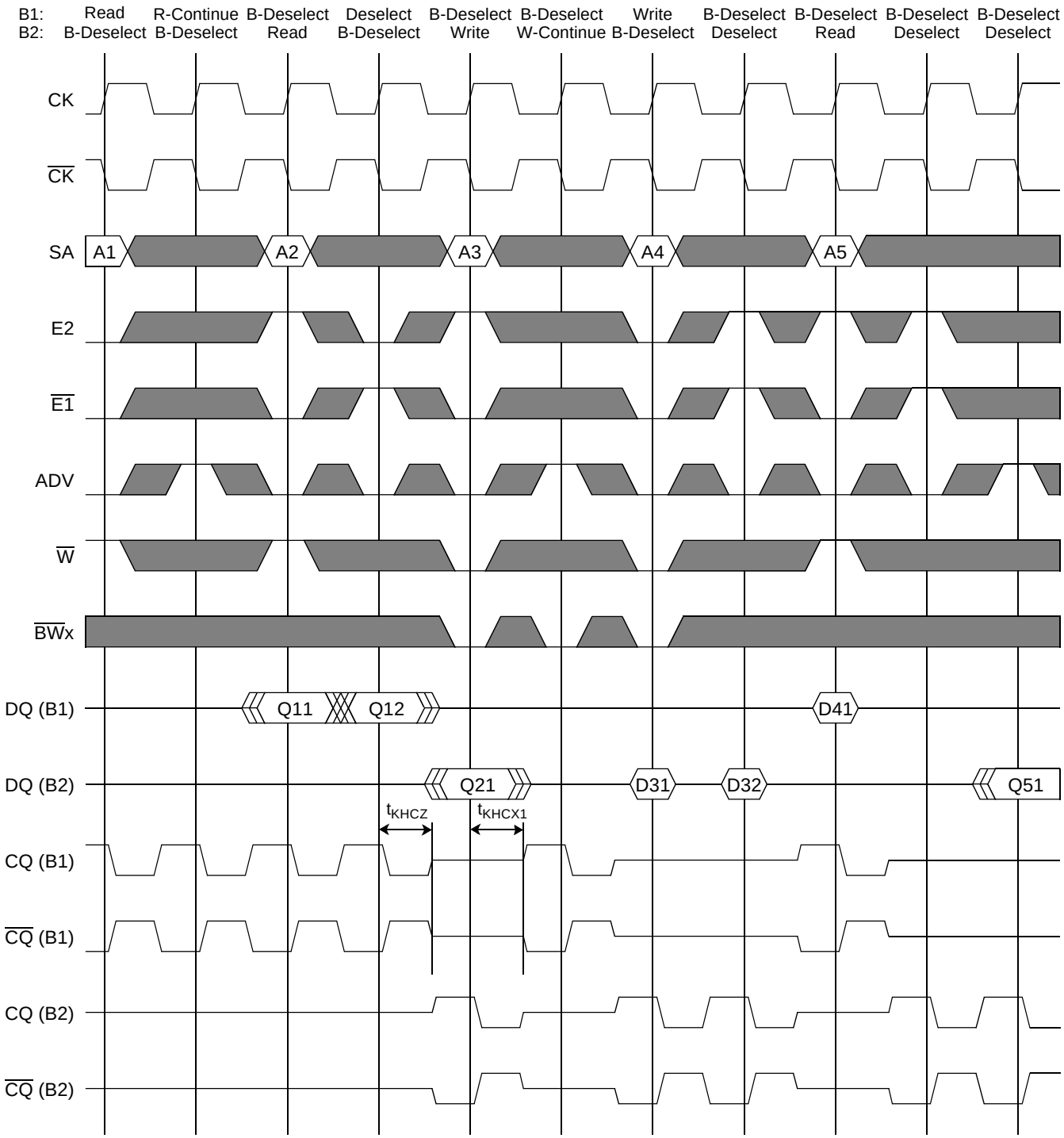
Figure 3



Note: In the diagram above, a Deselect operation is inserted between Read and Write operations to control the data bus transition from output to input. Similarly, a Deselect operation is inserted between Write and Read operations to control the data bus transition from input to output. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, these Deselect operations may not be necessary.

Timing Diagram of Read-Write-Read Operations
Two Bank Example
(Bank 1: EP2 Low and E3 = EP3, Bank 2: EP2 High and E3 = EP3)

Figure 4



Note: In the diagram above, a Deselect operation is inserted between Read and Write operations to control the data bus transition from output to input. Similarly, a Deselect operation is inserted between Write and Read operations to control the data bus transition from input to output. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, these Deselect operations may not be necessary.

•Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components, and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and four TAP Registers. The TAP Registers consist of one Instruction Register and three Data Registers (ID, Bypass, and Boundary Scan Registers).

The TAP consists of the following four signals:

TCK:	Test Clock	Induces (clocks) TAP Controller state transitions.
TMS:	Test Mode Select	Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.
TDI:	Test Data In	Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.
TDO:	Test Data Out	Outputs data serially from the TAP Registers. Driven from the falling edge of TCK.

Disabling the TAP

When JTAG is not used, TCK should be tied “low” to prevent clocking the SRAM. TMS and TDI should either be tied “high” through a pull-up resistor or left unconnected. TDO should be left unconnected.

Note: Operation of the TAP does not disrupt normal SRAM operation except when the EXTEST-A or SAMPLE-Z instruction is selected. Consequently, TCK, TMS, and TDI can be controlled any number of ways without adversely affecting the functionality of the device.

JTAG DC Recommended Operating Conditions

(V_{DD} = 1.8V ± 0.1V, T_A = 0 to 85°C)

Parameter	Symbol	Test Conditions	Min	Max	Units
JTAG Input High Voltage	V_{TIH}	---	1.2	V_{DD} + 0.3	V
JTAG Input Low Voltage	V_{TIL}	---	-0.3	0.6	V
JTAG Output High Voltage (CMOS)	V_{TOH}	I_{TOH} = -100uA	V_{DD} - 0.1	---	V
JTAG Output Low Voltage (CMOS)	V_{TOL}	I_{TOL} = 100uA	---	0.1	V
JTAG Output High Voltage (TTL)	V_{TOH}	I_{TOH} = -8mA	V_{DD} - 0.4	---	V
JTAG Output Low Voltage (TTL)	V_{TOL}	I_{TOL} = 8mA	---	0.4	V
JTAG Input Leakage Current	I_{TLI}	V_{TIN} = V_{SS} to V_{DD}	-10	10	uA

JTAG AC Test Conditions

(V_{DD} = 1.8V ± 0.1V, T_A = 0 to 85°C)

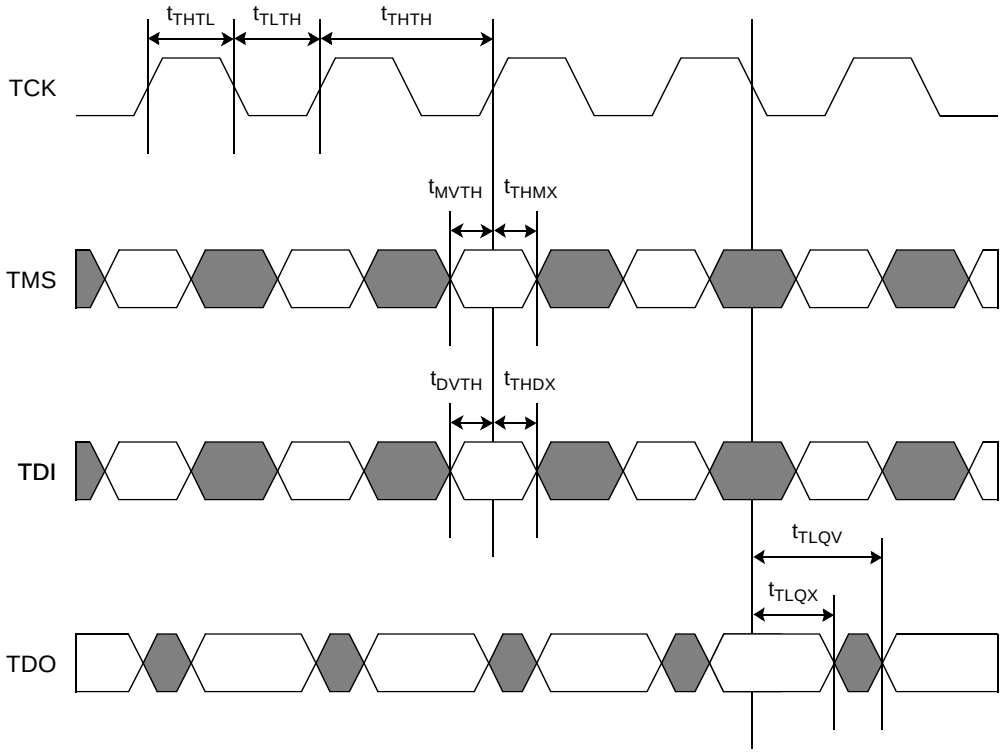
Parameter	Symbol	Conditions	Units	Notes
JTAG Input High Level	V_{TIH}	1.8	V	
JTAG Input Low Level	V_{TIL}	0.0	V	
JTAG Input Rise & Fall Time		1.0	V/ns	
JTAG Input Reference Level		0.9	V	
JTAG Output Reference Level		0.9	V	
JTAG Output Load Condition				See Figure 1 (page 14)

JTAG AC Electrical Characteristics

Parameter	Symbol	Min	Max	Units
TCK Cycle Time	t_{THTH}	20		ns
TCK High Pulse Width	t_{THTL}	8		ns
TCK Low Pulse Width	t_{TLTH}	8		ns
TMS Setup Time	t_{MVTH}	5		ns
TMS Hold TIme	t_{THMX}	5		ns
TDI Setup Time	t_{DVTH}	5		ns
TDI Hold TIme	t_{THDX}	5		ns
TCK Low to TDO Valid	t_{TLQV}		10	ns
TCK Low to TDO Hold	t_{TLQX}	0		ns

JTAG Timing Diagram

Figure 5



TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: “Instruction Registers”, of which there is one - the Instruction Register, and “Data Registers”, of which there are three - the ID Register, the Bypass Register, and the Boundary Scan Register. Individual TAP registers are “selected” (inserted between TDI and TDO) when the appropriate sequence of commands is given to the TAP Controller.

Instruction Register (3 bits)

The Instruction Register stores the instructions that are executed by the TAP Controller when the TAP Controller is in the “Run-Test / Idle” state, or in any of the various “Data Register” states. It is loaded with the IDCODE instruction at power-up, or when the TAP Controller is in the “Test-Logic Reset” state or the “Capture-IR” state. It is inserted between TDI and TDO when the TAP Controller is in the “Shift-IR” state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed by the TAP Controller until the TAP Controller has reached the “Update-IR” state.

The Instruction Register is 3 bits wide, and is encoded as follows:

Code (2:0)	Instruction	Description
000	EXTEST-A	Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO. Enables the SRAM’s data and clock output drivers. Moves the portion of the Boundary Scan Register comprising the SRAM’s output signals (DQs and CQs) to the input side of the SRAM’s output register.
001	IDCODE	Inserts the ID Register between TDI and TDO.
010	SAMPLE-Z	Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO. Disables the SRAM’s data and clock output drivers.
011	BYPASS	Inserts the Bypass Register between TDI and TDO.
100	SAMPLE	Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO.
101	PRIVATE	Do not use. Reserved for manufacturer use only.
110	BYPASS	Inserts the Bypass Register between TDI and TDO.
111	BYPASS	Inserts the Bypass Register between TDI and TDO.

Bit 0 is the LSB of the Instruction Register, and Bit 2 is the MSB. When the Instruction Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Bypass Register (1 bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic “0” when the BYPASS instruction has been loaded in the the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

ID Register (32 bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the "Capture-DR" state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the "Shift-DR" state.

The ID Register is 32 bits wide, and is encoded as follows:

Device	Revision Number (31:28)	Part Number (27:12)	Sony ID (11:1)	Start Bit (0)
256Kb x 72	xxxx	TBD	0000 1110 001	1
512Kb x 36	xxxx	TBD	0000 1110 001	1
1Mb x 18	xxxx	TBD	0000 1110 001	1

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Boundary Scan Register (123 bits for x72, 84 bits for x36, 65 bits for x18)

The Boundary Scan Register is equal in length to the number of active signal connections to the SRAM (excluding the TAP pins) plus a number of place holder locations reserved for density and/or functional upgrades. The Boundary Scan Register is loaded with the contents of the SRAM's I/O ring when the EXTEST-A, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the "Capture-DR" state. It is inserted between TDI and TDO when the EXTEST-A, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the "Shift-DR" state.

The Boundary Scan Register contains the following bits:

256Kb x 72		512Kb x 36		1Mb x 18	
DQ	72	DQ	36	DQ	18
A, A1, A0	18	A, A1, A0	19	A, A1, A0	20
CK, $\overline{CK}$	2	CK, $\overline{CK}$	2	CK, $\overline{CK}$	2
CQ, $\overline{CQ}$	4	CQ, $\overline{CQ}$	4	CQ, $\overline{CQ}$	4
$\overline{E1}$, ADV, $\overline{W}$, $\overline{BW}$x	11	$\overline{E1}$, ADV, $\overline{W}$, $\overline{BW}$x	7	$\overline{E1}$, ADV, $\overline{W}$, $\overline{BW}$x	5
E2, E3, EP2, EP3	4	E2, E3, EP2, EP3	4	E2, E3, EP2, EP3	4
$\overline{SD}$, M2, M3, M4, ZQ	5	$\overline{SD}$, M2, M3, M4, ZQ	5	$\overline{SD}$, M2, M3, M4, ZQ	5
Place Holder	7	Place Holder	7	Place Holder	7

For deterministic results, all signals composing the SRAM's I/O ring must meet setup and hold times with respect to TCK (same as TDI and TMS) when sampled.

CK/$\overline{CK}$ are connected to a differential input receiver that generates a single-ended input clock signal to these devices. Therefore, in order to capture specific values for these signals in the Boundary Scan Register, they must be at opposite logic levels when sampled.

Place Holders are required for some NC pins to allow for future density and/or functional upgrades. They are connected to V_{SS} internally, regardless of pin connection externally.

The Boundary Scan Order Assignment tables that follow depict the order in which the bits from the table above are arranged in the Boundary Scan Register. In each notation, Bit 1 is the LSB bit of the register. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Boundary Scan Order Assignments
(By Exit Sequence) TBD

TAP Instructions

IDCODE

IDCODE is the default instruction loaded into the Instruction Register at power-up, and when the TAP Controller is in the "Test-Logic Reset" state.

When the IDCODE instruction is selected, a predetermined device- and manufacturer-specific identification code is loaded into the ID Register when the TAP Controller is in the "Capture-DR" state, and the ID Register is inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state.

Normal SRAM operation is not disrupted when the IDCODE instruction is selected.

BYPASS

When the BYPASS instruction is selected, a logic "0" is loaded into the Bypass Register when the TAP Controller is in the "Capture-DR" state, and the Bypass Register is inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state.

Normal SRAM operation is not disrupted when the BYPASS instruction is selected.

SAMPLE

When the SAMPLE instruction is selected, the individual logic states of all signals composing the SRAM's I/O ring (see the Boundary Scan Register description for the complete list of signals) are loaded into the Boundary Scan Register when the TAP Controller is in the "Capture-DR" state, and the Boundary Scan Register is inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state.

Normal SRAM operation is not disrupted when the SAMPLE instruction is selected.

SAMPLE-Z

When the SAMPLE-Z instruction is selected, the individual logic states of all signals composing the SRAM's I/O ring (see the Boundary Scan Register description for the complete list of signals) are loaded into the Boundary Scan Register when the TAP Controller is in the "Capture-DR" state, and the Boundary Scan Register is inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state.

Additionally, when the SAMPLE-Z instruction is selected, the SRAM's data and clock output drivers are disabled.

Consequently, normal SRAM operation is disrupted when the SAMPLE-Z instruction is selected. Read operations initiated while the SAMPLE-Z instruction is selected will fail.

EXTEST-A

When the EXTEST-A instruction is selected, the individual logic states of all signals composing the SRAM's I/O ring (see the Boundary Scan Register description for the complete list of signals) are loaded into the Boundary Scan Register when the TAP Controller is in the "Capture-DR" state, and the Boundary Scan Register is inserted between TDI and TDO when the TAP Controller is in the "Shift-DR" state.

Additionally, when the EXTEST-A instruction is selected, the SRAM's data and clock output drivers are enabled, and the portion of the Boundary Scan Register comprising the SRAM's data and clock output signals is moved to the input side of the SRAM's output register. The SRAM's input clock can then be used to transfer the Boundary Scan Register contents directly to the SRAM's output pins (the input clock controls the SRAM's output register). A single rising edge of the input clock is sufficient to transfer the data; additional rising edges have no further effect, provided the contents of the Boundary Scan Register remain unchanged.

Consequently, normal SRAM operation is disrupted when the EXTEST-A instruction is selected. Read and write operations initiated while the EXTEST-A instruction is selected will fail.

TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction (see Figure 7 below). State transitions are controlled by TMS and occur on the rising edge of TCK.

The TAP Controller enters the “Test-Logic Reset” state in one of two ways:

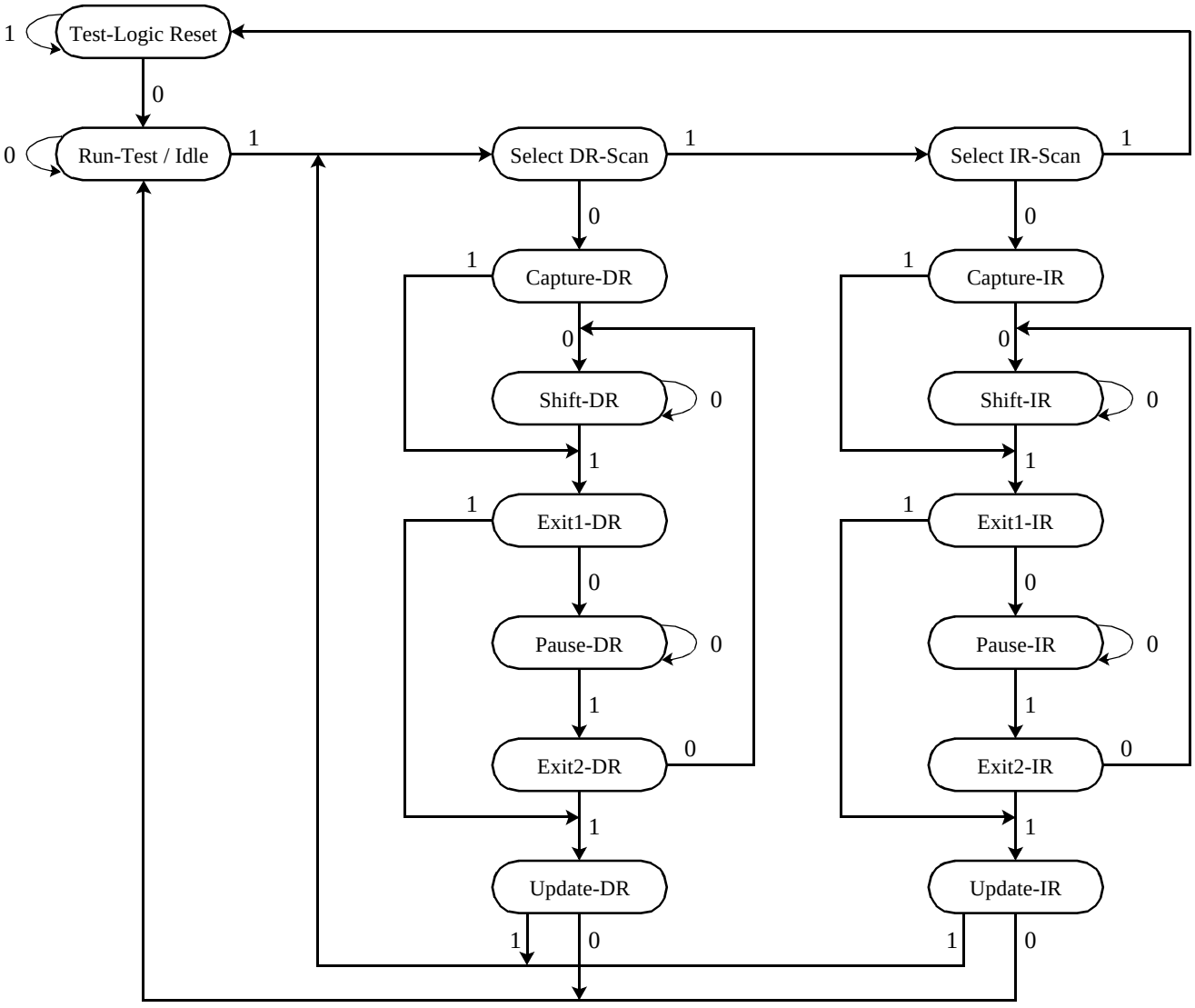
1. At power up.
2. When a logic “1” is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the “Shift-IR” state or the “Shift-DR” state.

The TDO output driver is active only when the TAP Controller is in either the “Shift-IR” state or the “Shift-DR” state.

TAP Controller State Diagram

Figure 6

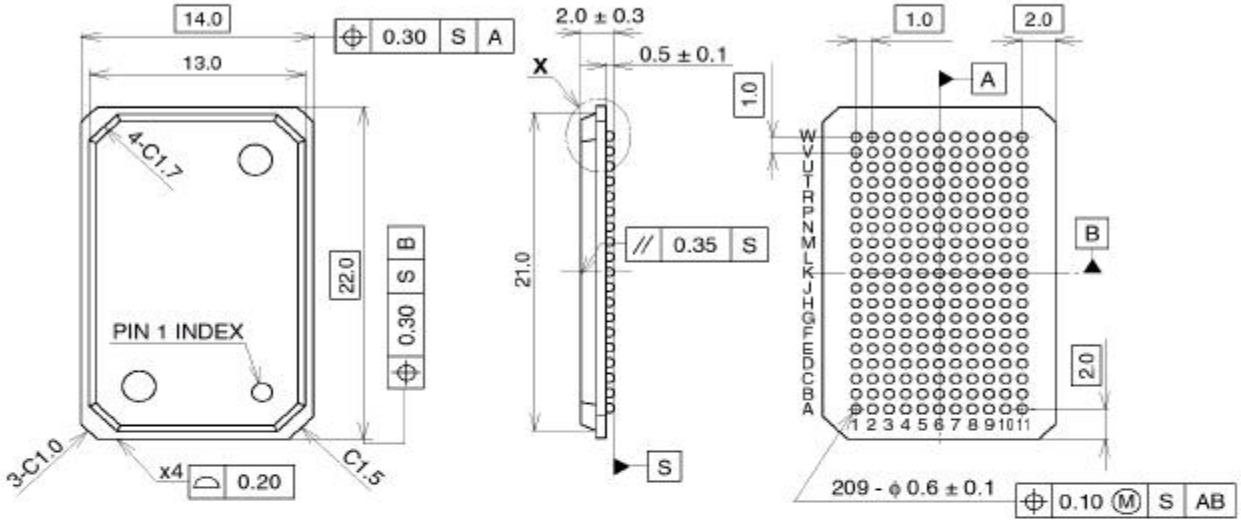


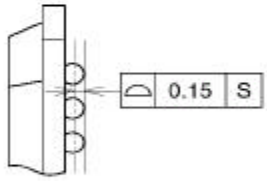
•Ordering Information

Part Number	V_{DD}	I/O Type	Configuration	Speed (Cycle Time / Data Access Time)
CXK79M72C164GB-33	1.8V	HSTL	256Kb x 72	3.3ns / 1.8ns
CXK79M72C164GB-4	1.8V	HSTL	256Kb x 72	4.0ns / 2.1ns
CXK79M72C164GB-44	1.8V	HSTL	256Kb x 72	4.4ns / 2.3ns
CXK79M36C164GB-33	1.8V	HSTL	512Kb x 36	3.3ns / 1.8ns
CXK79M36C164GB-4	1.8V	HSTL	512Kb x 36	4.0ns / 2.1ns
CXK79M36C164GB-44	1.8V	HSTL	512Kb x 36	4.4ns / 2.3ns
CXK79M18C164GB-33	1.8V	HSTL	1Mb x 18	3.3ns / 1.8ns
CXK79M18C164GB-4	1.8V	HSTL	1Mb x 18	4.0ns / 2.1ns
CXK79M18C164GB-44	1.8V	HSTL	1Mb x 18	4.4ns / 2.3ns

•(11x19) 209 Pin BGA Package Dimensions

209PIN BGA (PLASTIC)





DETAIL X

PRELIMINARY

SONY CODE	BGA-209P-01
JEITA CODE	P-BGA209-14X22-1.0
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	COPPER-CLAD LAMINATE
TERMINAL MATERIAL	SOLDER
PACKAGE MASS	1.1g

•Revision History

Rev. #	Rev. Date	Description of Modifications
rev 0.0	02/23/01	Initial Version.
rev 0.1	07/06/01	1. Modified DC Electrical Characteristics section (p. 11). Added I_{DD-33} and I_{DD-44} Average Power Supply Operating Current specifications. 2. Added Slow Down pin ($\overline{SD}$) and associated AC Electrical Characteristics (p. 12). 3. Added 209 Pin BGA Package Dimensions (p. 26).