SONY

High Cap Switchable Step Capacitor (SPI 32-bit) For Antenna Tuning

CXM3604UR

Description

This product has single 5-bit capacitor array with high accuracy.
Sony GaAs JPHEMT process is utilized for antenna tuning solution which needs high linearity and high Quality factor.

Features

- ◆5 bits resolution Switchable Step Capacitor
- ◆High power handling and High linearity
- ◆High Q factor and High accuracy capacitor (+/-5 % typ.)
- ◆Low insertion loss
- ◆Through path
- ◆Standby mode (Wakeup time < 40 µs)
- ◆Applicable frequency 100 MHz to 3 GHz
- ◆SPI 32-bit interface (1.8 V typ.)
- ◆Low voltage operation : 2.4 V to 3.3 V
- ◆Small package: UQFN-12P (2.2 mm × 2.2 mm × 0.6 mm Max.)
- ◆Robustness against ESD
- ◆Lead-Free and RoHS Compliant

Structure

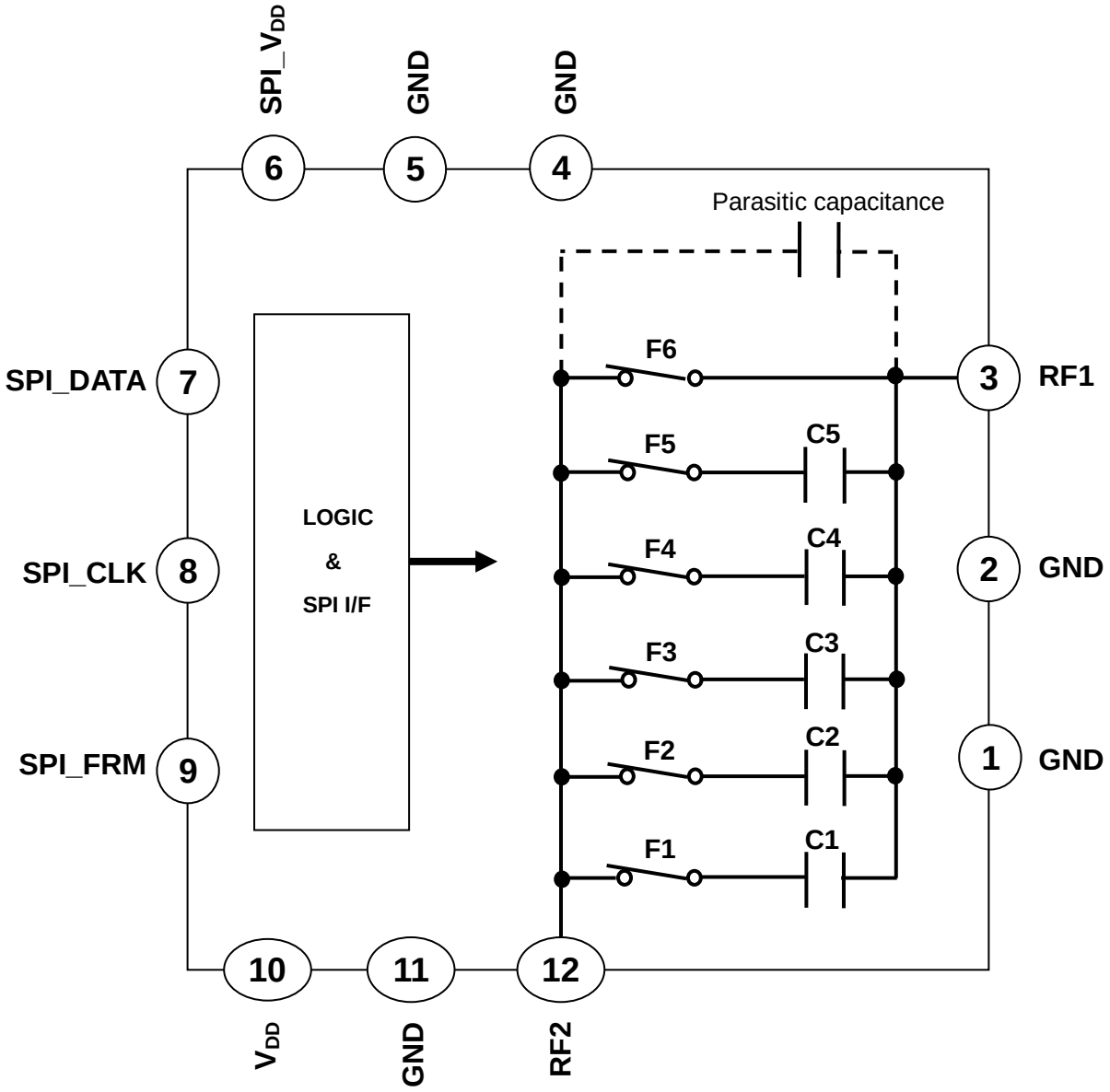
5 bits Capacitor Array: GaAs Junction Gate pHEMT (JPHEMT) MMIC
Driver: CMOS

This IC is ESD sensitive device. Special handling precautions are required.

E12825A2X

Block Diagram & Pin Configuration

UQFN-12P PKG (2.2 mm × 2.2 mm × 0.6 mm Max.)



Truth Table

Bit	Set	Function		Description
31	0	Write mode		Write to the Device
30	0	Address (Slave Type)		
29	0			
28	0			
27	0	Address (Slave Identifer)		
26	0			
25	0			
24	0			
23	0			
22	1/0	Address (Slave SPI register)		[22:18]=01000b
21	1/0			
20	1/0			
19	1/0			
18	1/0			
17	0	Not Used		
16	1/0	Standby*1		"1"=Active Mode, "0"=Standby Mode
15	1/0	Data	F1 selected	"1"=ON, "0"=OFF
14	1/0		F2 selected	"1"=ON, "0"=OFF
13	1/0		F3 selected	"1"=ON, "0"=OFF
12	1/0		F4 selected	"1"=ON, "0"=OFF
11	1/0		F5 selected	"1"=ON, "0"=OFF
10	1/0		F6 selected	"1"=ON, "0"=OFF(Through path)
9	0		Fixed	
8	0		Fixed	
7	0		Fixed	
6	0		Fixed	
5	0		Fixed	
4	0		Fixed	
3	0		Fixed	
2	0		Fixed	
1	0		Fixed	
0	0	Not Used		

*1 Standby

Standby bit is for low current operation in SSC disabled in mobile phone.
On Standby mode bias voltage for SSC part is shutoff.
Regardless of standby and active, IC can receive SPI data during supplying regular voltage to SPI_V_{DD}.

DC Bias Condition

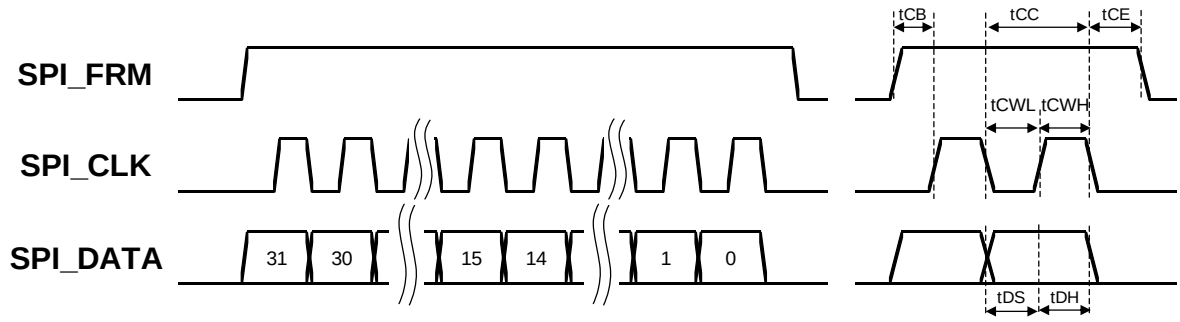
Ta = 25 ˚C

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{DD}	V_{DD}	2.40	2.80	3.30	V
SPI_V_{DD}(H)	SPI_V_{DD}	1.62	1.80	1.98	
SPI_CLK(H) SPI_DATA(H) SPI_FRM(H)	SPI_CLK SPI_DATA SPI_FRM	SPI_V_{DD} × 0.7	—	SPI_V_{DD} + 0.3	
SPI_CLK(L) SPI_DATA(L) SPI_FRM(L)		-0.3	—	SPI_V_{DD} × 0.2	

SPI Interface

Parameter	Specification
Address bits	16 bits
Data bits	16 bits
Total bits	32 bits
Clock rate	26 MHz max.
Clock edge (data sampling)	Rising edge

Definition of Timing



Absolute Maximum Ratings

Bias Voltage	V_{DD}	4	V	Ta = 25 ˚C
Control Voltage	SPI_V_{DD}, DATA, CLK, FRM	3.5	V	Ta = 25 ˚C
Maximum input power		+36	dBm	Duty cycle = 12.5 % to 50 %, Ta = 25 ˚C
Operating Temperature	Topr	−30 to +90	˚C	
Storage Temperature	Tstg	−65 to +150	˚C	

Electrical Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
SPI_Bias current	SPI_IDD	RF pins 50 Ω terminated. No RF power input. SPI_V_{DD} = 1.8 V	SPI_FRM = H, When signal is input.	140	—	300	μA
SPI_Enable	SPI_EN	Time from SPI_V_{DD}, turn on to SPI_FRM H_level		—	—	150	ns
Clock frequency	CLK_Freq	SPI_V_{DD} Enable		—	—	26	MHz
Clock cycle	tCC	CLK_Freq = 26 MHz		34	39	42	ns
Clock begin time	tCB			19.5	—	—	ns
Clock end time	tCE			9.5	—	—	ns
Clock width High	tCWH	tCC/2		17	—	21	ns
Clock width Low	tCWL	tCC/2		17	—	21	ns
Data setup time	tDS			14	—	—	ns
Data hold time	tDH			14	—	—	ns
Wake-up time	tWakeup	Wake-up time of inside DC-DC converter (V_{DD} On, release standby mode)		—	—	40	μs

Ta = 25 ˚C, V_{DD} = 2.8 V, SPI_V_{DD} = 1.8 V

Item	Symbol	Path	Condition		State	Min.	Typ.	Max.	Unit
DC Supply Current	IDD	—	Active mode, SPI:bit[16] = H		—	140	190	300	μA
			Standby mode, SPI:bit[16] = L		—	5	7	10	
	SPI_IDD	—	Active mode, SPI:bit[16] = H		—	1.5	4	16	
			Standby mode, SPI:bit[16] = L		—	1.5	4	16	
Transmission Performance	S21	RF1-RF2	Series connection	Freq. = 900 [MHz]	ALL OFF	-8.7	-7.3	-5.9	dB
					C1 ON	-6.8	-5.4	-4.0	
					C2 ON	-5.6	-4.3	-3.0	
					C3 ON	-4.1	-2.9	-1.9	
					C4 ON	-2.8	-1.6	-1.2	
					C5 ON	-1.4	-0.7	-0.4	
					ALL ON	-0.6	-0.3	-0.1	
				Freq. = 2000 [MHz]	ALL OFF	-4.4	-3.2	-2.0	
					C1 ON	-3.4	-2.2	-1.0	
					C2 ON	-2.9	-1.7	-0.7	
					C3 ON	-2.1	-1.1	-0.5	
					C4 ON	-1.2	-0.6	-0.4	
					C5 ON	-0.6	-0.4	-0.2	
					ALL ON	-0.5	-0.3	-0.1	
			Shunt connection	Freq. = 900 [MHz]	ALL OFF	-0.5	-0.3	-0.15	
					C1 ON	-0.7	-0.4	-0.2	
					C2 ON	-0.8	-0.5	-0.3	
					C3 ON	-1.6	-0.8	-0.6	
					C4 ON	-3.3	-1.6	-1.1	
					C5 ON	-5.7	-3.8	-2.2	
					ALL ON	-11.9	-9.9	-7.9	

Electrical Characteristics are measured with all RF ports terminated by 50 Ω.

Item	Symbol	Path	Condition	State	Min.	Typ.	Max.	Unit
Capacitance *1	Calloff	RF1	Calculated by S-parameter at 900 MHz.	0 (ALL OFF)	1.07	1.15	1.23	pF
	C1			1 (C1 ON)	1.32	1.42	1.52	
	C2			2 (C2 ON)	1.55	1.67	1.79	
				3	1.79	1.93	2.07	
	C3			4 (C3 ON)	2.00	2.15	2.30	
				5	2.23	2.40	2.57	
				6	2.45	2.64	2.83	
				7	2.68	2.88	3.08	
	C4			8 (C4 ON)	2.86	3.08	3.30	
				9	3.07	3.30	3.53	
				10	3.29	3.54	3.79	
				11	3.51	3.77	4.03	
				12	3.69	3.97	4.25	
				13	3.90	4.20	4.50	
				14	4.14	4.45	4.76	
				15	4.32	4.65	4.98	
	C5			16 (C5 ON)	4.51	4.85	5.19	
				17	4.68	5.04	5.40	
				18	4.87	5.24	5.61	
				19	5.05	5.43	5.81	
				20	5.23	5.63	6.03	
				21	5.41	5.82	6.23	
				22	5.59	6.01	6.43	
				23	5.75	6.19	6.63	
				24	5.95	6.40	6.85	
				25	6.13	6.59	7.05	
				26	6.30	6.78	7.26	
				27	6.45	6.94	7.43	
				28	6.62	7.12	7.62	
				29	6.79	7.30	7.81	
				30	6.96	7.48	8.00	
	Callon			31 (ALLON)	7.13	7.67	8.21	

Electrical Characteristics are measured with all RF ports terminated by 50 Ω.

*1: Capacitance calculation

$Z = R + jX$, $X = 1 / (\omega \cdot C) \Rightarrow \therefore C = 1 / (2\pi \cdot f \cdot X)$

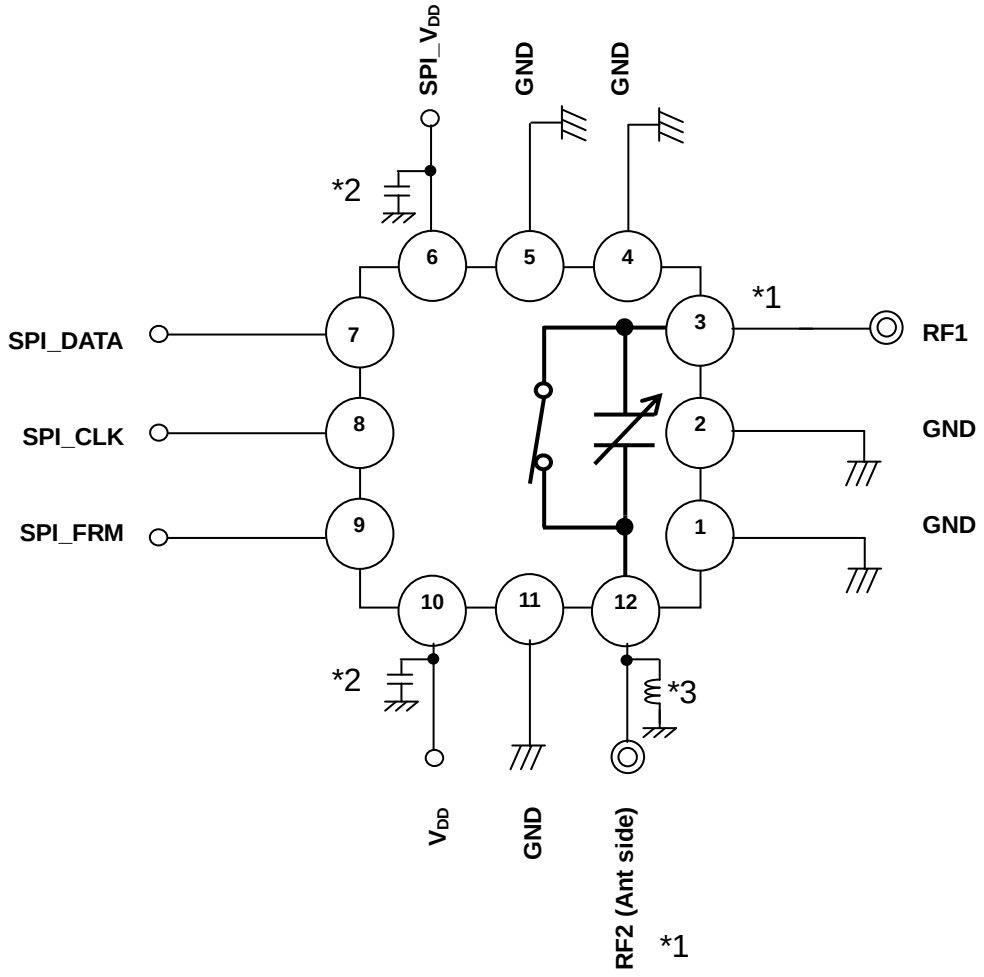
Item	Symbol	Path	Condition		State	Min.	Typ.	Max.	Unit
Harmonics	2fo	RF1-RF2	Series connection	Input Port : RF1 Freq. = 824 to 915 MHz Pin = 35 dBm 50 Ω LOAD	C1 ON	-75	-47	-40	dBm
					C2 ON	-75	-49	-40	
					C3 ON	-75	-50	-40	
					C4 ON	-75	-57	-40	
					C5 ON	-80	-70	-40	
					ALL ON	-75	-66	-40	
	3fo				C1 ON	-75	-54	-40	
					C2 ON	-75	-55	-40	
					C3 ON	-75	-58	-40	
					C4 ON	-75	-64	-40	
					C5 ON	-90	-78	-40	
					ALL ON	-90	-81	-40	
	2fo		Shunt connection		ALL OFF	-75	-50	-40	
					C1 ON	-75	-51	-40	
					C2 ON	-75	-52	-40	
					C3 ON	-75	-50	-40	
					C4 ON	-75	-53	-40	
					C5 ON	-75	-60	-40	
					ALL ON	-75	-65	-40	
	3fo				ALL OFF	-80	-72	-40	
					C1 ON	-80	-69	-40	
					C2 ON	-75	-67	-40	
					C3 ON	-75	-65	-40	
					C4 ON	-75	-65	-40	
					C5 ON	-85	-74	-40	
					ALL ON	-80	-69	-40	

Electrical Characteristics are measured with all RF ports terminated by 50 Ω.

Item	Symbol	Path	Condition		State	Min.	Typ.	Max.	Unit
Harmonics under Variable LOAD	2fo	RF1-RF2	Series connection	Input port : RF1 Freq. = 824 to 915 MHz Pin = 35 dBm VSWR = 5 ALL phase	C1 ON	—	—	-36	dBm
					C2 ON	—	—	-36	
					C3 ON	—	—	-36	
					C4 ON	—	—	-36	
					C5 ON	—	—	-36	
					ALL ON	—	—	-36	
	3fo				C1 ON	—	—	-36	
					C2 ON	—	—	-36	
					C3 ON	—	—	-36	
					C4 ON	—	—	-36	
					C5 ON	—	—	-36	
					ALL ON	—	—	-36	
	2fo	RF1-RF2	Shunt connection		ALL OFF	—	—	-36	
					C1 ON	—	—	-36	
					C2 ON	—	—	-36	
					C3 ON	—	—	-36	
					C4 ON	—	—	-36	
					C5 ON	—	—	-36	
					ALL ON	—	—	-36	
	3fo				ALL OFF	—	—	-36	
					C1 ON	—	—	-36	
					C2 ON	—	—	-36	
					C3 ON	—	—	-36	
					C4 ON	—	—	-36	
					C5 ON	—	—	-36	
					ALL ON	—	—	-36	
Switching Time	tSW	RF1-RF2	Time from falling edge of SPI_FRM to 100 % RF transient power Freq.= 824 to 915 MHz Pin = 35 dBm 50 Ω LOAD		—	8	9	11	µs

Recommended Circuit1

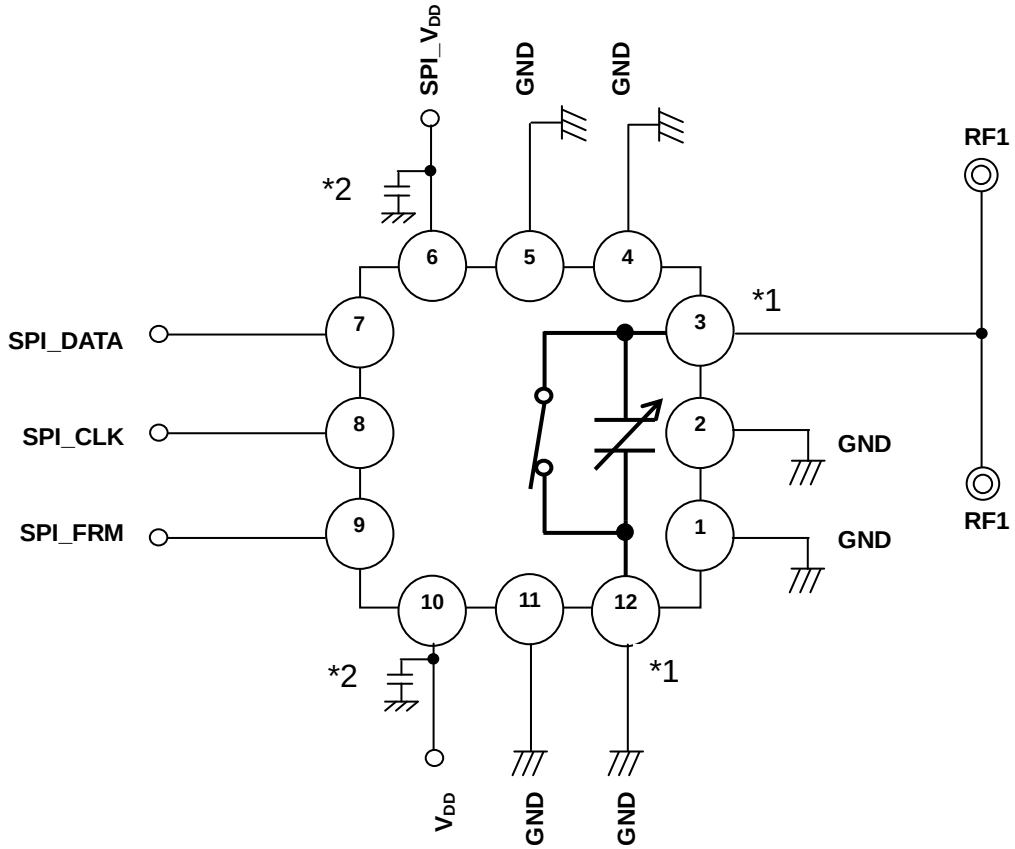
Series connection Case



*1: RF1 and RF2 connecting to signal line.
*2: Cbypass = 0.1 µF
*3: Inductor value depending on design. DC level of both RF1 and RF2 is GND.

Recommended Circuit2

Shunt connection Case

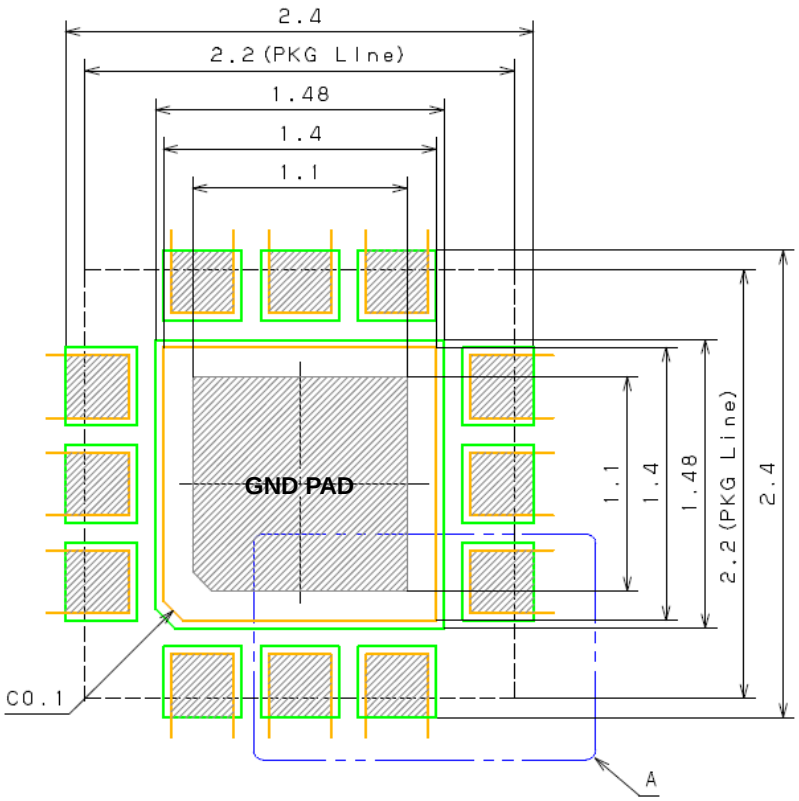


*1: RF1 port connecting to signal line, RF2 port connecting to gnd. DC level of RF1 is GND.
*2: Cbypass = 0.1 µF.

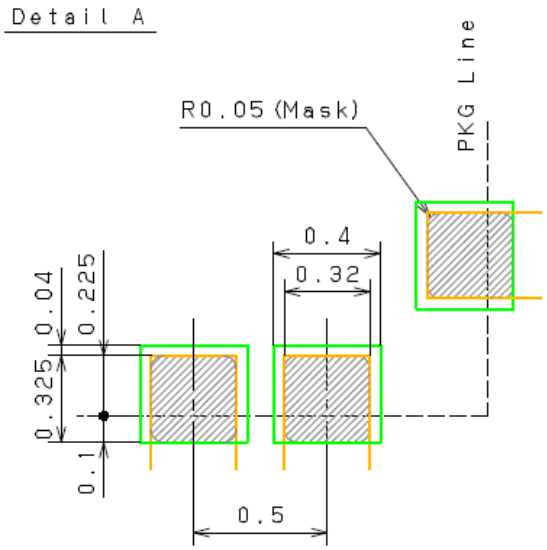
Recommended Land Pattern

(Unit : mm)

・PKG : 2.2mm×2.2mm
・Pin pitch : 0.5mm
＊Metal mask thickness : 110μm



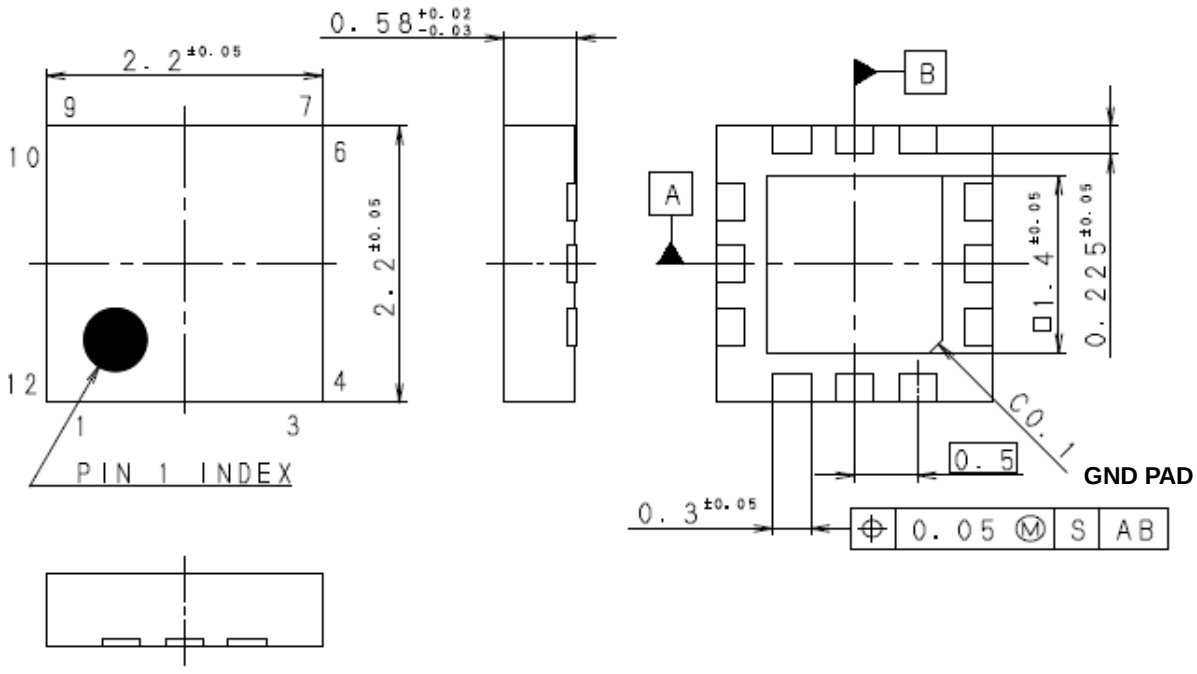
: Land
: Mask (Open area)
: Resist (Open area)

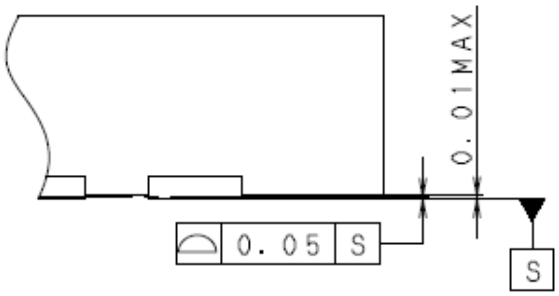


Package Outline

(Unit : mm)

12PIN UQFN (PLASTIC)





TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

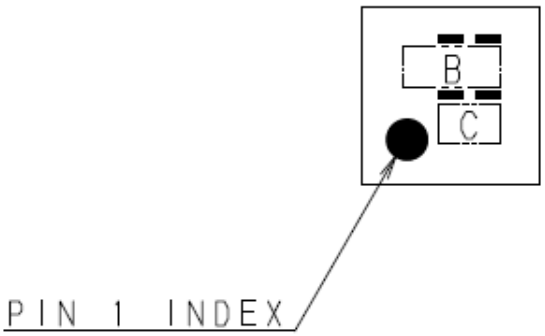
SONY CODE	UQFN-12P-391
JEITA CODE	P-UQFN12-2.2x2.2-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL
PACKAGE MASS	0.008g

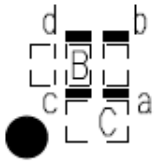
PART No. AP-2000-12QNAN1	Rev. 0
ISSUED 12.06.14	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:UR-12-FAN	

Marking



MARKING C: **GL**

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ２文字）を配置する。
（２文字を超える場合は製品名省略標示規定に従う。）



DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION d.
2) TYPE NO.(MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

Note

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