SONY

CXP5056/CXP5058

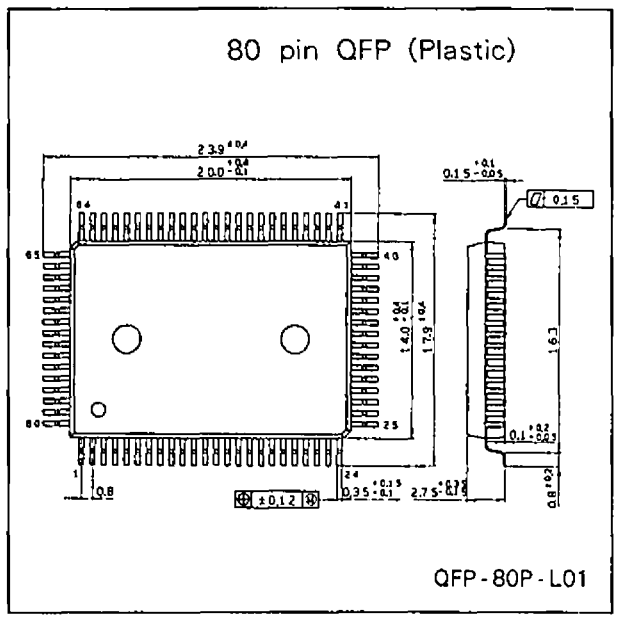
CMOS 4-bit 1 Chip Microcomputer

Description

CXP5056/CXP5058 is a CMOS 4-bit microcomputer which consists of 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interruption, power on reset function, fluorescent display tube controller/driver, D/A conversion PWM output port, a remote control reception circuit, 3-bit A/D converters, a 32kHz timer/event counter and a power supply current detection reset function. They are integrated into a single chip with the standby function, etc. which are to be operated at a low power consumption.

Package Outline

Unit : mm



Features

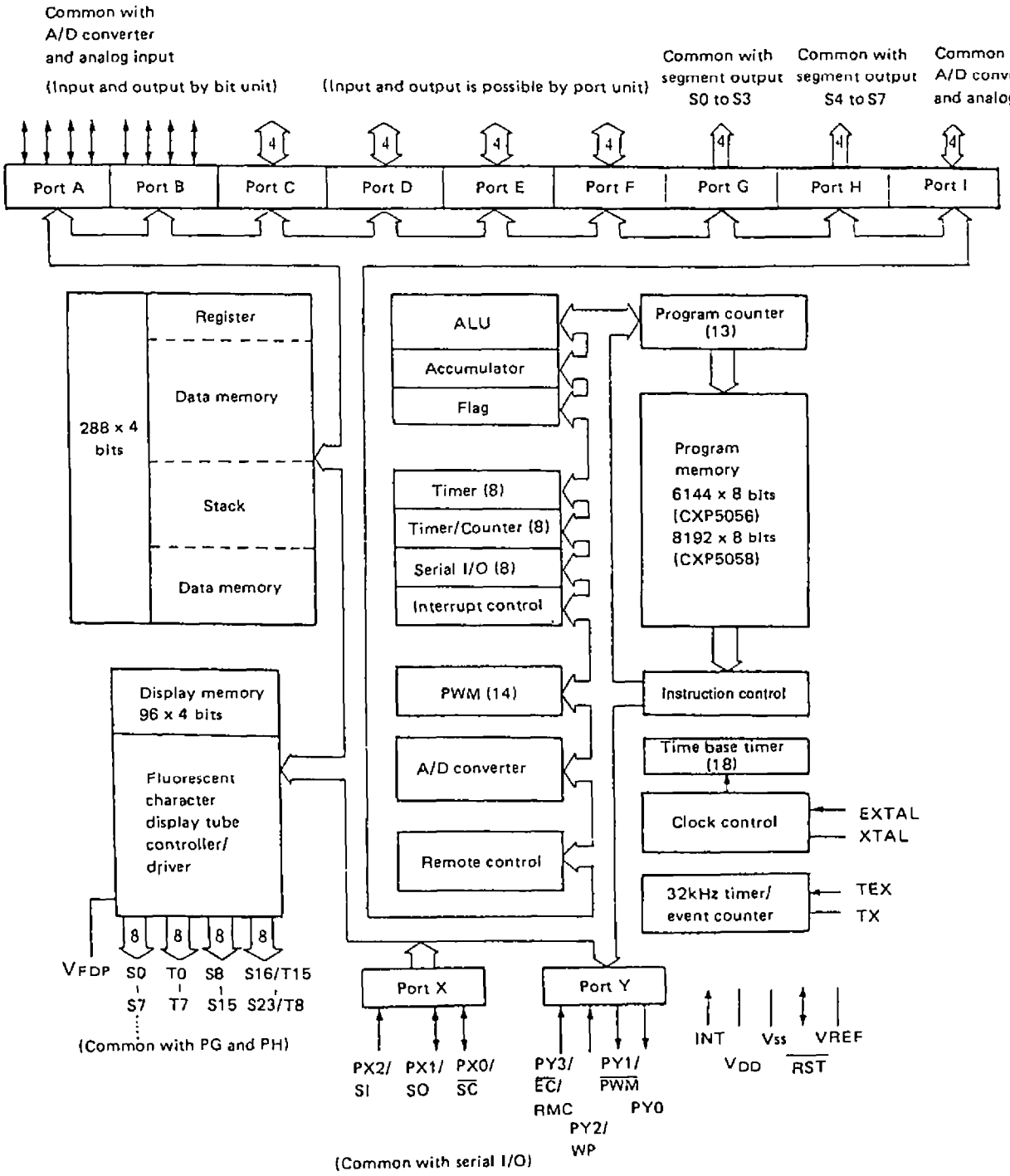
- Instruction cycle 3.8 µs/4.19MHz
  1.9 µs/4.19MHz
  (High speed version)
- ROM capacity 8,192 × 8 bits (CXP5058)
  6,144 × 8 bits (CXP5056)
- RAM capacity 384 × 4 bits (Including stack and display area)
- 43 general purpose I/O ports
- Fluorescent display tube controller/driver
  (Ables to display maximum 256 segments)
  - 1 to 16 digits dynamic scan display
  - Page mode/variable mode
  - Dimmer function
  - High tension proof output (40V)
  - Selection possible for incorporating pull-down resistance (mask option)
- 14-bit PWM output for D/A conversion
- Remote control receiving circuit
- 3-bit A/D converter (8 channels per circuit)
- 32kHz timer/event counter
- 8-bit/4-bit variable serial I/O
- 8-bit timer, 8-bit timer/event counter and 18-bit time base timer, independently controlled
- Arithmetic and logical operations possible between the entire RAM area, I/O area and the accumulator by means of memory mapped I/O
- Reference to the entire ROM area is possible with the table look-up instruction
- 2 kinds of power down modes of sleep and stop
- Power on reset circuit (mask option)
- Provided with 80 pin plastic QFP
- Provided with 80 pin piggyback QFP (CXP5050)

Structure

Silicon gate CMOS IC

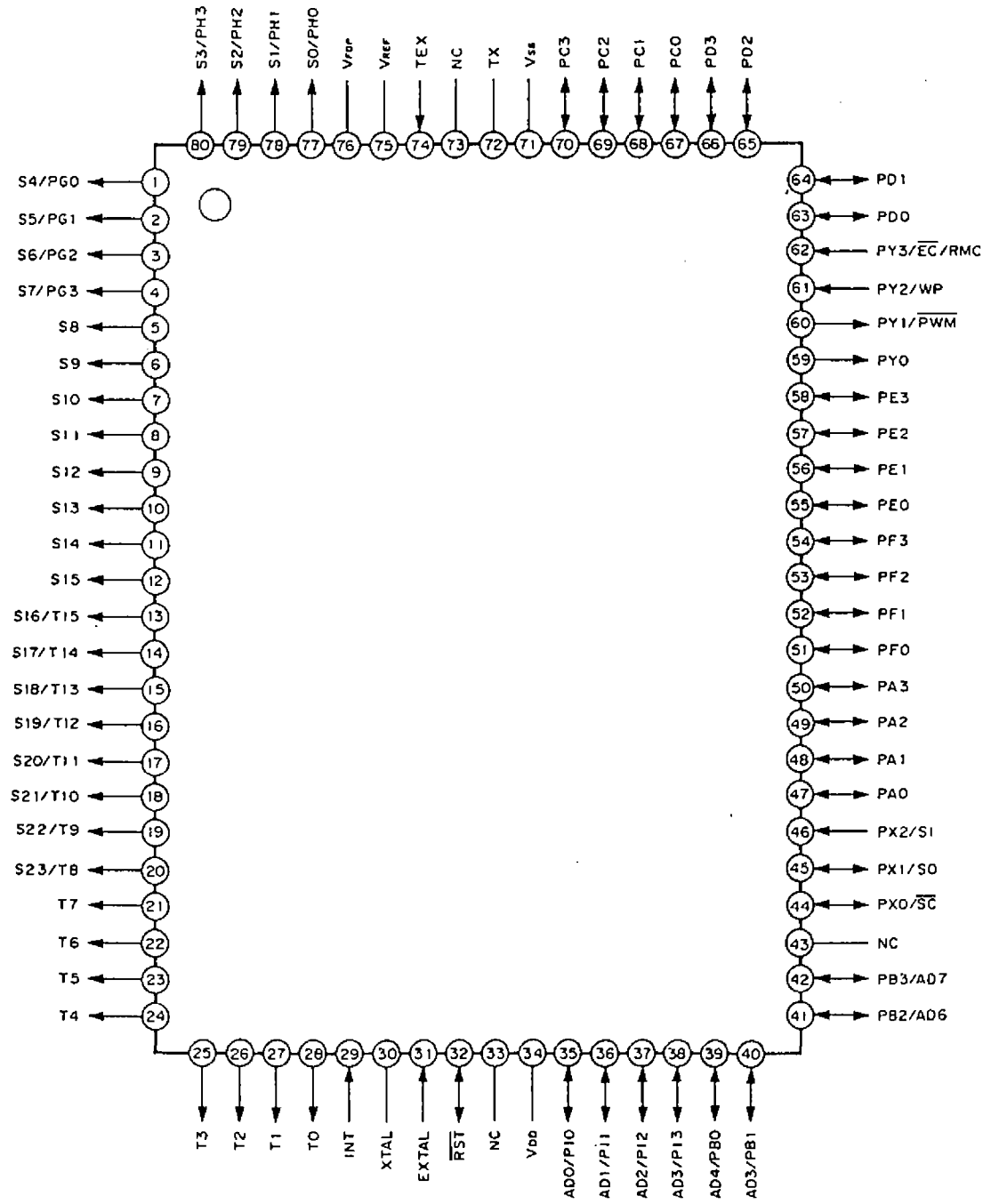
E89437 – ST

Block Diagram



Pin Configuration Diagram (Top View)

Note) Do not make any connections to NC pins.



Absolute Maximum Ratings Ta = − 20 °C to + 75 °C, V_{SS} = 0V

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	− 0.3 to + 7.0	V	
Input voltage	V_{IN}	− 0.3 to + 7.0*1	V	
Output voltage	V_{OUT}	− 0.3 to + 7.0*1	V	
Display output voltage	V_{OD}	V_{DD} − 40 to V_{DD} + 0.3	V	As P channel transistor is open drain, V_{DD} voltage is determined as standard.
High level output current	I_{OH}	− 5	mA	Other than display output pins*2 : per pin
	I_{ODH1}	− 15	mA	Display output S0 to S15 : per pin
	I_{ODH2}	− 35	mA	Display output T0 to T7, T8/S23 to T15/S16 : per pin
High level total output current	ΣI_{OH}	− 40	mA	Total of other than display output pins
	ΣI_{ODH}	− 100	mA	Total of display output pins
Low level output current	I_{OL}	15	mA	Port 1 pin
	I_{OLC}	20	mA	High current port pin*3
Low level total output current	ΣI_{OL}	100	mA	Entire pin total
Operating temperature	Topr	− 20 to + 75	°C	
Storage temperature	Tstg	− 55 to + 150	°C	
Allowable power dissipation	P_D	600	mW	QFP

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operation conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2) Specifies the output current of the general purpose I/O port PA to PF, PI, SO, $\overline{SC}$, PY0 and PY1.

*3) The high current operation transistors are the N-CH transistors of the PC and PD ports.

Recommended Operating Condition V_{SS} = 0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during operation
		2.5	5.5	V	Guaranteed data hold operation range during STOP
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*1
	V_{IHEX}	V_{DD}−0.4	V_{DD}+0.3	V	EXTAL pin*2
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*1
	V_{ILEX}	− 0.3	0.4	V	EXTAL pin*2
Operating temperature	Topr	− 20	+ 75	°C	

*1) The TEX pin when the counter mode is selected by each of INT, PX0, PX2, PY2, PY3, $\overline{RST}$ pins and mask option.

*2) Specified only during external clock input.

Electrical Characteristics

DC characteristics

Ta = − 20°C to + 75°C, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PF, PI PX0, PX1 PY0, PY1 $\overline{RST}$ (V_{OL} only)	V_{DD} = 4.5V, I_{OH} = − 0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = − 1.0mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC, PD	V_{DD} = 4.5V, I_{OL} = 12mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	− 0.5		− 40	µA
	I_{IHT}	TEX*3	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	− 0.1		− 10	µA
	I_{ILR}	$\overline{RST}$ *2		− 1.5		− 400	µA
High impedance I/O leakage current	I_{IZ}	PA to PF, PI PX0 to PX2, PY2, PY3, INT, $\overline{RST}$ *2, TEX*3	V_{DD} = 5.5V V_I = 0, 5.5V			± 10	µA
Display output current	I_{OH}	S0 to S15	V_{DD} = 4.5V V_{OH} = V_{DD} − 2.5V	− 7			mA
		S16/T15 to S23/T8, T0 to T7		− 18			mA
Open drain output leakage current (P-CH Tr OFF in state)	I_{LOL}	S0 to S15, S16/T15 to S23/T8, T0 to T7	V_{DD} = 5.5V V_{OL} = V_{DD} − 35V			− 20	µA
Pull-down resistance*1	R_L	S0 to S15, S16/T15 to S23/T8, T0 to T7	V_{DD} = 5V V_{FDP} = V_{DD} − 35V	60	100	270	kΩ
Supply current	I_{DD}	V_{DD}	Crystal oscillation (C1 = C2 = 22pF) of V_{DD} = 5.5V, 4.19MHz entire output pins open		5 (7)*4	15 (20)*4	mA
	I_{DDSP}		SLEEP mode		3 (5)*4	9 (12)*4	mA
	I_{DDS}		STOP mode V_{DD}=3V, 32kHz with T/C		30	200	µA
			V_{DD} = 5.5V, 32kHz without T/C (For mask option select counter, Pin is fixed.)			10	µA
Input capacity	C_{IN}	PA to PF, PI, PX, PY2, PY3, EXTAL, TEX, INT, $\overline{RST}$	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) In case the incorporated pull-down resistance has been selected with mask option.
*2) $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when nonresistance is selected.
*3) The TEX pin specifies the input current when the 32kHz oscillation is selected by the mask option, and specifies the leak current when the counter mode is specified.
*4) Specifies the power supply current of the high speed version.

AC Characteristics

(1) Clock timing

Ta = − 20°C to + 75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1	5	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	90		ns
System clock input rising and falling times	t_{CR} t_{CF}				200	ns
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{EC}$	Fig. 3	tsys*1 +0.05		µs
Event count clock input rising and falling times	t_{ER} t_{EF}	$\overline{EC}$	Fig. 3		20	ms
Event count input clock input pulse width	t_{TL} t_{TH}	TEX*2	Fig. 3	10		µs
Event count input clock rising and falling times	t_{TR} t_{TF}	TEX*2	Fig. 3		20	ms

*1) tsys in the standard version is tsys = 16/fc
tsys in the high speed version is tsys = 8/fc
*2) Specified when the counter mode is selected by the mask option.
Note) When adjusting the frequency accurately, there may be cases in which they may differ from Fig. 2.

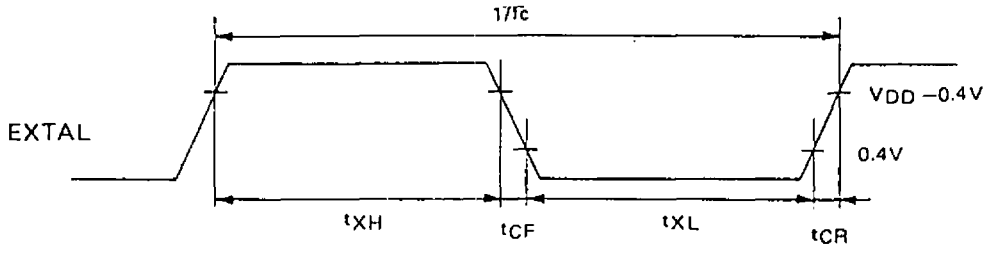


Fig. 1 Clock timing

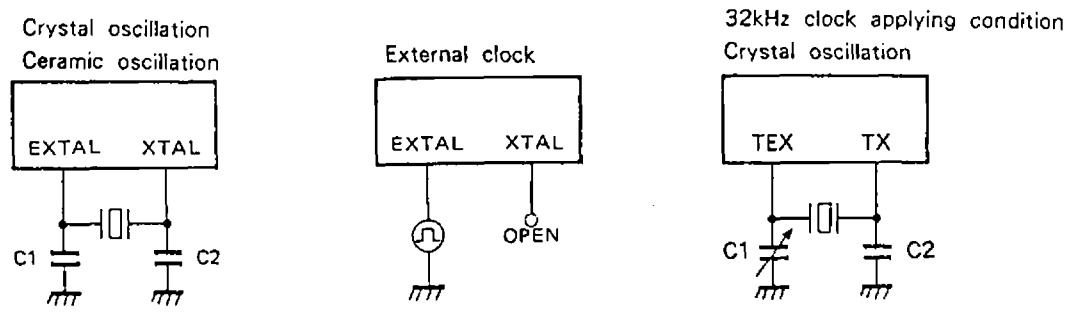


Fig. 2 Clock applying condition

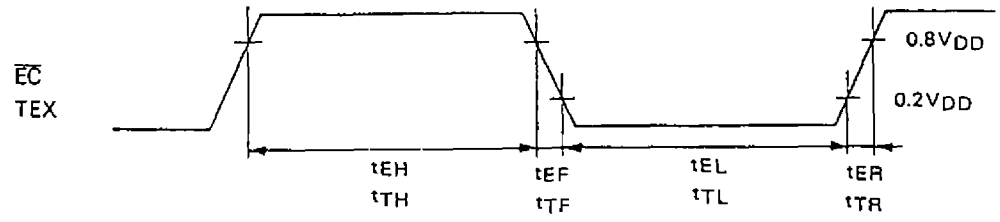


Fig. 3 Event count clock timing

(2) Serial transfer Ta = −20°C to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock ($\overline{SC}$) cycle time	t_{KCY}	$\overline{SC}$	Input mode	tsys/4 +1.42		µs
			Output mode	2tsys		µs
Serial transfer clock ($\overline{SC}$) high and low level widths	t_{KH} t_{KL}	$\overline{SC}$	Input mode	tsys/8 +0.7		µs
			Output mode	tsys − 0.1		µs
Serial data input setup time (against $\overline{SC}$ ↑)	t_{SIK}	SI	$\overline{SC}$ input mode	0.1		µs
			$\overline{SC}$ output mode	0.2		µs
Serial data input hold time (against $\overline{SC}$ ↑)	t_{KSI}	SI	$\overline{SC}$ input mode	tsys/8 +0.5		µs
			$\overline{SC}$ output mode	0.1		µs
Data delay time from $\overline{SC}$ falling	t_{KSO}	SO			tsys/8 +0.5	µs

Note 1) tsys in the standard version is tsys = 16/fc
tsys in the high speed version is tsys = 8/fc
2) The Load of data output delay is 50pF + 1TTL

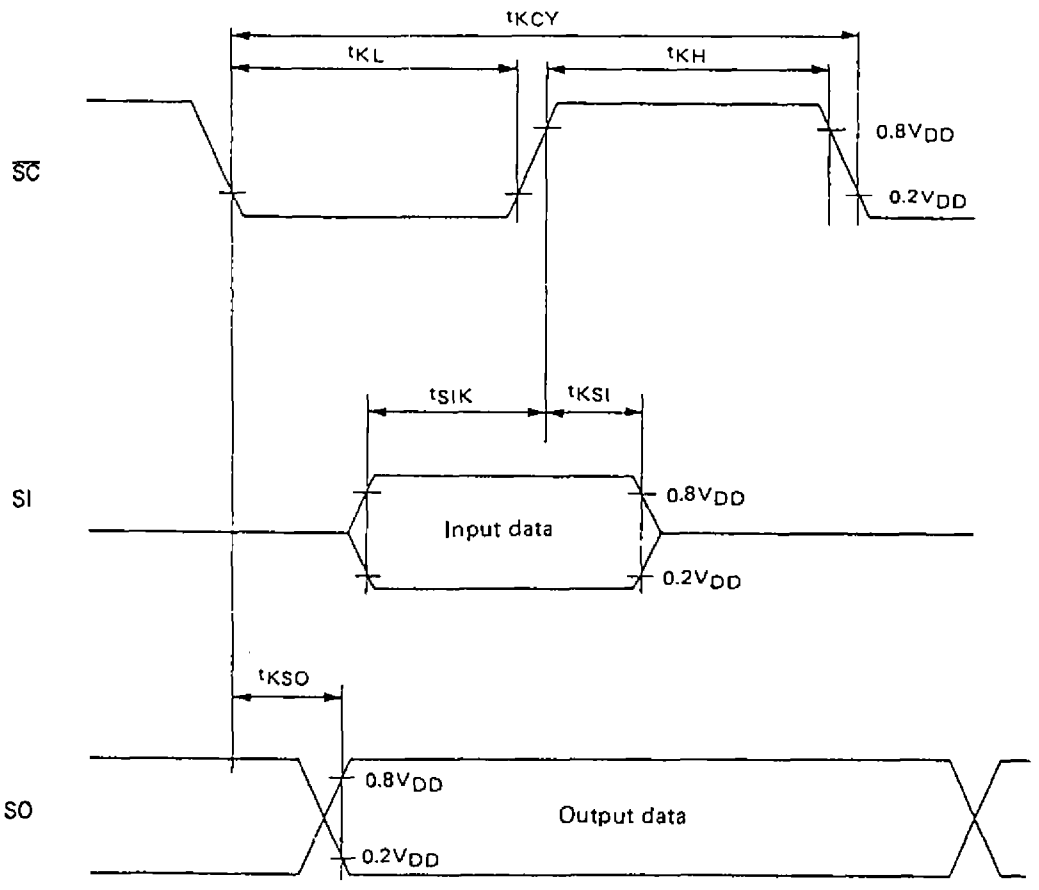


Fig. 4 Serial transfer timing

(3) A/D converter Ta = − 20°C to + 75°C, V_{SS} = 0V

Analog input voltage	Pin	Condition	Digital conversion value
0.0 to 0.33V	AD0 to AD7	V_{DD} = 5V	000
0.82 to 1.29V			001
1.78 to 2.21V			010
2.69 to 3.06V			011
3.56 to 4.06V			100
4.62 to 5.0V			101

Note) The digital conversion value are the values when $B5_H$ address of the RAM file 1 in the program are read.

(4) Power Supply Voltage Detection Reset Function Ta = − 20 °C to + 75 °C, Vss = 0V

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply voltage detection reset function of operation voltage range	V_{LPOP}	V_{DD}	Voltage range allowing system operation	2.5		5.5	V
Power supply voltage drop detection function	V_{POP}	V_{DD}	When V_{REF} pin voltage is 3.3V Flag set when voltage drops System reset when voltage rises	3.8	4.0	4.2	V

The graph in Fig. 5 shows the relationship between the power supply voltage V_{DD} and reference voltage V_{REF} of the power supply voltage detection reset function.

Note 1) The graph in Fig. 5 serves as guide to the function operation area obtained using average devices.
Individual adjustment is needed when Zener diodes, etc., are connected to the V_{REF} pin.

2) At the rising edge of the power supply, the reset function is activated below 4.5V.
As there is no oscillation stabilization time for resets by the power supply voltage reset function, it is necessary that the voltage of the power supply rises to above 4.5V immediately (approx. 30 µs). Ample consideration is required for the oscillation stabilization time as it varies according to the oscillation element.
(In general, time required for stabilization from the beginning of oscillation is shorter for ceramic oscillators than for crystal oscillators.)

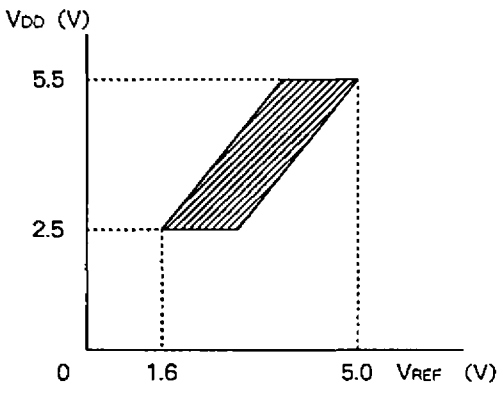


Fig. 5 Power supply voltage detection reset function chart

(5) Others Ta = − 20 °C to + 75 °C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{I1H}, t_{I1L}	INT	During edge detection mode	tsys + 0.05		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		2tsys		µs
Wake-up input high level width	t_{WPH}	WP	STOP mode	500		ns
			SLEEP mode	tsys + 0.05		µs

Note) tsys in the standard version is tsys = 16/fc
tsys in the high speed version is tsys = 8/fc

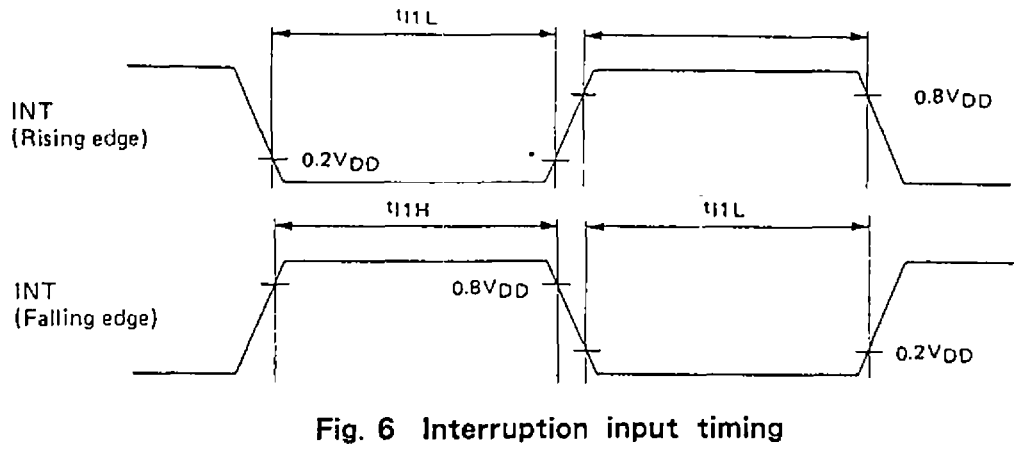


Fig. 6 Interruption input timing

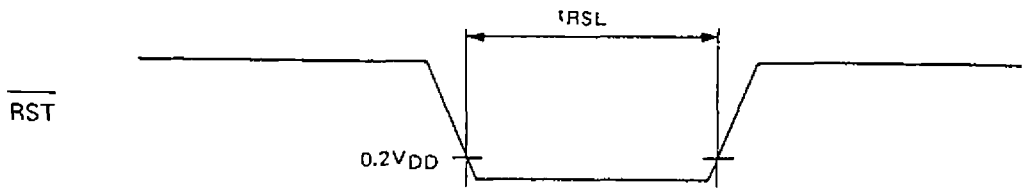


Fig. 7 Reset input timing

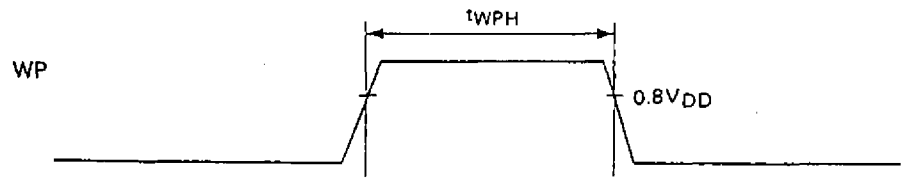
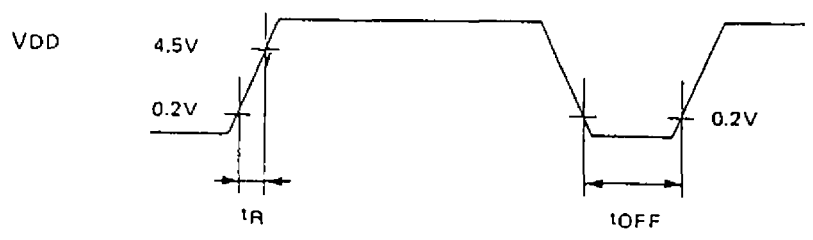


Fig. 8 Wake-up input timing

Power on reset * Ta = − 20 °C to + 75 °C, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.



The power supply should rise smoothly.

Fig. 9 Power on reset

Notes on Application

See Fig. 10, Additive capacity calculation chart, when using the crystal oscillator and select the appropriate capacity.

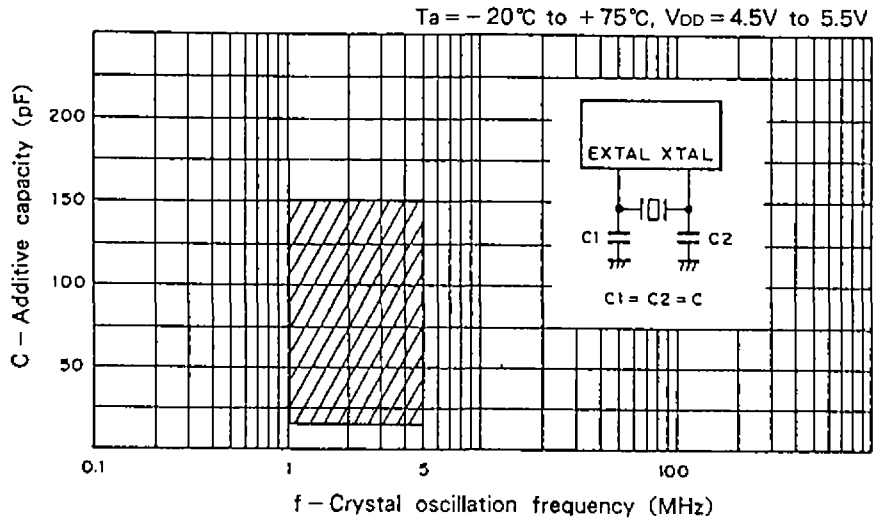


Fig. 10 Crystal oscillation circuit additive capacity calculation chart

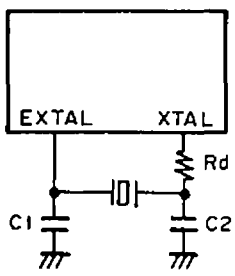
Note) The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

Fig. 11 shows recommended circuits and oscillators.

Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

1. Main clock

4.19MHz



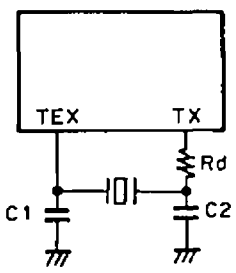
Ceramic resonator

Manufacturer	Model	Frequency range(MHz)	C1(pF)	C2(pF)	Rd(Ω)
MURATA MFG CO., LTD.	CSA4.19MG040	4.19	100	100	—
	CSA4.19MGW040		built in	built in	—

Crystal oscillator

Manufacturer	Model	Frequency range(MHz)	C1(pF)	C2(pF)	Rd(Ω)
CITIZEN WATCH CO., LTD.	CSA309	4.19	10 (20 trimmer)	10	—
NIHON DEMPA KOGYO CO., LTD.	AT-51		15 (20 trimmer)	15	6.8k
KINSEKI LTD.	HC-49/U-S		22 (20 trimmer)	22	3.3k

2. 32kHz Timer/Counter



Manufacturer	Model	Frequency range(kHz)	C1(pF)	C2(pF)	Rd(Ω)
CITIZEN WATCH CO., LTD.	CFS-308	32.768	18 (20 trimmer)	18	—
NIHON DEMPA KOGYO CO., LTD.	MX-38T		22 (20 trimmer)	22	470k
KINSEKI LTD.	P3		22 (20 trimmer)	22	3.3k

About the details of oscillators, please inquire the makers or the agencies.

Fig. 11 Recommended oscillation circuit

When using the A/D converter as the key input, it is recommended that the circuit structure shown in Fig. 12 be used.

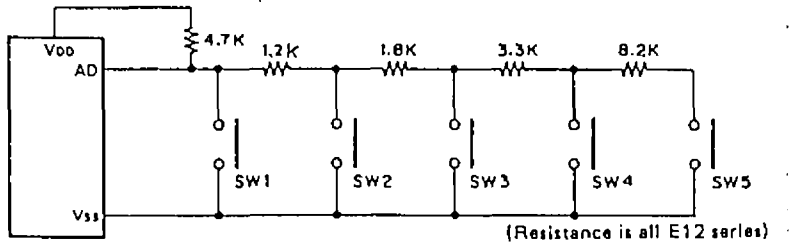


Fig. 12 Recommended example of key circuit by A/D converter