200-MHz Differential Clock Buffer/Driver

Features

- **Up to 200 MHz operation**
- **Phase-locked loop clock distribution for Double Data Rate Synchronous DRAM applications**
- **Distributes one clock input to ten differential outputs**
- **External feedback pin (FBIN) is used to synchronize the outputs to the clock input**
- **Conforms to the DDR1 specification**
- **Spread Aware™ for EMI reduction**
- **48-pin SSOP package**

Description

This PLL clock buffer is designed for 2.5-VDD and 2.5-AVDD operation and differential outputs levels.

This device is a zero delay buffer that distributes a clock input (CLKIN) to ten differential pairs of clock outputs (YT[0:9], YC[0:9]) and one feedback clock output (FBOUT). The clock outputs are individually controlled by the serial inputs SCLK and SDATA.

The two line serial bus can set each output clock pair (YT[0:9], YC[0:9]) to the Hi-Z state. When AVDD is grounded, the PLL is turned off and bypassed for the test purposes.

The PLL in this device uses the input clock (CLKIN) and the feedback clock (FBIN) to provide high-performance, low-skew, low-jitter output differential clocks.

Block Diagram

Pin Configuration
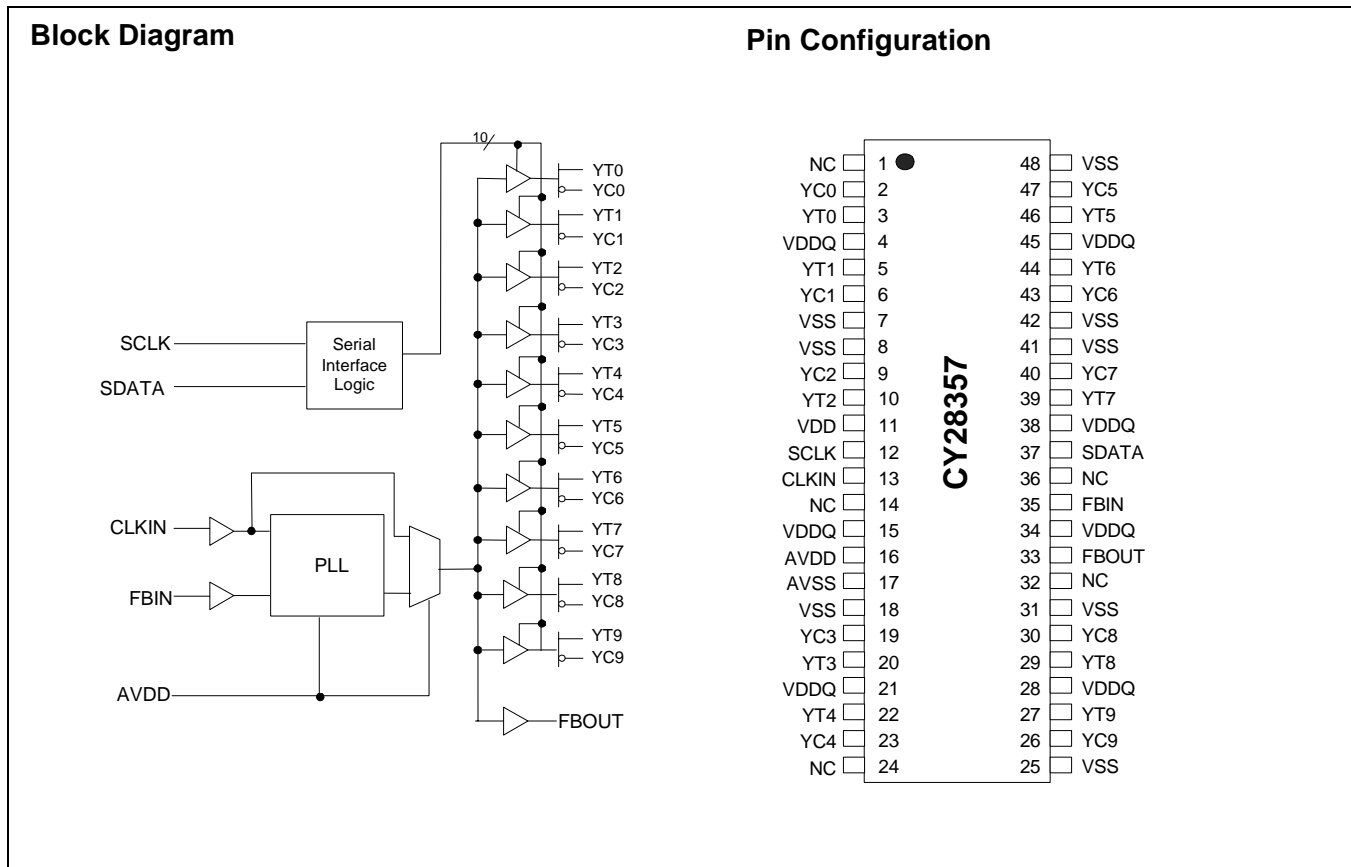
Pin Description[1]

Pin	Name	I/O	Description	Electrical Characteristics
13	CLKIN	I	Clock Input.	Input
35	FBIN	I	**Feedback Clock Input**. Connect to FBOUT for accessing the PLL.	Input
3, 5, 10, 20, 22 46, 44, 39, 29,27	YT(0:9)	O	Clock Outputs	Differential Outputs
2, 6, 9, 19, 23 47, 43, 40,30,26	YC(0:9)	O	Clock Outputs	
33	FBOUT	O	**Feedback Clock Output**. Connect to FBIN for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.	Output
12	SCLK	I	**Serial Clock Input**. Clocks data at SDATA into the internal register.	Data Input for the two line serial bus
37	SDATA	I/O	**Serial Data Input**. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.	Data Input and Output for the two line serial bus
11	VDD		2.5V Power Supply for Logic	2.5V Nominal
4, 15, 21, 28, 34, 38, 45	VDDQ		2.5V Power Supply for Output Clock Buffers.	2.5V Nominal
16	AVDD		2.5V Power Supply for PLL	2.5V Nominal
1, 24	NC		No Connect	
7, 8, 18, 25, 31, 41, 42, 48	VSS		Common Ground	0.0V Ground
17	AVSS		Analog Ground	0.0V Analog Ground
14,32,36	NC		Not Connected	

Note:

1. A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Function Table

Input		Outputs			PLL
VDDA	**CLKIN**	**YT(0:9)**[2]	**YC(0:9)**[2]	**FBOUT**	
GND	L	L	H	L	BYPASSED/OFF
GND	H	H	L	H	BYPASSED/OFF
2.5V	L	L	H	L	On
2.5V	H	H	L	H	On
2.5V	< 20 MHz	Hi-Z	Hi-Z	Hi-Z	Off

Zero Delay Buffer

When used as a zero delay buffer the CY28357 will likely be in a nested clock tree application. For these applications the CY28357 offers a clock input as a PLL reference. The CY28357 then can lock onto the reference and translate with near zero delay to low-skew outputs. For normal operation, the external feedback input, FBIN, is connected to the feedback output, FBOUT. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

Note:
2. Each output pair can be three-stated via the two line serial interface

When VDDA is strapped LOW, the PLL is turned off and by-passed for test purposes.

Power Management

The individual output enable/disable control of the CY28357 allows the user to implement unique power management schemes into the design. Outputs are three-stated when disabled through the two-line interface as individual bits are set low in Byte0 and Byte1 registers. The feedback output (FBOUT) cannot be disabled via two line serial bus. The enabling and disabling of individual outputs is done in such a manner as to eliminate the possibility of partial "runt" clocks.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 1*. The slave receiver address is 11010010 (D2h).

Table 1. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	....	39:46	Data byte from slave – 8 bits
....	Data Byte (N–1) – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Data Byte N – 8 bits	56	Acknowledge
....	Acknowledge from slave	....	Data bytes from slave/Acknowledge
....	Stop	....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

Byte0: Output Register 1 (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	1	3, 2	YT0, YC0
6	1	5, 6	YT1, YC1
5	1	10, 9	YT2, YC2
4	1	20, 19	YT3, YC3
3	1	22, 23	YT4, YC4
2	1	46, 47	YT5, YC5
1	1	44, 43	YT6, YC6
0	1	39, 40	YT7, YC7

Byte1 Output Register 2 (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	1	29, 30	YT8, YC8
6	1	27, 26	YT9, YC9
5	0		Reserved
4	0		Reserved
3	0		Reserved
2	0		Reserved
1	0		Reserved
0	0		Reserved

Byte2 Test Register 3

Bit	@Pup	Pin#	Description
7	1		Reserved
6	1		Reserved
5	1		Reserved
4	1		Reserved
3	1		Reserved
2	1		Reserved
1	1		Reserved
0	1		Reserved

Parameter Measurement Information
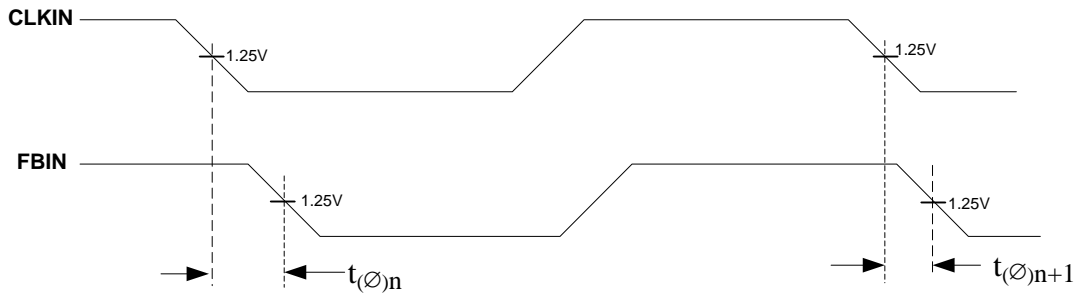
$$t_{(\varnothing)n} = \frac{\sum_1^{n=N} t_{(\varnothing)n}}{} \quad \text{(N is large number of samples)}$$

Figure 1. Static Phase Offset
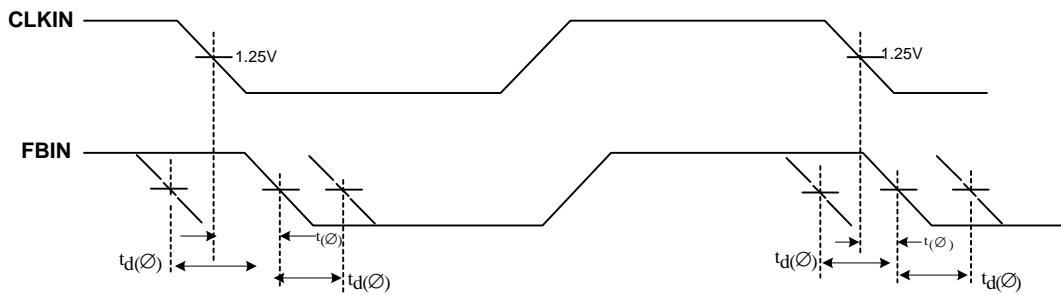
Figure 2. Dynamic Phase Offset

Figure 3. Output Skew

YT[0:9], FBOUT

YC[0:9]

$$t_{c(n)}$$

YT[0:9], FBOUT

YC[0:9]

$$\frac{1}{f(o)}$$

$$t_{jit(hper)} = t_{c(n)} - \frac{1}{fo}$$

Figure 4. Period Jitter

YT[0:9], FBOUT

YC[0:9]

$$t_{(hper\_n)}$$

$$t_{(hper\_N+1)}$$

$$\frac{1}{f(o)}$$

$$t_{jit(hper)} = t_{hper(n)} - \frac{1}{2x \, fo}$$
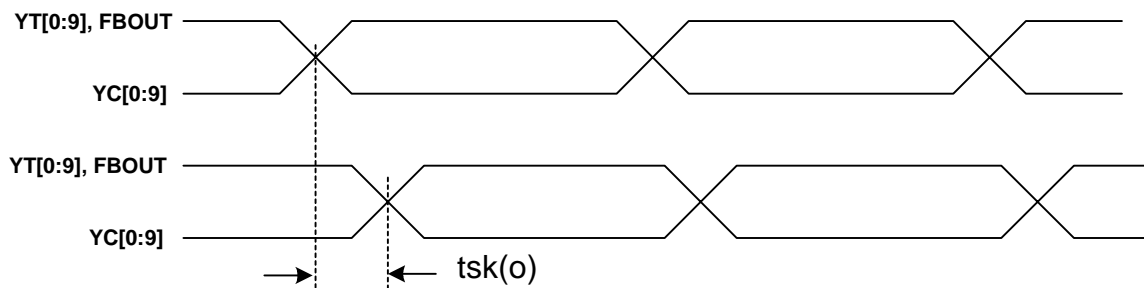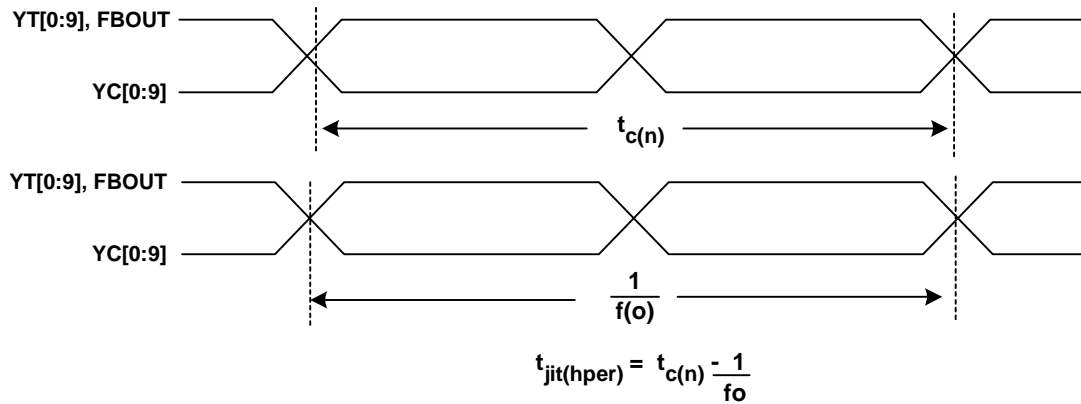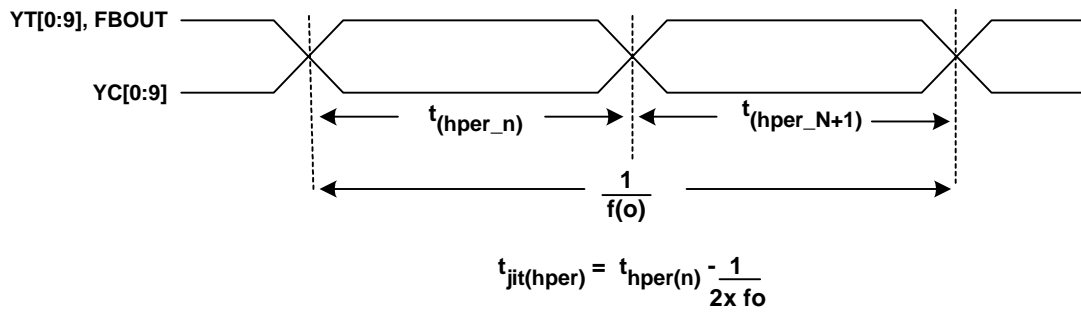
Figure 5. Half-Period Jitter

CLKT[0:5], FBOUT

CLKC[0:5]

$$t_{c(n)}$$

$$t_{c(n)}$$

$$t_{jit(cc)} = t_{c(n)} - t_{c(n+1)}$$
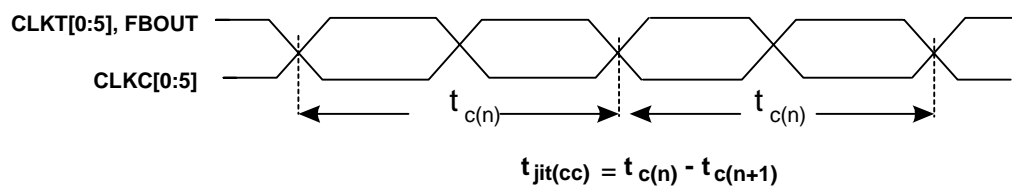
Figure 6. Cycle-to-cycle Jitter

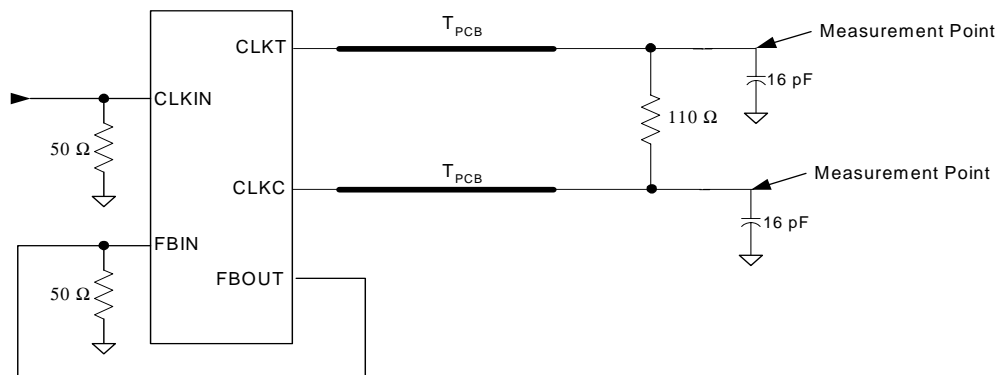**Figure 7. Differential Signal Using Direct Termination Resistor**

Maximum Ratings[3]

Input Voltage Relative to V_{SS}:...............................V_{SS} – 0.3V

Input Voltage Relative to V_{DDQ} or AV_{DD}: ....V_{DD} + 0.3V

Storage Temperature: ....–65°C to + 150°C

Operating Temperature:...................................0°C to +85°C

Maximum Power Supply: 3.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters[4] (V_{DD} = V_{DDA} = V_{DDQ} = V_{DDI} = 2.5V ± 5%, T_A = 0°C to +70°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	SDATA, SCLK			1.0	V
V_{IH}	Input High Voltage	SDATA, SCLK	2.2			V
V_{IL}	Input Voltage Low	CLKIN, FBIN			0.4	V
V_{IH}	Input Voltage High	CLKIN, FBIN	2.1			V
I_{IN}	Input Current	V_{IN} = 0V or V_{IN} = V_{DDQ}, CLKT, FBIN	–10		10	μA
I_{OL}	Output Low Current	V_{DDQ} = 2.375V, V_{OUT} = 1.2V	26	35		mA
I_{OH}	Output High Current	V_{DDQ} = 2.375V, V_{OUT} = 1V	–18	-32		mA
V_{OL}	Output Low Voltage	V_{DDQ} = 2.375V, I_{OL} = 12 mA			0.6	V
V_{OH}	Output High Voltage	V_{DDQ} = 2.375V, I_{OH} = –12 mA	1.7			V
V_{OUT}	Output Voltage Swing[5]		1.1		V_{DDQ}–0.4	V
V_{OC}	Output Crossing Voltage[6]		(V_{DDQ}/2) – 0.2	V_{DDQ}/2	(V_{DDQ}/2) + 0.2	V
I_{OZ}	High-Impedance Output Current	V_O = G_{ND} or V_O=V_{DDQ}	–10		10	μA
I_{DDQ}	Dynamic Supply Current[7]	All V_{DDQ} and V_{DDI}, F_O = 200 MHz		235	300	mA
I_{DSTAT}	Static Supply Current				1	mA
I_{DD}	PLL Supply Current	V_{DDA} only		9	12	mA
C_{IN}	Input Pin Capacitance			4	6	pF

Notes:
3. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply srquencing is NOT required.
4. unused inputs must be held high or low to prevent them from floating.
5. For load conditions see *Figure 7*.
6. The value of V_{OC} is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120Ω resistor. See *Figure 7*.
7. All outputs switching loaded with 16 pF in 60Ω environment. See *Figure 7*.

**AC Parameters**[8,9] (V_{DD} = V_{DDQ} = 2.5V ±5%, TA = 0°C to + 70°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{CLK}	Operating Clock Frequency		60		200	MHz
t_{DC}	Input Clock Duty Cycle		40		60	%
t_{LOCK}	Maximum PLL lock Time				100	µs
t_R/t_F	Output Clocks Slew Rate	20% to 80% of V_{OD}	1		2.5	V/ns
t_{CCJ}	Cycle to Cycle Jitter[11]	f > 66 MHz	−100		100	ps
tjit(h-per)	Half-period jitter[11]	f > 66 MHz	−100		100	ps
t_{PLH}	Low-to-High Propagation Delay, CLKIN to YT		1.5	3.5	6	ns
t_{PHL}	High-to-Low Propagation Delay, CLKIN to YT		1.5	3.5	6	ns
t_{SKEW}	Any Output to Any Output Skew[10]				100	ps
t_{PHASE}	Phase Error[10]		−150		150	ps
t_{PHASEJ}	Phase Error Jitter	f > 66 MHz	−50		50	ps

Notes:
8. Parameters are guaranteed by design and characterization. Not 100% tested in production.
9. PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30 kHz and 33.3 kHz with a down spread of −0.5%.
10. All differential input and output terminals are terminated with 120Ω/16 pF as shown in *Figure 7*.
11. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.

Ordering Information

Part Number	Package Type	Product Flow
CY28357OC	48-pin SSOP	Commercial, 0° to 70°C
CY28357OCT	48-pin SSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

48-Lead Shrunk Small Outline Package O48

51-85061-*C
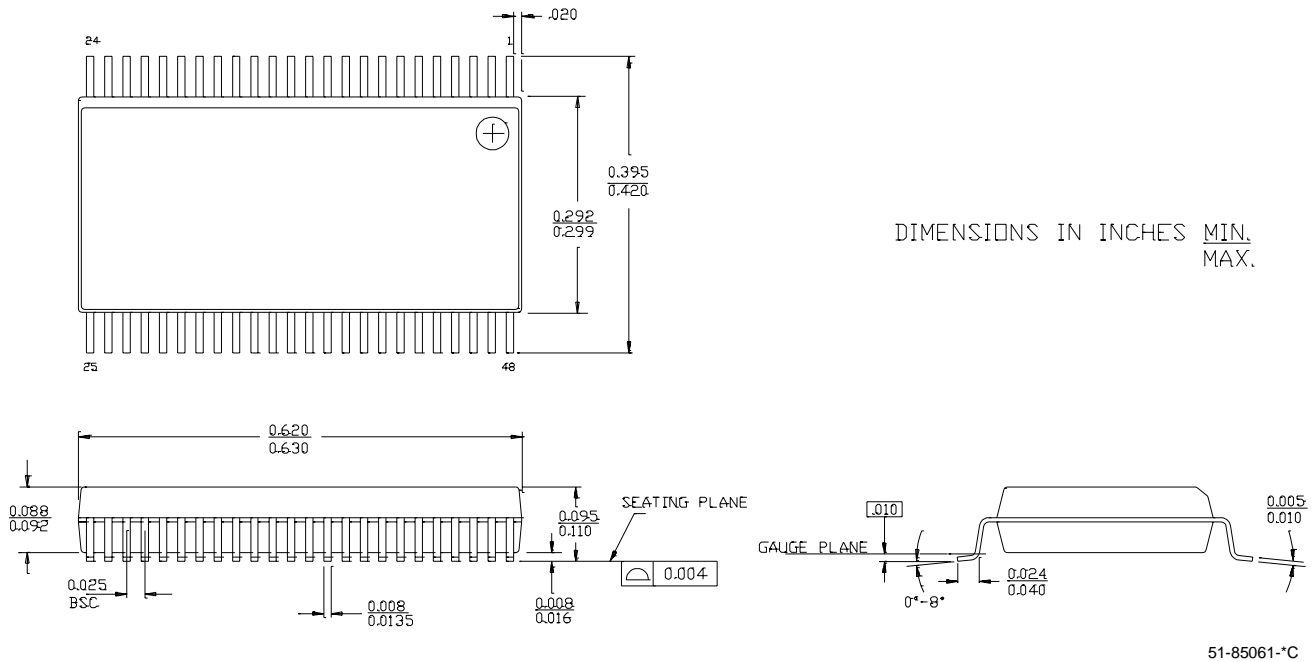
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Document History Page

Document Title: CY28357 200-MHz Differential Clock Buffer/Driver Document #: 38-07416				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	118003	09/11/02	RGL	New Data Sheet
*A	122924	12/27/02	RBI	Add power up requirements to maximum ratings information.