

3.3 V 125 MHz Multi-Output Zero Delay Buffer

Features

- Output Frequency up to 125 MHz
- 12 Clock Outputs: Frequency Configurable
- 350 ps max. Output to Output Skew
- Configurable Output Disable
- Two Reference Clock Inputs for Dynamic Toggling
- Oscillator or PECL Reference Input
- Spread Spectrum Compatible
- Glitch-free Output Clocks Transitioning
- 3.3 V Power Supply
- Pin Compatible with MPC973
- Industrial Temperature Range: -40 °C to +85 °C
- 52-pin TQFP Package

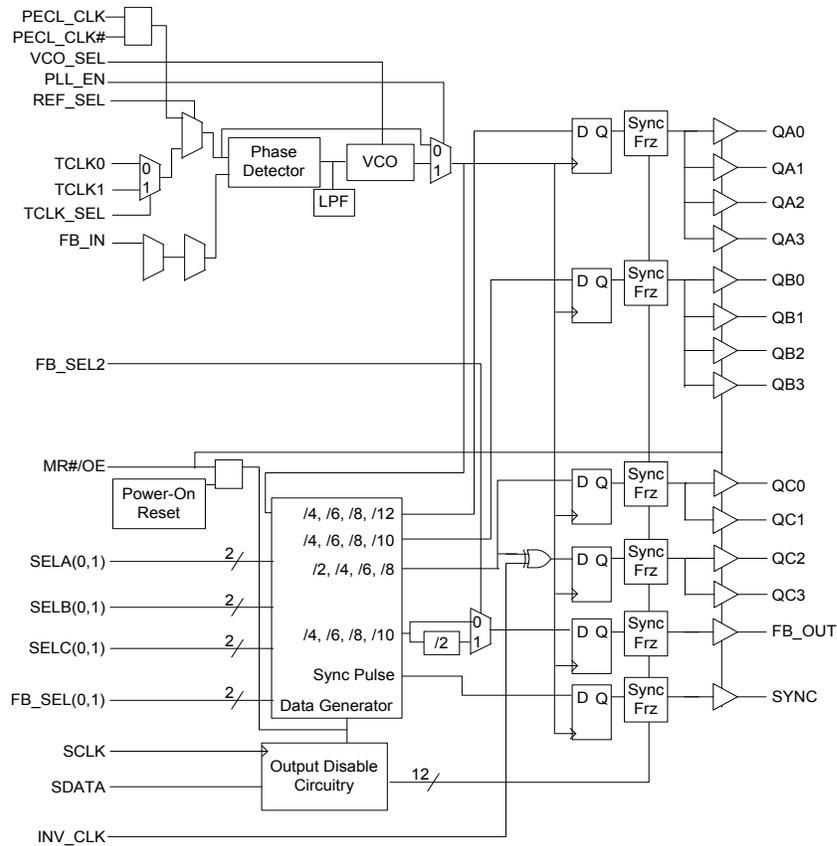
Table 1. Frequency Table^[1]

| VC0_SEL | FB_SEL2 | FB_SEL1 | FB_SEL0 | F _{VC0} |
|---------|---------|---------|---------|------------------|
| 0 | 0 | 0 | 0 | 8x |
| 0 | 0 | 0 | 1 | 12x |
| 0 | 0 | 1 | 0 | 16x |
| 0 | 0 | 1 | 1 | 20x |
| 0 | 1 | 0 | 0 | 16x |
| 0 | 1 | 0 | 1 | 24x |
| 0 | 1 | 1 | 0 | 32x |
| 0 | 1 | 1 | 1 | 40x |
| 1 | 0 | 0 | 0 | 4x |
| 1 | 0 | 0 | 1 | 6x |
| 1 | 0 | 1 | 0 | 8x |
| 1 | 0 | 1 | 1 | 10x |
| 1 | 1 | 0 | 0 | 8x |
| 1 | 1 | 0 | 1 | 12x |
| 1 | 1 | 1 | 0 | 16x |
| 1 | 1 | 1 | 1 | 20x |

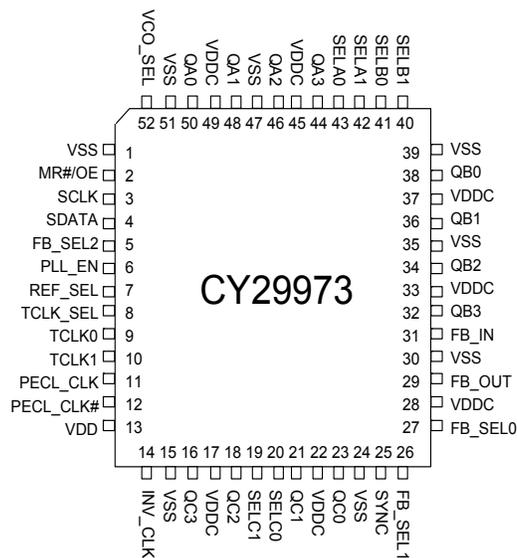
Note

1. x = reference input frequency, 200 MHz < F_{VC0} < 480 MHz.

Logic Block Diagram



Pinouts



Pin Definitions^[2]

| Pin | Name | PWR | IO | Type | Description |
|-------------------------------|-------------|------|----|------|---|
| 11 | PECL_CLK | | I | PU | PECL Clock Input. |
| 12 | PECL_CLK# | | I | PD | PECL Clock Input. |
| 9 | TCLK0 | | I | PU | External Reference or Test Clock Input. |
| 10 | TCLK1 | | I | PU | External Reference or Test Clock Input. |
| 44, 46, 48, 50 | QA(3:0) | VDDC | O | | Clock Outputs. See Table 2 on page 4 for frequency selections. |
| 32, 34, 36, 38 | QB(3:0) | VDDC | O | | Clock Outputs. See Table 2 on page 4 for frequency selections. |
| 16, 18, 21, 23 | QC(3:0) | VDDC | O | | Clock Outputs. See Table 2 on page 4 for frequency selections. |
| 29 | FB_OUT | VDDC | O | | Feedback Clock Output. Connect to FB_IN for normal operation. The divider ratio for this output is set by FB_SEL(0:2). See Table 1 on page 1 . A bypass delay capacitor at this output control Input Reference or Output Banks phase relationships. |
| 25 | SYNC | VDDC | O | | Synchronous Pulse Output. This output is used for system synchronization. The rising edge of the output pulse is in sync with both the rising edges of QA (0:3) and QC(0:3) output clocks regardless of the divider ratios selected. |
| 42, 43 | SELA(1,0) | | I | PU | Frequency Select Inputs. These inputs select the divider ratio at QA(0:3) outputs. See Table 2 on page 4 . |
| 40, 41 | SELB(1,0) | | I | PU | Frequency Select Inputs. These inputs select the divider ratio at QB(0:3) outputs. See Table 2 on page 4 . |
| 19, 20 | SELC(1,0) | | I | PU | Frequency Select Inputs. These inputs select the divider ratio at QC(0:3) outputs. See Table 2 on page 4 . |
| 5, 26, 27 | FB_SEL(2:0) | | I | PU | Feedback Select Inputs. These inputs select the divide ratio at FB_OUT output. See Table 1 on page 1 . |
| 52 | VCO_SEL | | I | PU | VCO Divider Select Input. When set LOW, the VCO output is divided by 2. When set HIGH, the divider is bypassed. See Table 1 on page 1 . |
| 31 | FB_IN | | I | PU | Feedback Clock Input. Connect to FB_OUT for accessing the PLL. |
| 6 | PLL_EN | | I | PU | PLL Enable Input. When asserted HIGH, PLL is enabled. When LOW, PLL is bypassed. |
| 7 | REF_SEL | | I | PU | Reference Select Input. When HIGH, the PECL inputs are selected. When LOW, TCLK[0:1] are selected. |
| 8 | TCLK_SEL | | I | PU | TCLK Select Input. When LOW, TCLK0 is selected. When HIGH TCLK1 is selected. |
| 2 | MR#/OE | | I | PU | Master Reset or Output Enable Input. When asserted LOW, resets all of the internal flip-flops and also disables all of the outputs. When pulled HIGH, releases the internal flip-flops from reset and enables all of the outputs. |
| 14 | INV_CLK | | I | PU | Inverted Clock Input. When set HIGH, QC(2,3) outputs are inverted. When set LOW, the inverter is bypassed. |
| 3 | SCLK | | I | PU | Serial Clock Input. Clocks data at SDATA into the internal register. |
| 4 | SDATA | | I | PU | Serial Data Input. Input data is clocked to the internal register to enable or disable individual outputs. This provides flexibility in power management. |
| 17, 22, 28, 33, 37, 45, 49 | VDDC | | | | 3.3V Power Supply for Output Clock Buffers. |
| 13 | VDD | | | | 3.3V Supply for PLL. |
| 1, 15, 24, 30, 35, 39, 47, 51 | VSS | | | | Common Ground. |

Note

2. A bypass capacitor (0.1µF) must be placed as close as possible to each positive power (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics is cancelled by the lead inductance of the traces.

Description

The CY29973 has an integrated PLL that provides low-skew and low-jitter clock outputs for high-performance microprocessors. Three independent banks of four outputs and an independent PLL feedback output, FB_OUT, provide exceptional flexibility for possible output configurations. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 480 MHz. This allows a wide range of output frequencies up to 125 MHz.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by FB_SEL(0:2) and VCO_SEL select inputs, refer to [Table 1 on page 1](#). The VCO frequency is then divided down to provide the required output frequencies. These dividers are set by SELA(0,1), SELB(0,1), SELC(0,1) select inputs, see [Table 2](#). For situations where the VCO needs to run at relatively low frequencies and hence might not be stable, assert VCO_SEL LOW to divide the VCO frequency by 2. This maintains the desired output relationships, but provides an enhanced PLL lock range.

The CY29973 is also capable of providing inverted output clocks. When INV_CLK is asserted high, QC2 and QC3 output clocks are inverted. These clocks could be used as feedback outputs to the CY29973 or a second PLL device to generate early or late clocks for a specific design. This inversion does not affect the output to output skew.

Zero Delay Buffer

When used as a zero delay buffer the CY29973 is likely to be in a nested clock tree application. For these applications the CY29973 offers a low voltage PECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The CY29973 then can lock onto the LVPECL reference and translate with near zero delay to low skew outputs.

By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock the Tpd of the CY29973 is a function of the configuration used.

Glitch-Free Output Frequency Transitions

Customarily when output buffers have their internal counters changed “on the fly” their output clock periods will:

1. Contain short or “runt” clock periods. These are clock cycles in which the cycle(s) are shorter in period than either the old or new frequency that is being transitioned to.
2. Contain stretched clock periods. These are clock cycles in which the cycle(s) are longer in period than either the old or new frequency that is being transitioned to.

This device specifically includes logic to guarantee that runt and stretched clock pulses do not occur if the device logic levels of any or all of the following pins changed “on the fly” while it is operating: SELA, SELB, SELC, and VCO_SEL.

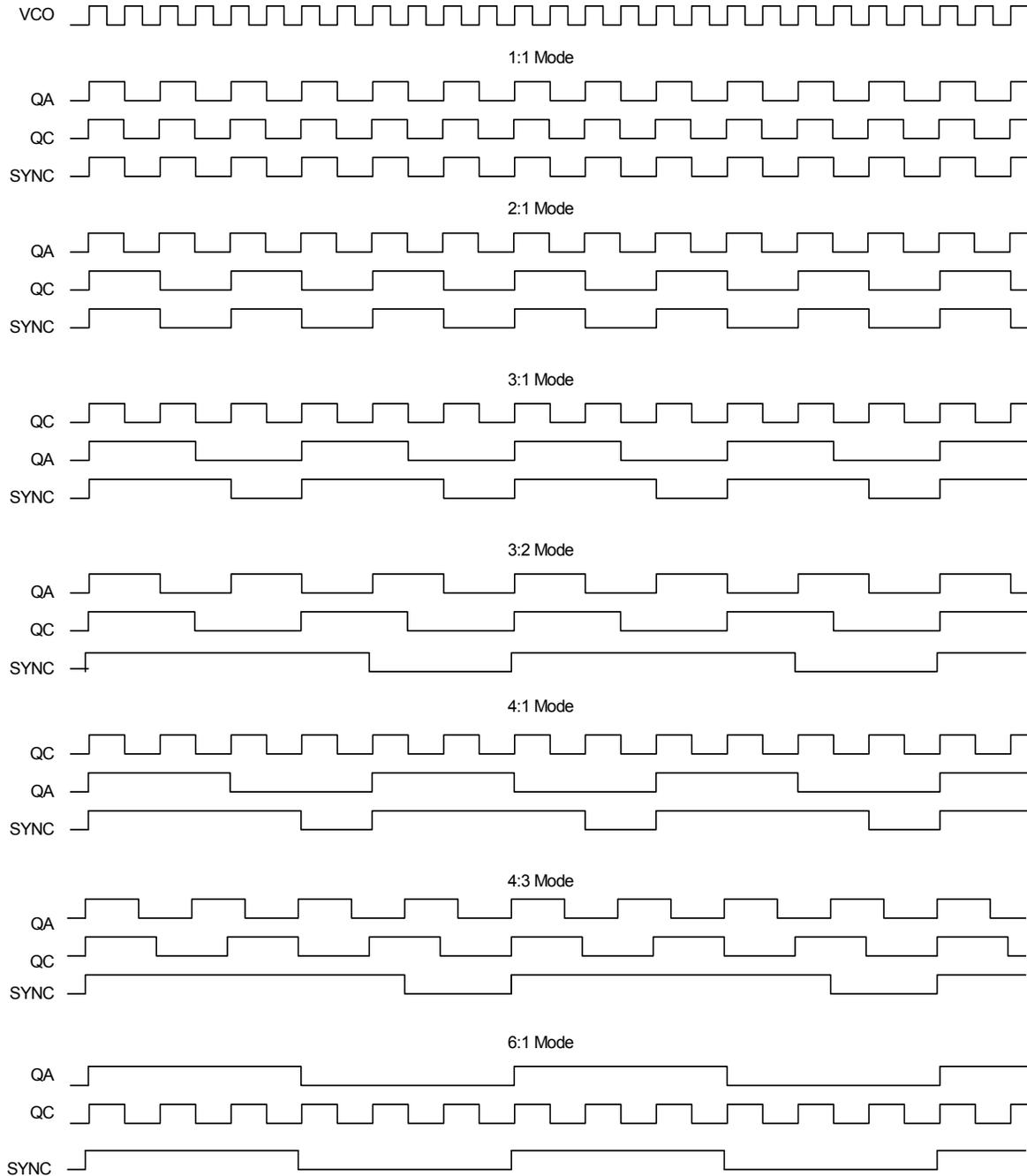
Table 2. Divider Table

| VCO_SEL | SELA1 | SELA0 | QA | SELB1 | SELB0 | QB | SELC1 | SELC0 | QC |
|---------|-------|-------|--------|-------|-------|--------|-------|-------|--------|
| 0 | 0 | 0 | VCO/8 | 0 | 0 | VCO/8 | 0 | 0 | VCO/4 |
| 0 | 0 | 1 | VCO/12 | 0 | 1 | VCO/12 | 0 | 1 | VCO/8 |
| 0 | 1 | 0 | VCO/16 | 1 | 0 | VCO/16 | 1 | 0 | VCO/12 |
| 0 | 1 | 1 | VCO/24 | 1 | 1 | VCO/20 | 1 | 1 | VCO/16 |
| 1 | 0 | 0 | VCO/4 | 0 | 0 | VCO/4 | 0 | 0 | VCO/2 |
| 1 | 0 | 1 | VCO/6 | 0 | 1 | VCO/6 | 0 | 1 | VCO/4 |
| 1 | 1 | 0 | VCO/8 | 1 | 0 | VCO/8 | 1 | 0 | VCO/6 |
| 1 | 1 | 1 | VCO/12 | 1 | 1 | VCO/10 | 1 | 1 | VCO/8 |

SYNC Output

In situations where output frequency relationships are not integer multiples of each other the SYNC output provides a signal for system synchronization. The CY29973 monitors the relationship between the QA and the QC output clocks. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse depend on the higher of the QA and QC output frequencies. The following timing diagram illustrates various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the QA and QC outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

Figure 1. SYNC Output for Different Input and Out Ratio

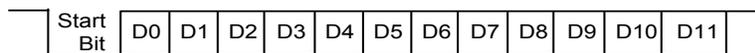


Power Management

The individual output enable or freeze control of the CY29973 allows the user to implement unique power management schemes into the design. The outputs are stopped in the logic '0' state when the freeze control bits are activated. The serial input register contains one programmable freeze enable bit for 12 of the 14 output clocks. The QC0 and FB_OUT outputs can not be frozen with the serial port, this avoids any potential lock up situation must an error occur in the loading of the serial data. An output is frozen when a logic '0' is programmed and enabled when a logic '1' is written. The enabling and freezing of individual outputs is done in such a manner as to eliminate the possibility of partial "runt" clocks.

The serial input register is programmed through the SDATA input by writing a logic '0' start bit followed by 12 NRZ freeze enable bits. The period of each SDATA bit equals the period of the free running SCLK signal. The SDATA is sampled on the rising edge of SCLK.

Figure 2. Control Bit Map



D0-D3 are the control bits for QA0-QA3, respectively
 D4-D7 are the control bits for QB0-QB3, respectively
 D8-D10 are the control bits for QC1-QC3, respectively
 D11 is the control bit for SYNC

Absolute Maximum Conditions^[3]

Maximum Input Voltage Relative to V_{SS} :..... $V_{SS} - 0.3 V$
 Maximum Input Voltage Relative to V_{DD} :..... $V_{DD} + 0.3 V$
 Storage Temperature:..... $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature:..... $-40^{\circ}C$ to $+85^{\circ}C$
 Maximum ESD protection..... 2 kV
 Maximum Power Supply:..... 5.5 V
 Maximum Input Current:..... ± 20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions must be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} must be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications

$V_{DD} = 2.9 V$ to $3.6 V$, $V_{DDC} = 3.3 V \pm 10\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|---|-------------------|----------------|-----|----------------|---------|
| V_{IL} | Input Low Voltage | | V_{SS} | – | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | – | V_{DD} | V |
| V_{PP} | Peak-to-Peak Input Voltage PECL_CLK | | 300 | – | 1000 | mV |
| V_{CMR} | Common Mode Range PECL_CLK ^[4] | | $V_{DD} - 2.0$ | – | $V_{DD} - 0.6$ | V |
| I_{IL} | Input Low Current ^[5] | | – | – | –120 | μA |
| I_{IH} | Input High Current ^[5] | | – | – | 120 | μA |
| V_{OL} | Output Low Voltage ^[6] | $I_{OL} = 20$ mA | – | – | 0.5 | V |
| V_{OH} | Output High Voltage ^[6] | $I_{OH} = -20$ mA | 2.4 | – | – | V |
| I_{DDQ} | Quiescent Supply Current | | – | 10 | 15 | mA |
| I_{DDA} | PLL Supply Current | V_{DD} only | – | 15 | 20 | mA |

Notes

- Multiple Supplies: The voltage on any input or IO pin cannot exceed the power pin during power up. Power supply sequencing is not required.
- The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
- Inputs have pull up/pull down resistors that effect input current.
- Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.

DC Electrical Specifications

 $V_{DD} = 2.9\text{ V to }3.6\text{ V}$, $V_{DDC} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ (continued)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|------------------------|---|-----|-----|-----|----------|
| I_{DD} | Dynamic Supply Current | QA and QB at 60 MHz, QC at 120 MHz, CL=30 pF | – | 225 | – | mA |
| | | QA and QB at 25 MHz, QC at 50 MHz, CL=30 pF | – | 125 | – | |
| C_{in} | Input Pin Capacitance | | – | 4 | – | pF |
| Z_{OUT} | Output Impedance | | 15 | 18 | 22 | Ω |

AC Electrical Specifications

 $V_{DD} = 2.9\text{ V to }3.6\text{ V}$, $V_{DDC} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ [7]

| Parameter | Description | Conditions | Min | Typ. | Max | Unit | |
|------------|---|----------------|-----------------------|-----------|----------------|------|-----|
| Tr/Tf | TCLK Input Rise or Fall | | | – | 3.0 | ns | |
| Fref | Reference Input Frequency | | Note 8 | – | Note 8 | MHz | |
| FrefDC | Reference Input Duty Cycle | | 25 | – | 75 | % | |
| Fvco | PLL VCO Lock Range | | 200 | – | 480 | MHz | |
| Tlock | Maximum PLL lock Time | | – | – | 10 | ms | |
| Tr/Tf | Output Clocks Rise or Fall Time ^[9] | 0.8 V to 2.0 V | 0.15 | – | 1.2 | ns | |
| Fout | Maximum Output Frequency | Q ($\div 2$) | – | – | 125 | MHz | |
| | | Q ($\div 4$) | – | – | 120 | | |
| | | Q ($\div 6$) | – | – | 80 | | |
| | | Q ($\div 8$) | – | – | 60 | | |
| FoutDC | Output Duty Cycle ^[9] | | TCYCLE/2 – 750 | – | TCYCLE/2 + 750 | ps | |
| tpZL, tpZH | Output Enable Time ^[9] (all outputs) | | 2 | – | 10 | ns | |
| tpLZ, tpHZ | Output Disable Time ^[9] (all outputs) | | 2 | – | 8 | ns | |
| TCCJ | Cycle to Cycle Jitter ^[9] (peak to peak) | | – | ± 100 | – | ps | |
| TSKEW | Any Output to Any Output Skew ^[9, 10] | | – | 250 | 350 | ps | |
| Tpd | Propagation Delay ^[10, 11] | PECL_CLK | –225 | –25 | 175 | ps | |
| | | TCLK0 | QFB = ⁽³⁸⁾ | –70 | 130 | | 330 |
| | | TCLK1 | | –130 | 70 | | 270 |

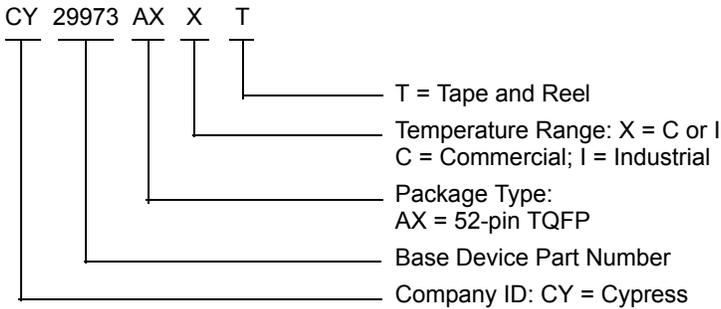
Notes

7. Parameters are guaranteed by design and characterization. Not 100% tested in production.
8. Maximum and minimum input reference is limited by VCO lock range.
9. Outputs loaded with 30pF each.
10. 50 Ω transmission line terminated into VDD/2.
11. Tpd is specified for a 50MHz input reference. Tpd does not include jitter.

Ordering Information

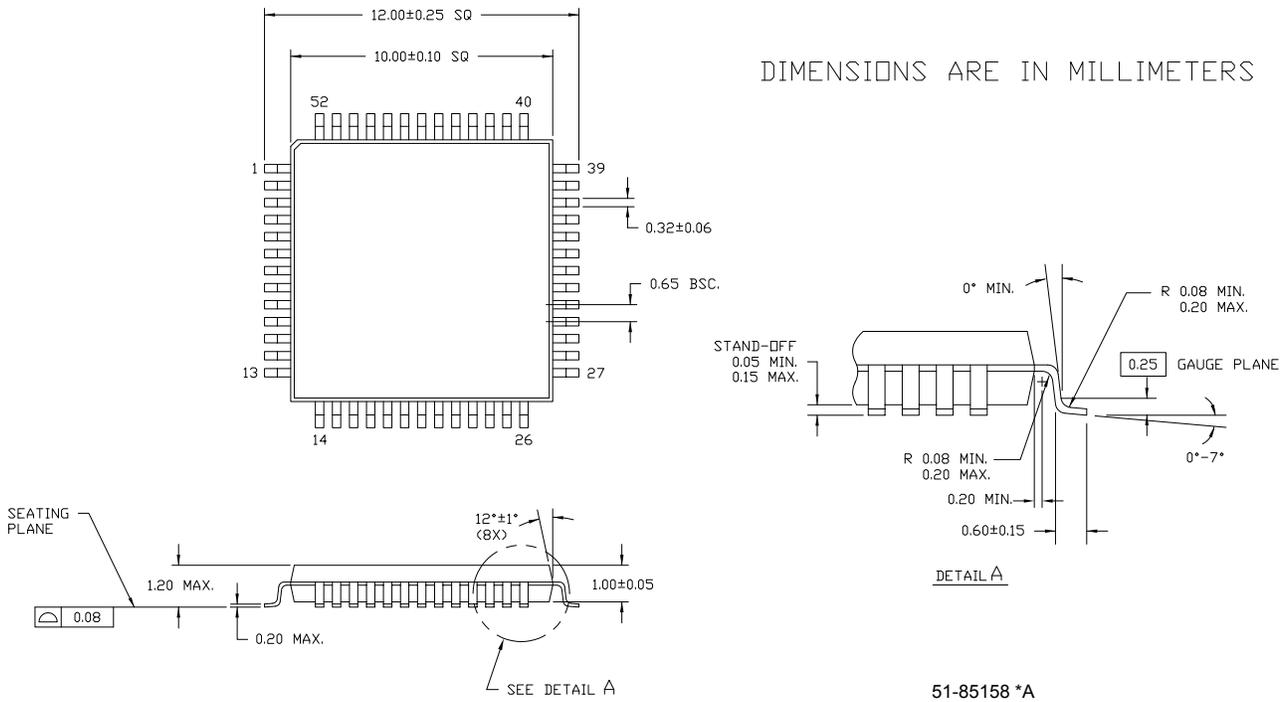
| Part Number | Package Type | Production Flow |
|----------------|-----------------------------|------------------------------|
| Pb-free | | |
| CY29973AXI | 52-pin TQFP | Industrial, -40 °C to +85 °C |
| CY29973AXIT | 52-pin TQFP – Tape and reel | Industrial, -40 °C to +85 °C |

Ordering Code Definitions



Package Drawing and Dimensions

Figure 3. 52-pin Thin Plastic Quad Flat Pack (10 × 10 × 1.0 mm) A52B



Acronyms

| Acronym | Description |
|---------|---|
| I/O | Input/Output |
| LVPECL | Low Voltage Positive/Pseudo Emitter Coupled Logic |
| PECL | Positive/Pseudo Emitter Coupled Logic |
| PLL | phase locked loop |
| TQFP | thin quad flat pack |
| VCO | voltage-controlled oscillator |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| Hz | Hertz |
| kHz | kilo Hertz |
| MHz | Mega Hertz |
| μA | micro Amperes |
| mA | milli Amperes |
| ms | milli seconds |
| ns | nano seconds |
| Ω | ohms |
| % | percent |
| μF | micro Farads |
| pF | pico Farads |
| ps | pico seconds |
| kV | kilo Volts |
| mV | milli Volts |
| V | Volts |
| W | Watts |

Document History Page

| Document Title: CY29973 3.3 V 125 MHz Multi-Output Zero Delay Buffer | | | | |
|--|---------|-----------------|-----------------|--|
| Document Number: 38-07291 | | | | |
| REV. | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 111102 | BRK | 02/07/02 | New data sheet |
| *A | 122883 | RBI | 12/22/02 | Added power up requirements to Maximum Ratings |
| *B | 200081 | RGL | 01/22/04 | Added Z _{OUT} specifications in the DC Electrical Specs Changed the Package Drawing and Dimension to CY standard |
| *C | 2562606 | AESA | 09/09/08 | Updated template. Added Note "Not recommended for new designs." Added part number CY29973AXI and CY29973AXIT in ordering information table. |
| *D | 2904743 | CXQ | 04/05/2010 | Removed inactive part numbers CY29973AI and CY29973AIT. Updated package diagram. |
| *E | 3163592 | CXQ | 02/05/2011 | Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated in new template. |

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