

# MoBL<sup>®</sup> 1-Mbit (64 K × 16) Static RAM

### **Features**

- Temperature ranges
  □ Industrial: -40 °C to 85 °C
- Very high speed: 55 ns
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62127BV
- Ultra-low active power
  - □ Typical active current: 0.85 mA at f = 1 MHz
     □ Typical active current: 5 mA at f = f<sub>MAX</sub>
- Ultra-low standby power
- Easy memory expansion with CE and OE features
- Automatic power-down when deselected
- Available in Pb-free 48-ball FBGA and 44-pin TSOP Type II packages

### **Functional Description**

The CY62127DV30 is a high-performance CMOS static RAM organized as 64 K words by 16-bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life<sup>™</sup> (MoBL<sup>®</sup>) in portable

applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected (CE HIGH or both BHE and BLE are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected (CE HIGH), outputs are disabled (OE HIGH), both byte high enable and byte low enable are disabled (BHE, BLE HIGH) or during a write operation (CE LOW and WE LOW).

CY62127DV30

Writing to the device is accomplished by taking chip enable  $\overline{(CE)}$  and write enable  $\overline{(WE)}$  inputs LOW. If byte low enable  $\overline{(BLE)}$  is LOW, then data from I/O pins  $(I/O_0 \text{ through } I/O_7)$ , is written into the location specified on the address pins  $(A_0 \text{ through } A_{15})$ . If byte high enable  $\overline{(BHE)}$  is LOW, then data from I/O pins  $(I/O_8 \text{ through } I/O_{15})$  is written into the location specified on the address pins  $(A_0 \text{ through } A_{15})$ .

Reading from the device is accomplished by taking chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) LO<u>W</u> while forcing the write enable (WE) HIGH. If byte low enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If byte high enable (BHE) is LOW, then data from memory appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this datasheet for a complete description of read and write modes.

## Logic Block Diagram



Cypress Semiconductor Corporation Document Number: 38-05229 Rev. \*M 198 Champion Court • San Jose, CA 95134-1709 • 408-943-2600



# CY62127DV30

# Contents

Product Portfolio	3
Pin Configurations	3
Maximum Ratings	4
Operating Range	4
DC Electrical Characteristics	4
Capacitance	4
Thermal Resistance	5
AC Test Loads and Waveforms	5
Data Retention Characteristics	5
Switching Characteristics	
Truth Table	

Ordering Information	10
Ordering Code Definitions	
Package Diagrams	11
Acronyms	12
Document Conventions	12
Units of Measure	12
Document History Page	13
Sales, Solutions, and Legal Information	14
Worldwide Sales and Design Support	14
Products	14
PSoC Solutions	14



## **Product Portfolio**

						Power Dissipation					
Product	Vcc	Range	e (V)	Speed		Operating, I <sub>CC</sub> (mA)				Standby	I <sub>SB2</sub> (μΑ)
Troduct				(ns)	f = 1 MHz f = f <sub>MAX</sub> Standby			'SB2 (μ~)			
	Min	Тур	Мах		<b>Typ</b> <sup>[1]</sup>	Max	<b>Typ</b> <sup>[1]</sup>	Max	Range	<b>Typ</b> <sup>[1]</sup>	Мах
CY62127DV30LL	2.2	3.0	3.6	55	0.85	1.5	5	10	Industrial	1.5	4

# **Pin Configurations**



TSOP II (Forward) <sup>[2, 3]</sup> Top View						
A <sub>4</sub> E A <sub>3</sub> E	1 2	44 43				
A <sub>2</sub> L	3	42				
A₁ Ľ	4	41	I OE			
A <sub>0</sub> E	5	40	BHE			
CEL	6	39	BLE			
I/O <sub>0</sub> []	7	38	□ I/O <sub>15</sub>			
I/O <sub>1</sub> Γ	8	37	I/O <sub>14</sub>			
I/O <sub>2</sub> [	9	36	I/O <sub>13</sub>			
I/O <sub>3</sub> [	10	35				
V <sub>CČ</sub> ⊑	11	34	V <sub>SS</sub>			
V <sub>SS</sub> [	12	33	Vcc			
I/O4 🗆	13	32	□ I/Õ <sub>11</sub>			
I/O <sub>5</sub> ⊑	14	31	I/O <sub>10</sub>			
I/O <sub>6</sub> 🗆	15	30	I/O <sub>9</sub>			
1 <u>/07</u>	16	29	□ I/O <sub>8</sub>			
WEL	17	28	NC NC			
A <sub>15</sub> L	18	27	A <sub>8</sub>			
A <sub>14</sub> L	19	26	A9			
A <sub>13</sub>	20	25				
A <sub>12</sub> [	21	24				
NC L	22	23	UNU L			

Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25 \degree C$ . 2. NC pins are not connected to the die. Expansion pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M 3. Pin #23 of TSOP-II and E3 ball of FBGA are DNU, which have to be left floating or tied to Vss to ensure proper application.



## **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature65 °C to +150 °C
Ambient temperature with power applied–55 °C to +125 °C
Supply voltage to ground potential–0.3 V to 3.9 V
DC voltage applied to outputs in high Z State $^{[4]}$ –0.3 V to $V_{CC}$ + 0.3 V

# **DC Electrical Characteristics**

DC input voltage<sup>[4]</sup>.....-0.3 V to V<sub>CC</sub> + 0.3 V Output current into outputs (LOW) ...... 20 mA Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015) Latch-up current ......> 200 mA

## **Operating Range**

Range	Ambient Temperature (T <sub>A</sub> )	<b>V<sub>CC</sub></b> <sup>[5]</sup>
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Over the	Operating	Range
----------	-----------	-------

Devenueter	Description	Test Co			-55		Unit
Parameter	Description	Test Conditions		Min	<b>Typ</b> <sup>[6]</sup>	Max	Unit
V <sub>OH</sub>	Output HIGH voltage	$2.2 \leq V_{CC} \leq 2.7$	I <sub>OH</sub> = -0.1 mA	2.0	-	-	V
		$2.7 \leq V_{CC} \leq 3.6$	I <sub>OH</sub> = -1.0 mA	2.4	-	-	
V <sub>OL</sub>	Output LOW voltage	$2.2 \leq V_{CC} \leq 2.7$	I <sub>OL</sub> = 0.1 mA	-	-	0.4	V
		$2.7 \leq V_{CC} \leq 3.6$	I <sub>OL</sub> = 2.1 mA	-	-	0.4	
V <sub>IH</sub>	Input HIGH voltage	$2.2 \leq V_{CC} \leq 2.7$		1.8	-	V <sub>CC</sub> + 0.3	V
		$2.7 \leq V_{CC} \leq 3.6$	$2.7 \le V_{CC} \le 3.6$		-	V <sub>CC</sub> + 0.3	
V <sub>IL</sub>	Input LOW voltage	$2.2 \le V_{CC} \le 2.7$		-0.3	-	0.6	V
		$2.7 \leq V_{CC} \leq 3.6$	$2.7 \le V_{CC} \le 3.6$		-	0.8	
I <sub>IX</sub>	Input leakage current	$GND \leq V_I \leq V_{CC}$	$GND \le V_I \le V_{CC}$		-	+1	μA
I <sub>OZ</sub>	Output leakage current	$GND \le V_O \le V_{CC}$ , Outp	out disabled	-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	$f = f_{MAX} = 1/t_{RC}$	V <sub>CC</sub> = 3.6 V,	-	5	10	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA, CMOS level	-	0.85	1.5	
I <sub>SB1</sub>	Automatic CE power-down current— CMOS Inputs	$\label{eq:cellson} \begin{array}{l} \hline CE \geq V_{CC} - 0.2 \text{ V}, \ V_{IN} \geq V_{CC} - 0.2 \text{ V}, \\ V_{IN} \leq \underline{0.2} \text{ V}, \ f = f_{\underline{MAX}} \ (\text{Add}\underline{ress} \ \text{and} \ \text{data only}), \\ f = 0 \ (\text{OE}, \ \text{WE}, \ \text{BHE} \ \text{and} \ \text{BLE}) \end{array}$		-	1.5	4	μA
I <sub>SB2</sub>	Automatic CE power-down current— CMOS Inputs	$\label{eq:cell} \begin{aligned} \overline{CE} \geq V_{CC} &= 0.2 \text{ V}, V_{IN} \\ V_{IN} \leq 0.2 \text{ V}, \text{ f = 0},  V_{CC} \end{aligned}$		-	1.5	4	μA

## Capacitance

Parameter <sup>[7]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz	8	pF
C <sub>OUT</sub>	Output capacitance	$V_{CC} = V_{CC(typ)}$	8	pF

- 4. V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns., V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
  5. Full device operation requires linear ramp of V<sub>CC</sub> from 0 V to V<sub>CC(min)</sub> and V<sub>CC</sub> must be stable at V<sub>CC(min)</sub> for 500 µs.
  6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
  7. Tested initially and after any design or process changes that may affect these parameters.



## **Thermal Resistance**

Parameter <sup>[8]</sup>	Description	Test Conditions	FBGA	TSOP-II	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch,	55	76	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)	two-layer printed circuit board	12	11	°C/W

## AC Test Loads and Waveforms





Equivalent to: THEVENIN EQUIVALENT

R<sub>TH</sub>

Parameters	2.5 V (2.2 V – 2.7 V)	3.0 V (2.7 V – 3.6 V)	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

## **Data Retention Characteristics**

Parameter	Description	Conditions	Min	<b>Typ</b> <sup>[9]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.5	-	-	V
I <sub>CCDR</sub>	Data retention current	$ \begin{array}{l} V_{CC} \mbox{=} 1.5 \mbox{ V}, \ensuremath{\overline{CE}} \geq V_{CC} - 0.2 \mbox{ V}, \\ V_{IN} \geq V_{CC} - 0.2 \mbox{ V} \mbox{ or } V_{IN} \leq 0.2 \mbox{ V} \end{array} $		-	3	μA
t <sub>CDR</sub>	Chip deselect to data retention time		0	-	_	ns
t <sub>R</sub> <sup>[10]</sup>	Operation recovery time		55	-	_	ns

## Data Retention Waveform<sup>[11]</sup>



- Notes
  8. Tested initially and after any design or process changes that may affect these parameters.
  9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
  10. <u>Full device</u> operation requires <u>line</u>ar V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min</sub>) > 200 μs.
  11. <u>BHE.BLE</u> is the AND of both <u>BHE</u> and <u>BLE</u>. Chip can be deselected by either disabling the Chip Enable signals or by disabling both byte enable pins.



## **Switching Characteristics**

(Over the Operating Range)

Parameter <sup>[12]</sup>	Description	CY62127DV30-55		Unit
Parameter	Description	Min	Мах	Unit
Read Cycle	•			
t <sub>RC</sub>	Read cycle time	55	-	ns
t <sub>AA</sub>	Address to data valid	-	55	ns
t <sub>OHA</sub>	Data hold from address change	10	-	ns
t <sub>ACE</sub>	CE LOW to data valid	-	55	ns
t <sub>DOE</sub>	OE LOW to data valid	-	25	ns
t <sub>LZOE</sub>	OE LOW to low Z <sup>[13]</sup>	5	-	ns
t <sub>HZOE</sub>	OE HIGH to high Z <sup>[13, 14]</sup>	_	20	ns
t <sub>LZCE</sub>	CE LOW to low Z <sup>[13]</sup>	10	_	ns
t <sub>HZCE</sub>	CE HIGH to high Z <sup>[13, 14]</sup>	_	20	ns
t <sub>PU</sub>	CE LOW to power-up	0	_	ns
t <sub>PD</sub>	CE HIGH to power-down	_	55	ns
t <sub>DBE</sub>	BLE/BHE LOW to data valid	_	55	ns
t <sub>LZBE</sub> <sup>[15]</sup>	BLE/BHE LOW to low Z <sup>[13]</sup>	5	_	ns
t <sub>HZBE</sub>	BLE/BHE HIGH to high Z <sup>[13, 14]</sup>	_	20	ns
Write Cycle <sup>[16]</sup>				
t <sub>WC</sub>	Write cycle time	55	_	ns
t <sub>SCE</sub>	CE LOW to write end	40	_	ns
t <sub>AW</sub>	Address setup to write end	40	_	ns
t <sub>HA</sub>	Address hold from write end	0	_	ns
t <sub>SA</sub>	Address setup to write start	0	_	ns
t <sub>PWE</sub>	WE pulse width	40	_	ns
t <sub>BW</sub>	BLE/BHE LOW to write end	40	_	ns
t <sub>SD</sub>	Data setup to write end	25	_	ns
t <sub>HD</sub>	Data hold from write end	0	_	ns
t <sub>HZWE</sub>	WE LOW to high Z <sup>[13, 14]</sup>	_	20	ns
t <sub>LZWE</sub>	WE HIGH to low Z <sup>[13]</sup>	10	-	ns

Notes

12. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of V<sub>CC(typ.)</sub>/2, input pulse levels of 0 to V<sub>CC(typ.)</sub>, and output loading of the specified I<sub>OL</sub>.
13. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZDE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
14. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
15. If both byte enables are toggled together, this value is 10 ns.

16. The internal Write time of the memory is defined by the overlap of WE,  $\overline{CE} = V_{\parallel L}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{\parallel L}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.



#### Switching Waveforms







Figure 3. Write Cycle No. 1 (WE Controlled)<sup>[20, 21, 22, 23, 24]</sup>



- 17. <u>Dev</u>ice is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE} = V_{IL}$ .
- 18. WE is HIGH for Read cycle.
- 19. Address valid prior to or coincident with  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.
- 20. t<sub>HZCE</sub>, t<sub>HZCE</sub>, t<sub>HZEE</sub>, and t<sub>HZWE</sub> transitions are measured when the <u>outputs</u> enter a <u>high-impedance</u> state.
   21. The internal Write time of the memory is defined by the overlap of WE, CE = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

- 22. Data I/O is high-impedance if  $\overline{OE} = V_{\text{H}}$ . 23. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state. 24. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.



#### Switching Waveforms (continued)



Figure 4. Write Cycle No. 2 (CE Controlled)<sup>[25, 26, 27, 28, 29]</sup>

- 25. t<sub>HZCE</sub>, t<sub>HZCE</sub>, t<sub>HZEE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter <u>a high-impedance</u> state.
   26. The internal Write time of the memory is defined by the overlap of WE, CE = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

- 27. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ . 28. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state. 29. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.



#### Switching Waveforms (continued)



**Truth Table** 

CE	WE	OE	BHE	BLE	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
Н	Х	Х	Х	Х	High Z	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
Х	Х	Х	Н	Н	High Z	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
L	Н	L	L	L	Data Out	Data Out	Read All bits	Active (I <sub>CC</sub> )
L	Н	L	Н	L	Data Out	High Z	Read Lower Byte Only	Active (I <sub>CC</sub> )
L	Н	L	L	Н	High Z	Data Out	Read Upper Byte Only	Active (I <sub>CC</sub> )
L	Н	Н	L	L	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	Н	Н	L	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	Н	L	Н	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	L	Х	L	L	Data In	Data In	Write	Active (I <sub>CC</sub> )
L	L	Х	Н	L	Data In	High Z	Write Lower Byte Only	Active (I <sub>CC</sub> )
L	L	Х	L	Н	High Z	Data In	Write Upper Byte Only	Active (I <sub>CC</sub> )



# **Ordering Information**

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and see product summary page at http://www.cypress.com/products or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62127DV30LL-55BVXI	51-85150	48-ball fine pitch BGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial

### **Ordering Code Definitions**





#### **Package Diagrams**





NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.







# Acronyms

Acronym	Description		
BHE	byte high enable		
BLE	byte low enable		
CMOS	complementary metal oxide semiconductor		
CE	chip enable		
I/O	input/output		
ŌĒ	output enable		
SRAM	static random access memory		
TSOP	thin small outline package		
FBGA	fine-pitch ball grid array		
WE	write enable		

## **Document Conventions**

### **Units of Measure**

Symbol	Unit of Measure			
ns	nanosecond			
V	volt			
μA	microampere			
mA	milliampere			
pF	picofarad			
°C	degree Celsius			
W	watt			



# **Document History Page**

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	117690	JUI	08/27/02	New Datasheet
*A	127311	MPR	06/13/03	Changed From Advanced Status to Preliminary Changed Isb2 to 5 μA (L), 4 μA (LL) Changed Iccdr to 4 μA (L), 3 μA (LL) Changed Cin from 6 pF to 8 pF
*B	128341	JUI	07/22/03	Changed from Preliminary to Final Add 70-ns speed, updated ordering information
*C	129000	CDY	08/29/03	Changed Icc 1 MHz typ from 0.5 mA to 0.85 mA
*D	316039	PCI	See ECN	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote # 8 on page #4 Added Lead-Free Package ordering information on page# 9 Changed 44-lead TSOP-II package name from Z44 to ZS44
*E	346982	AJU	See ECN	Added 56-pin QFN package
*F	369955	SYT	See ECN	Added Temperature Ranges in the Features Section on Page # 1 Added Automotive Specs for $I_{IX}$ , $I_{OZ}$ , $I_{SB1}$ and $I_{SB2}$ in the Product portfolio on Page #2 and the DC Electrical Characteristics table on Page# 4 Added Automotive spec for $I_{CCDR}$ in the Data Retention Characteristics table on Page# 5 Added Pb-Free Automotive parts for 55 ns Speed bin
*G	457685	NXR	See ECN	Removed 56-pin QFN package from product offering Updated ordering Information Table
*H	470383	NXR	See ECN	Changed pin #23 of TSOP II from NC to DNU and updated footnote #2
*	2897885	RAME/NIKM	03/22/10	Removed inactive parts from the ordering information table. Updated package diagrams.
*J	3010373	AJU	08/20/2010	Updated Features Updated Product Portfolio Updated Operating Range Updated DC Electrical Characteristics Updated Data Retention Characteristics Updated Switching Characteristics Updated Ordering Information Added Ordering Code Definitions Minor edits and updated in new template
*K	3329789	RAME	07/27/11	Removed references to AN1064 SRAM system guidelines. Updated template according to current CY standards.
*L	3393183	RAME	10/03/11	Post to web.
*M	3861271	TAVA	01/08/2013	Updated Ordering Information (Updated part numbers).
				Updated Package Diagrams: spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E.



## Sales, Solutions, and Legal Information

#### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

#### Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

#### **PSoC Solutions**

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2013. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document Number: 38-05229 Rev. \*M

Revised January 8, 2013

All products and company names mentioned in this document may be the trademarks of their respective holders.