CY62147EV18 MoBL®

4-Mbit (256K x 16) Static RAM

Features

- Very high speed: 55 ns
- Wide voltage range: 1.65 V to 2.25 V
- Pin compatible with CY62147DV18
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Ultra low standby power
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in a Pb-free 48-ball very fine ball grid array (VFBGA) package

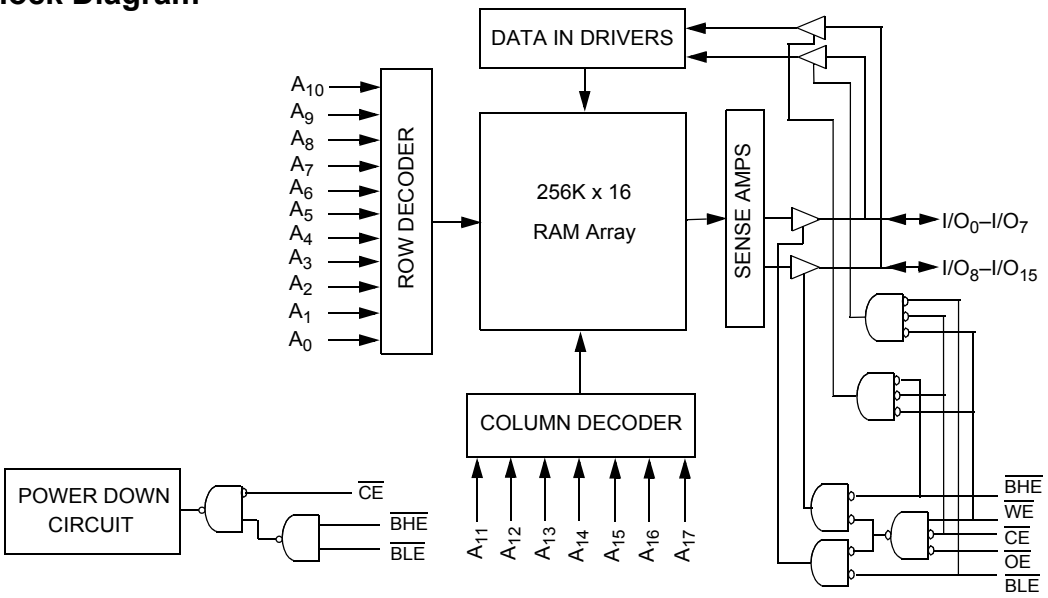
Functional Description

The CY62147EV18 is a high performance CMOS static RAM organized as 256 K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both the Byte High Enable and the Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during an active write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins apears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the "Truth Table" on page 10 for a complete description of read and write modes.

Logic Block Diagram



Contents

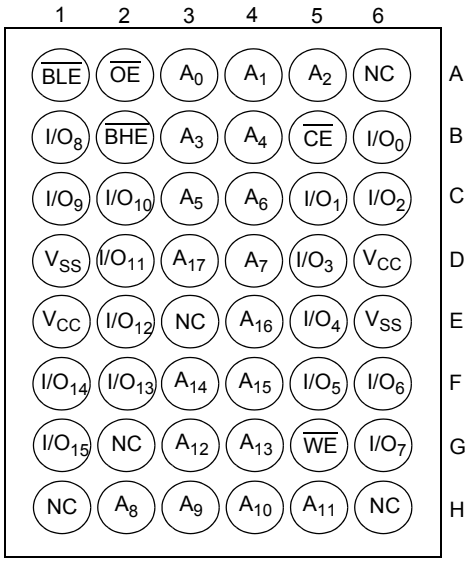
Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1MHz		f = f_{max}			
	Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62147EV18LL	1.65	1.8	2.25	55	2	2.5	15	20	1	7

Pin Configuration

Figure 1. 48-Ball VFBGA Pinout [2, 3]

Top View



Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C
2. NC pins are not connected on the die.
3. Pins H1, G2, and H6 in the VFBGA package are address expansion pins for 8 Mb, 16 Mb and 32 Mb, respectively.

Maximum Ratings

Exceeding the maximum ratings may shorten the battery life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential .....–0.2 V to + 2.45 V (V_{CCmax} + 0.2 V)

DC voltage applied to outputs in High Z state[4, 5] .....–0.2 V to 2.45 V (V_{CCmax} + 0.2 V)

DC input voltage[4, 5] .....–0.2 V to 2.45 V (V_{CCmax} + 0.2 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V (MIL-STD-883, Method 3015)

Latch up current .....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62147EV18LL	Industrial	–40 °C to +85 °C	1.65 V to 2.25 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ[7]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		1.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA			–	0.2	V
V_{IH}	Input high voltage	V_{CC} =1.65 V to 2.25 V		1.4	–	V_{CC}+ 0.2	V
V_{IL}	Input low voltage	V_{CC} =1.65 V to 2.25 V		–0.2	–	0.4	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	$V_{CC(max)}$ = 2.25 V, I_{OUT} = 0 mA CMOS levels	–	15	20	mA
		f = 1 MHz	$V_{CC(max)}$ = 2.25 V	–	2	2.5	mA
I_{SB1}[8]	Automatic power down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V) f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = V_{CC} (max)	$V_{CC(max)}$ = 2.25 V	–	1	7	µA
I_{SB2}[8]	Automatic power down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = V_{CC} (max)	$V_{CC(max)}$ = 2.25 V	–	1	7	µA

Capacitance

Parameter[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

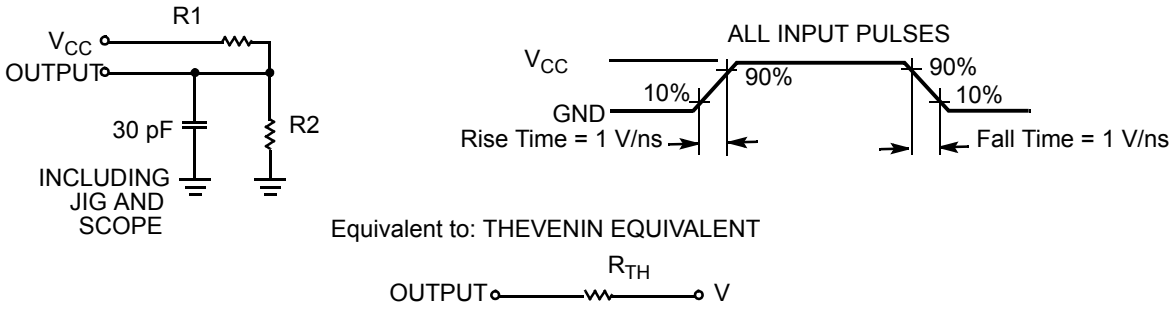
Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ =V_{CC}+0.5 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1}/ I_{SB2} / I_{CCDR} spec. Other inputs can be left floating
9. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter[10]	Description	Test Conditions	VFBGA Package	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	°C / W
Θ_{JC}	Thermal resistance (Junction to case)		10	°C / W

Figure 2. AC Test Loads and Waveforms



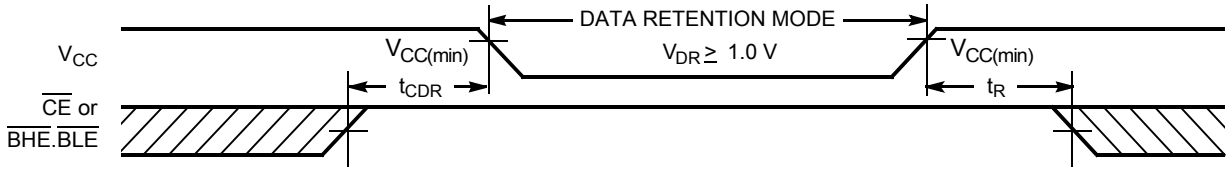
Parameters	1.80V	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ[11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR}[12]	Data retention current	V_{CC} = 1.0 V, $\overline{CE} \geq V_{CC} - 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	0.5	5	µA
t_{CDR}[10]	Chip deselect to data retention time		0	–	–	ns
t_R[13]	Operation recovery time		55	–	–	ns

Figure 3. Data Retention Waveform[14]



Notes

10. Tested initially and after any design or process changes that may affect these parameters
11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C
12. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1}/ I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs
14. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter[15,16]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[17]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[17, 18]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[17]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[17, 18]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	55	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	55	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[17]	10	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z[17, 18]	–	18	ns
Write Cycle[19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[17, 18]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[17]	10	–	ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "" on page 5 section
16. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. See application note AN13842 for further clarification.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the output enters a high impedence state
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled)[20, 21]

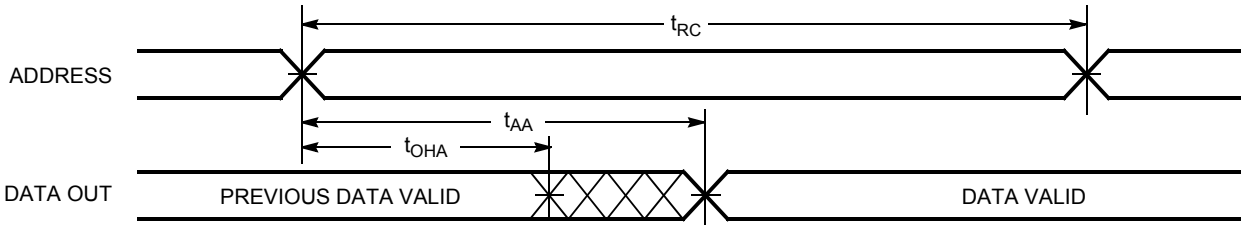
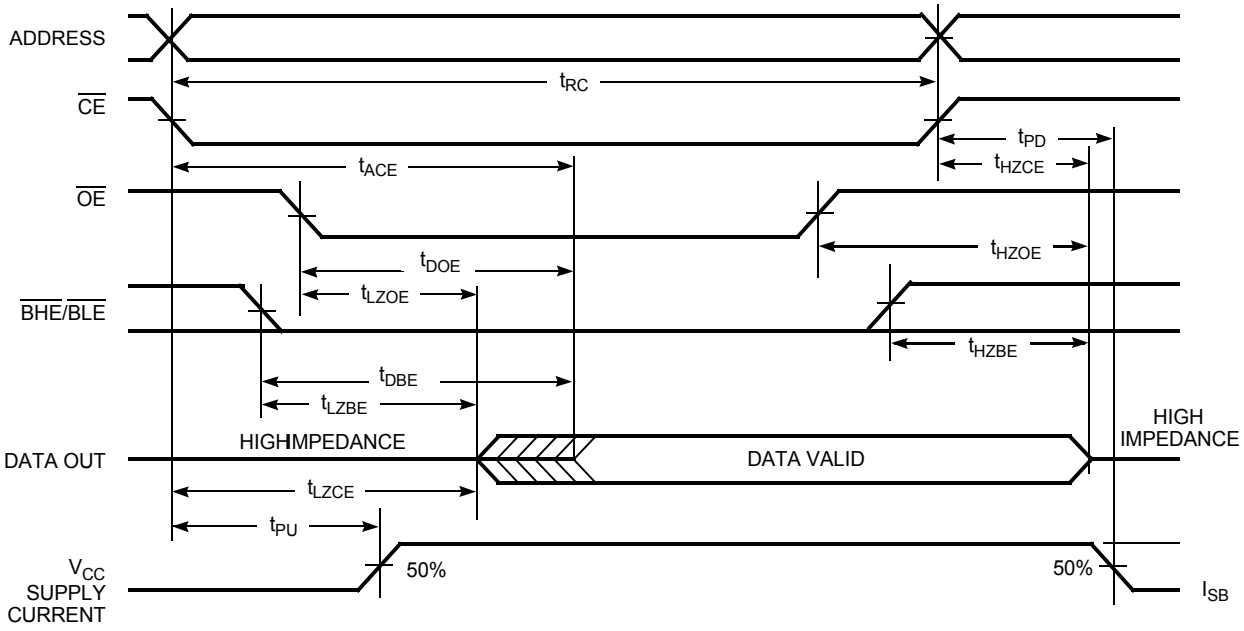


Figure 5. Read Cycle No. 2 ($\overline{OE}$ controlled)[21, 22]



Notes:
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}.
21. $\overline{WE}$ is high for read cycle.
22. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition low.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1($\overline{WE}$ Controlled) [23,24,25]

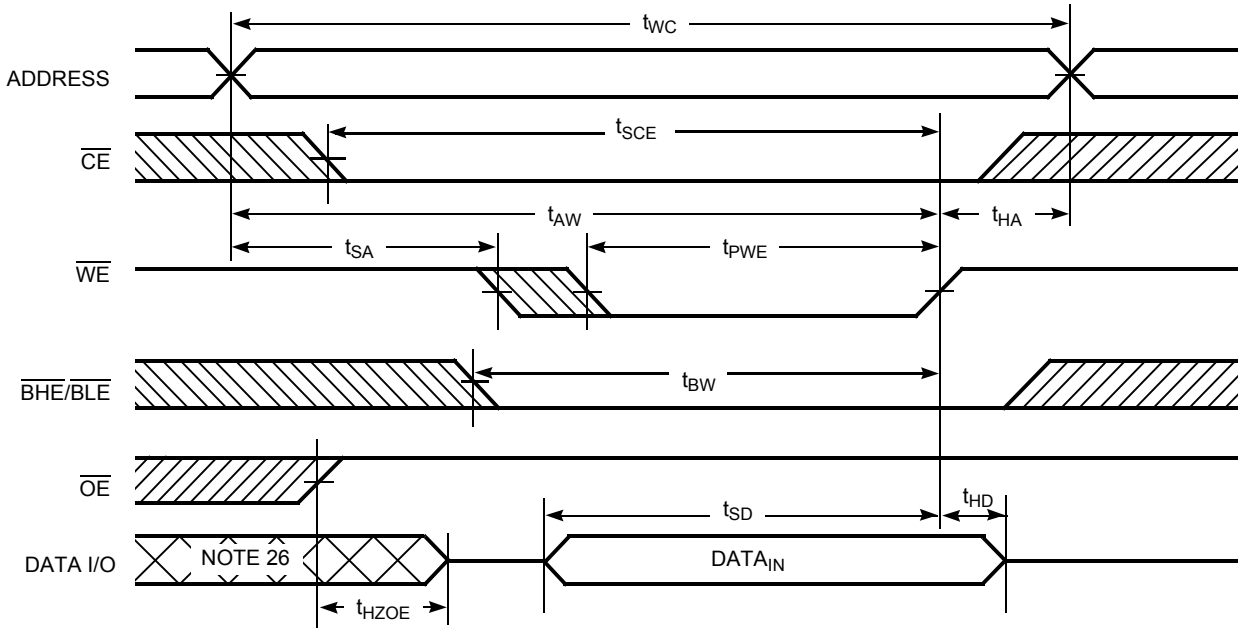
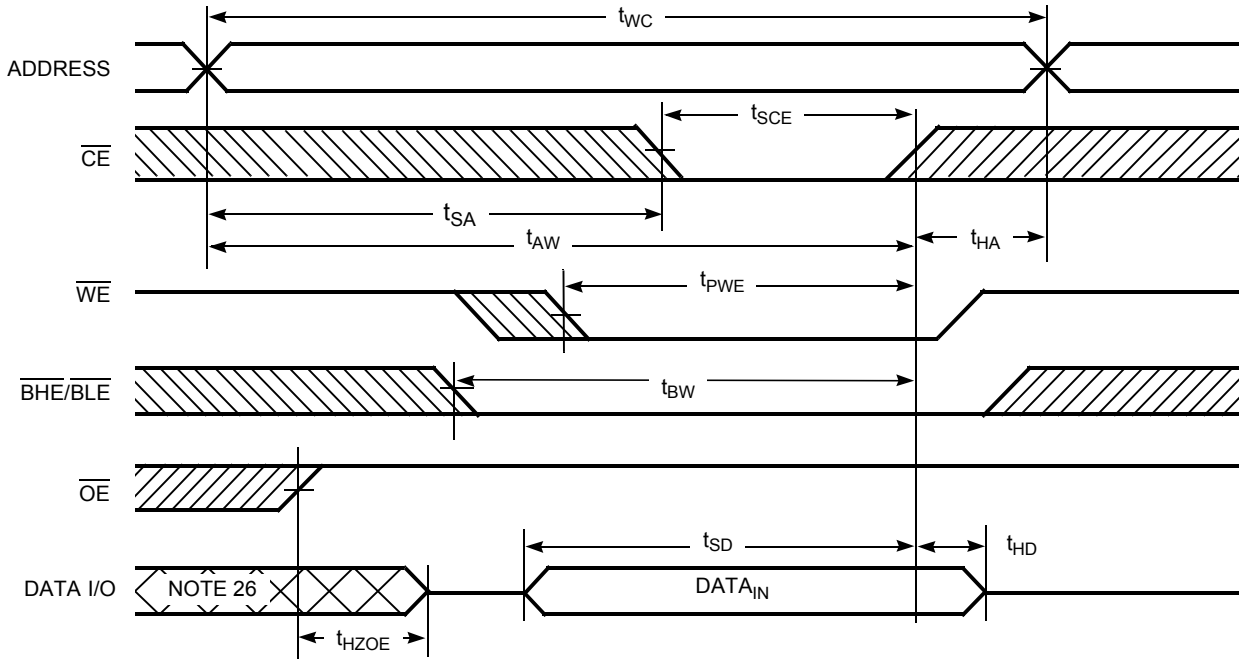


Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [23,24,25]



Notes:
23. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
25. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (WE Controlled and OE LOW) [27]

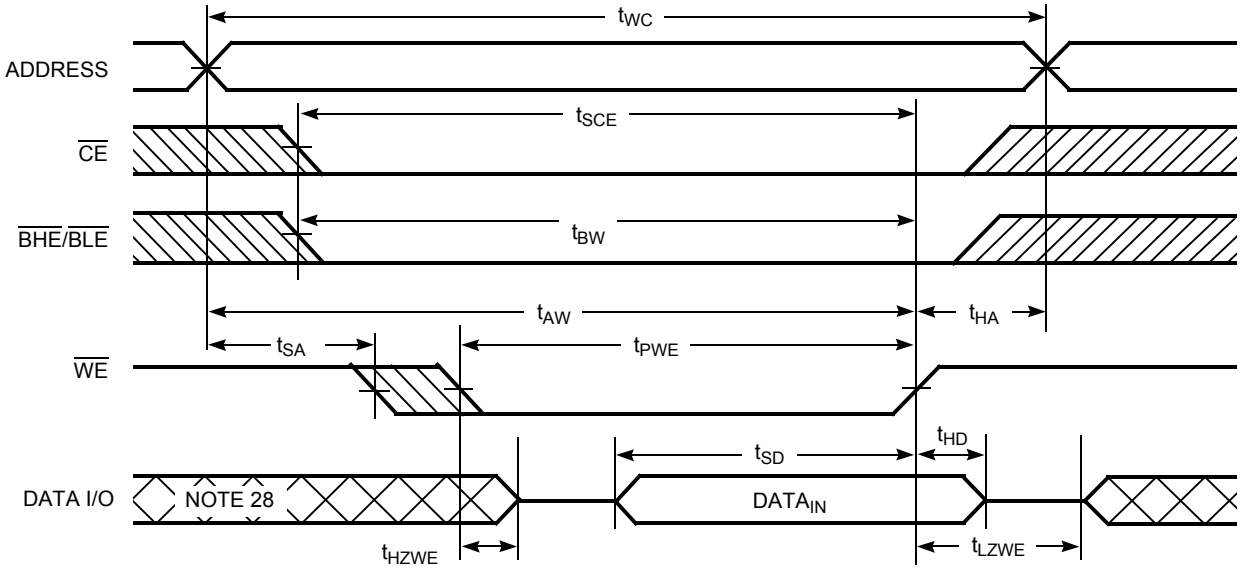
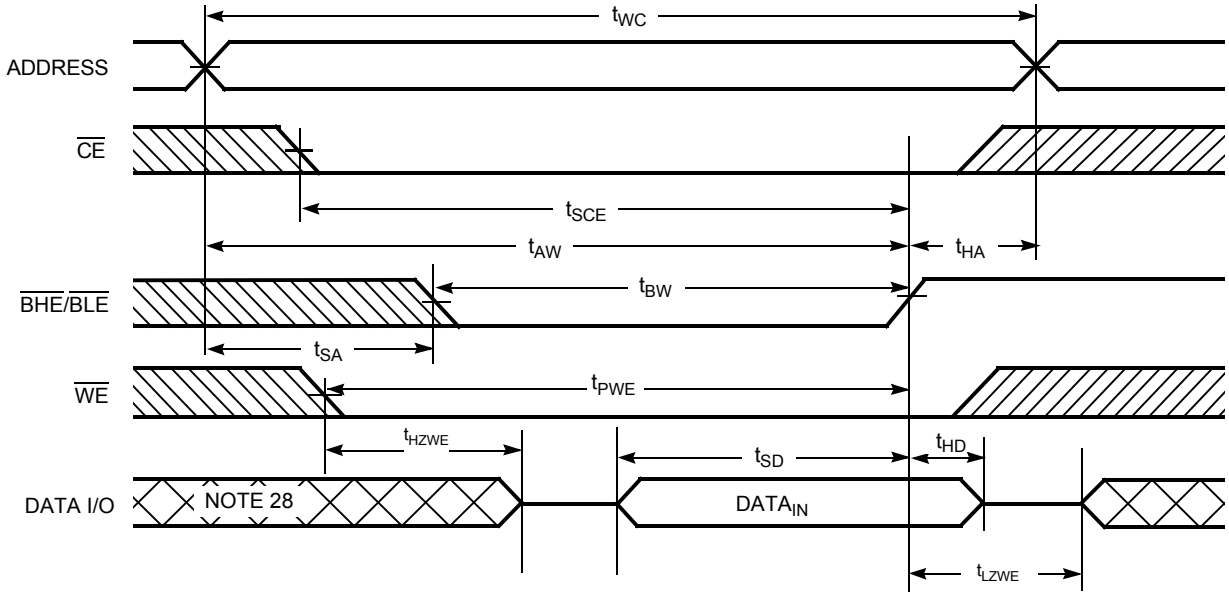


Figure 9. Write Cycle No. 4 (BHE/BLE Controlled and OE LOW) [27]



Notes
27. If CE goes high simultaneously with WE = V_{IH}, the output remains in a high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs or Outputs	Mode	Power
H	X	X	X[29]	X[29]	High-Z	Deselect or power down	Standby (I_{SB})
X[29]	X	X	H	H	High-Z	Deselect or power down	Standby (I_{SB})
L	H	L	L	L	Data out ($I/O_0 – I/O_{15}$)	Read	Active (I_{CC})
L	H	L	H	L	Data out ($I/O_0 – I/O_7$); $I/O_8 – I/O_{15}$ in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out ($I/O_8 – I/O_{15}$); $I/O_0 – I/O_7$ in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in ($I/O_0 – I/O_{15}$)	Write	Active (I_{CC})
L	L	X	H	L	Data in ($I/O_0 – I/O_7$); $I/O_8 – I/O_{15}$ in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data in ($I/O_8 – I/O_{15}$); $I/O_0 – I/O_7$ in High-Z	Write	Active (I_{CC})

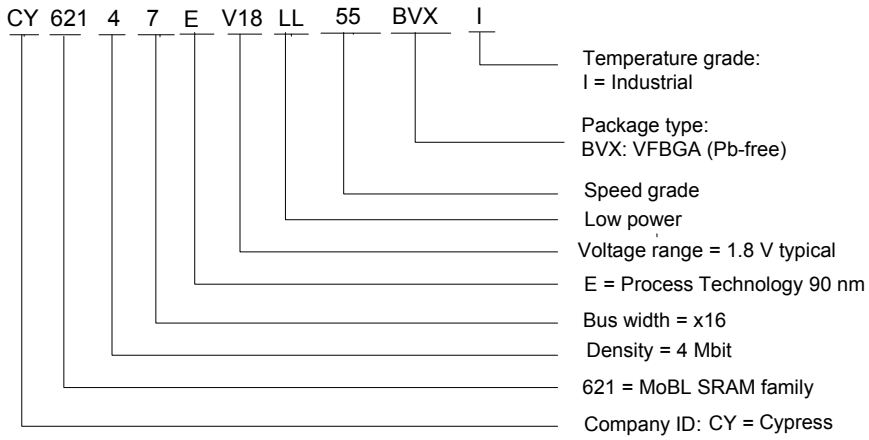
Note
29. The 'X' (Do not care) state for the Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) in the truth table refer to the logic state (either high or low). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62147EV18LL-55BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

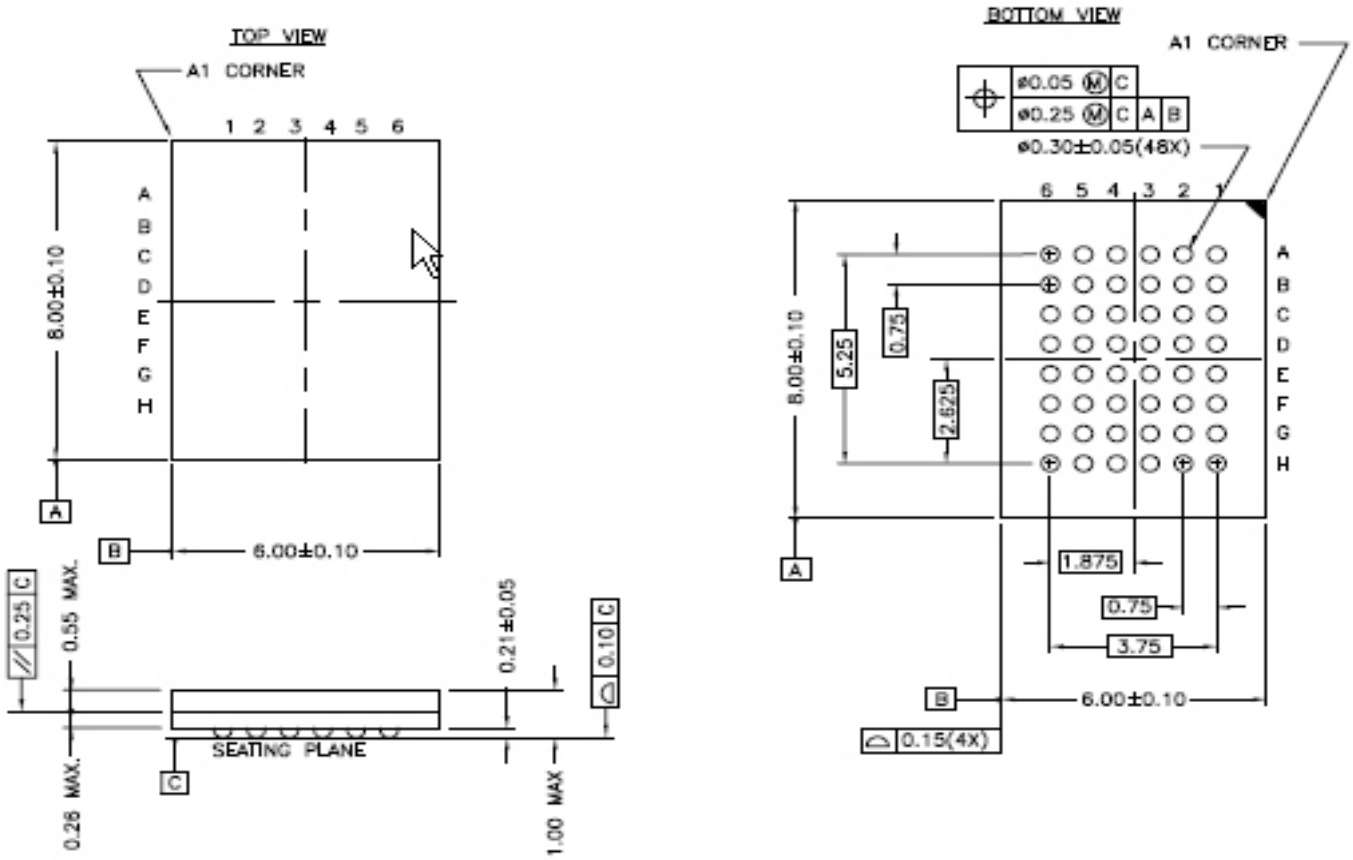
Contact your local Cypress sales representative for availability of other parts.

Ordering Code Definition



Package Diagram

Figure 10. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



51-85150 *F

Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
CMOS	complementary metal oxide semiconductor
$\overline{CE}$	chip enable
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62147EV18 MoBL® 4-Mbit (256K x 16) Static RAM Document Number: 38-05441				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	201580	01/08/04	AJU	New Datasheet
*A	247009	See ECN	SYT	Changed from Advance Information to Preliminary Moved Product Portfolio to Page 2 Changed V_{CCMax} from 2.20 to 2.25 V Changed V_{CC} stabilization time in footnote #8 from 100 μs to 200 μs Removed Footnote #15 (t_{LZBE}) from Previous Revision Changed I_{CCDR} from 2.0 μA to 2.5 μA Changed typo in Data Retention Characteristics (t_R) from 100 μs to t_{RC} ns Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed t_{SCE} and t_{BW} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed t_{HZCE} from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Changed Ordering Information to include Pb-Free Packages
*B	414820	See ECN	ZSD	Changed from Preliminary to Final Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Removed 35 ns Speed Bin Removed “L” version of CY62147EV18 Changed ball E3 from DNU to NC Changed I_{CC}(typ) value from 1.5 mA to 2 mA at f = 1 MHz Changed I_{CC}(max) value from 2 mA to 2.5 mA at f = 1 MHz Changed I_{CC}(typ) value from 12 mA to 15 mA at f = f_{max} Changed I_{SB1} and I_{SB2} Typ values from 0.7 μA to 1 μA and Max values from 2.5 μA to 7 μA Extended undershoot limit to –2 V in footnote #5 Changed I_{CCDR} Max from 2.5 μA to 3 μA Added I_{CCDR} typical value Changed t_{LZOE} from 3 ns to 5 ns Changed t_{LZCE}, t_{LZBE} and t_{LZWE} from 6 ns to 10 ns Changed t_{HZCE} from 22 ns to 18 ns Changed t_{PWE} from 30 ns to 35 ns Changed t_{SD} from 22 ns to 25 ns Updated the package diagram 48-pin VFBGA from *B to *D Updated the ordering information table and replaced Package Name Column with Package Diagram
*C	571786	See ECN	VKN	Replaced 45ns speed bin with 55 ns

Document Title: CY62147EV18 MoBL® 4-Mbit (256K x 16) Static RAM Document Number: 38-05441				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*D	908120	See ECN	VKN	Added footnote #8 related to I_{SB2} and I_{CCDR} Added footnote #13 related AC timing parameters Changed t_{WC} specification from 45 ns to 55 ns Changed t_{SCE}, t_{AW}, t_{PWE}, t_{BW} spec from 35 ns to 40 ns Changed t_{HZWE} specification from 18 ns to 20 ns
*E	1045701	See ECN	VKN	Changed I_{CCDR} specification from 3 μA to 5 μA
*F	1274728	See ECN	VKN/AESA	Changed t_{WC} specification from 55 ns to 45 ns Changed t_{SCE}, t_{AW}, t_{PWE}, t_{BW} specification from 40 ns to 35 ns Changed t_{HZWE} specification from 20 ns to 18 ns
*G	2944332	06/04/2010	VKN	Added Contents Added footnote related to chip enable in Truth Table Updated Package Diagram Added Sales, Solutions, and Legal Information
*H	3047228	10/06/2010	RAME	Added Acronyms and Units of Measure Table Updated Package Diagram from *E to *F version. Updated Data Retention Characteristics and Electrical Characteristics table. Updated and converted all table notes into footnotes.
*I	3302815	07/29/2011	RAME	Ordering Code Definition updated. Updated as per new template. Removed AN1064 reference from the document.

Sales, Solutions, and Legal Information

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