CY7C68300
EZ-USB AT2™
USB 2.0 to ATA/ATAPI Bridge

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 Introduction

The EZ-USB AT2™ implements a fixed function bridge between one USB port and one ATA- or ATAPI-based mass storage device port. This bridge adheres to the *Mass Storage Class Bulk-Only Transport Specification* and is intended for self-powered devices.

The USB port of the EZ-USB AT2 is connected to a host computer directly or via the downstream port of a USB hub. Host software issues commands and data to the EZ-USB AT2 and receives status and data from the EZ-USB AT2 using standard USB protocol.

The ATA/ATAPI port of the EZ-USB AT2 is connected to a mass storage device. A 4-Kbyte buffer maximizes ATA/ATAPI data transfer rates by minimizing losses due to device seek times. The ATA interface supports ATA PIO modes 0, 3, and 4, and Ultra DMA modes 2 and 4.

The device initialization process is configurable, enabling the EZ-USB AT2 to initialize ATA/ATAPI devices without software intervention.

1.1 Features

- **Complies with USB-IF specifications for USB 2.0, the USB *Mass Storage Class*, and the USB *Mass Storage Class Bulk-Only Transport Specification***
- **Operates at high (480-Mbps) or full (12-Mbps) speed**
- **Complies with T13's ATA/ATAPI-6 Draft Specification**
- **Supports 48-bit addressing for large hard drives**
- **Supports PIO modes 0, 3, 4, and UDMA modes 2, 4**
- **Uses one external serial EEPROM containing the USB device serial number, vendor and product identification data, and device configuration data**
- **ATA interface IRQ signal support**
- **Support for ATA/ATAPI devices configured either as master or slave**
- **"ATA-Enable" input signal, which three-states all signals on the ATA interface in order to allow sharing of the bus with another controller (e.g., an IEEE-1394 to ATA bridge chip)**
- **Support for board-level manufacturing test via USB interface**
- **3.3V operation for self-powered devices**
- **56-pin SSOP and 56-pin QFN packages**.
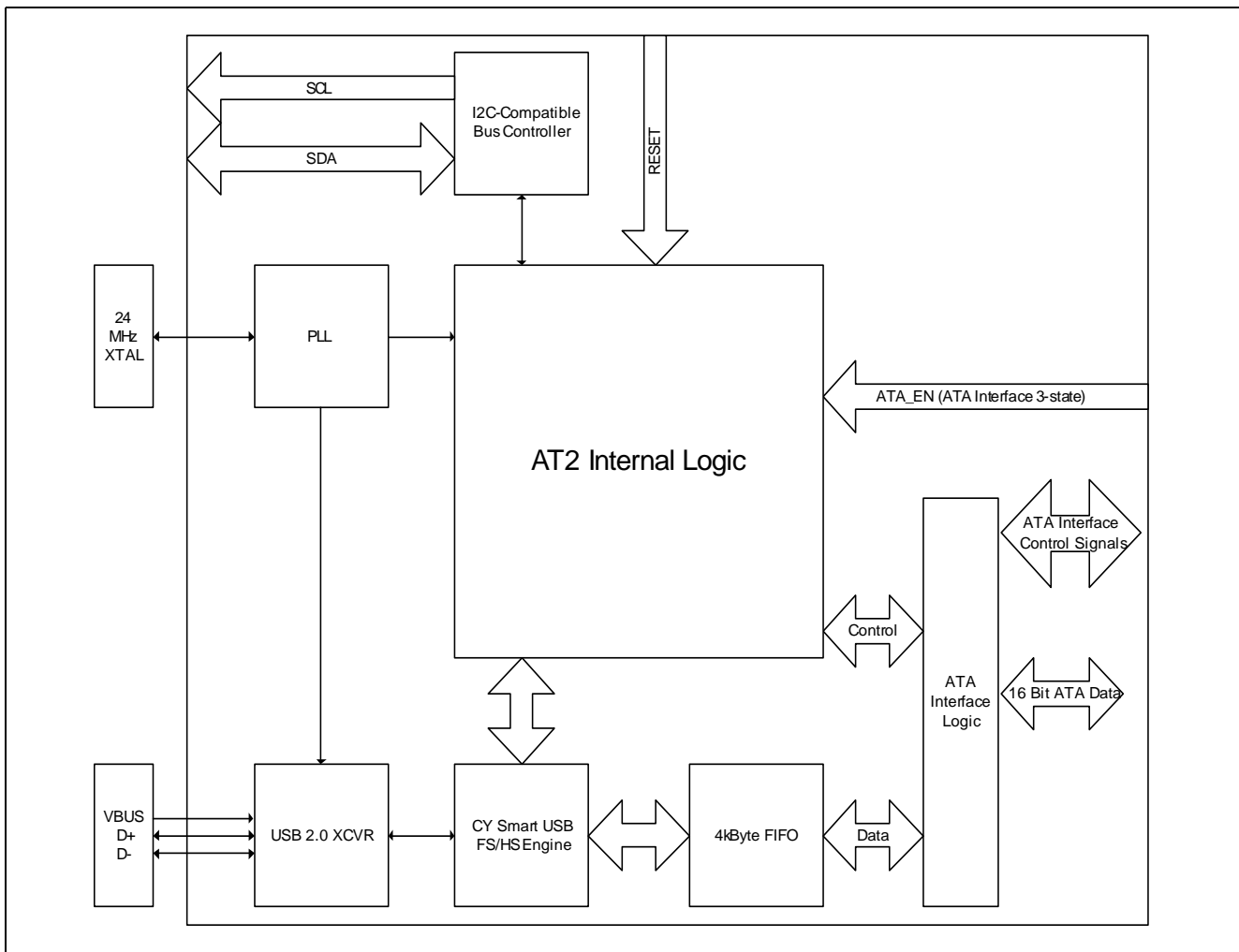
Figure 1-1. Block Diagram

2.0 Pin Assignments

2.1 Pin Diagram

Pin	Signal		Signal	Pin
1	DD13		DD12	56
2	DD14		DD11	55
3	DD15		DD10	54
4	GND		DD9	53
5	NC		DD8	52
6	Vcc		ATA_EN	51
7	GND		Vcc	50
8	IORDY		RESET#	49
9	DMARQ		GND	48
10	AVcc		ARESET#	47
11	XTALOUT		VBUS_PWR_VALID	46
12	XTALIN		CS1#	45
13	AGND	EZ-USB AT2	CS0#	44
14	Vcc	CY7C68300	DA2	43
15	DPLUS		DA1	42
16	DMINUS		DA0	41
17	GND		INTRQ	40
18	Vcc		Vcc	39
19	GND		DMACK#	38
20	PU10K		DIOR#	37
21	RESERVED		DIOW#	36
22	SCL		GND	35
23	SDA		Vcc	34
24	Vcc		GND	33
25	DD0		DD7	32
26	DD1		DD6	31
27	DD2		DD5	30
28	DD3		DD4	29

Figure 2-1. 56-pin SSOP

Pin 1: IORDY
Pin 2: DMARQ
Pin 3: AVCC
Pin 4: XTALOUT
Pin 5: XTALIN
Pin 6: AGND
Pin 7: VCC
Pin 8: DPLUS
Pin 9: DMINUS
Pin 10: GND
Pin 11: VCC
Pin 12: GND
Pin 13: PU10K
Pin 14: RESERVED

Pin 56: GND
Pin 55: VCC
Pin 54: NC
Pin 53: GND
Pin 52: DD15
Pin 51: DD14
Pin 50: DD13
Pin 49: DD12
Pin 48: DD11
Pin 47: DD10
Pin 46: DD9
Pin 45: DD8
Pin 44: ATA_EN
Pin 43: VCC

Pin 15: SCL
Pin 16: SDA
Pin 17: VCC
Pin 18: DD0
Pin 19: DD1
Pin 20: DD2
Pin 21: DD3
Pin 22: DD4
Pin 23: DD5
Pin 24: DD6
Pin 25: DD7
Pin 26: GND
Pin 27: VCC
Pin 28: GND

Pin 42: RESET#
Pin 41: GND
Pin 40: ARESET#
Pin 39: VBUS_PWR_VALID
Pin 38: CS1#
Pin 37: CS0#
Pin 36: DA2
Pin 35: DA1
Pin 34: DA0
Pin 33: INTRQ
Pin 32: VCC
Pin 31: DMACK#
Pin 30: DIOR#
Pin 29: DIOW#

EZ-USB AT2
CY7C68300
56-pin QFN

Figure 2-2. 56-pin QFN

2.2 Pin Descriptions

SSOP Pin	QFN Pin	Pin Name	Pin Type	Default State at Start-up	Pin Description
1	50	DD13	I/O[1]	Hi-Z	**ATA Data bit 13**.
2	51	DD14	I/O[1]	Hi-Z	**ATA Data bit 14**.
3	52	DD15	I/O[1]	Hi-Z	**ATA Data bit 15**.
4	53	GND	GND		**Ground**.
5	54	NC		Hi-Z	**Reserved**. This pin should remain a no-connect.
6	55	V_{CC}	PWR		**V_{CC}**. Connect to 3.3V power source.
7	56	GND	GND		**Ground**.
8	1	IORDY	I[1]	I	**ATA Control**.
9	2	DMARQ	I[1]	I	**ATA Control**.
10	3	AV_{CC}	PWR		**Analog V_{CC}**. Connect the V_{CC} through the shortest path possible.
11	4	XTALOUT	Xtal	Xtal	**24-MHz Crystal Output** (see subsection 2.3.3).
12	5	XTALIN	Xtal	Xtal	**24-MHz Crystal Input** (see subsection 2.3.3).
13	6	AGND	GND		**Analog Ground**. Connect to ground with as short a path as possible.
14	7	V_{CC}	PWR		**V_{CC}**. Connect to 3.3V power source.
15	8	DPLUS	I/O	Pulled high at Reset. When the firmware starts, the pullup is controlled by pin 46(SSOP)/39(QFN). When VBUS_PWR _VALID is high, the line is pulled up. VBUS_PWR _VALID is polled at start-up and then every 20 ms.	**USB D+ Signal** (see subsection 2.3.1).
16	9	DMINUS	I/O	Hi-Z	**USB D- Signal** (see subsection 2.3.1).
17	10	GND	GND		**Ground**.
18	11	V_{CC}	PWR		**V_{CC}**. Connect to 3.3V power source.
19	12	GND	GND		**Ground**.
20	13	PU10K		Hi-Z	**Tied to 10k ± 5% pull-up resistor**.
21	14	RESERVED			**Reserved**. Tie to GND.
22	15	SCL	O	SCL/SDA will be active for several ms at start-up. Then driven high.	**Clock signal for I²C-compatible interface** (see 2.3.2).
23	16	SDA	I/O		**Data signal for I²C-compatible interface** (see 2.3.2).
24	17	V_{CC}	PWR		**V_{CC}**. Connect to 3.3V power source.
25	18	DD0	I/O	Hi-Z	**ATA Data bit 0**.
26	19	DD1	I/O	Hi-Z	**ATA Data bit 1**.
27	20	DD2	I/O	Hi-Z	**ATA Data bit 2**.
28	21	DD3	I/O	Hi-Z	**ATA Data bit 3**.
29	22	DD4	I/O	Hi-Z	**ATA Data bit 4**.
30	23	DD5	I/O	Hi-Z	**ATA Data bit 5**.
31	24	DD6	I/O	Hi-Z	**ATA Data bit 6**.
32	25	DD7	I/O	Hi-Z	**ATA Data bit 7**.
33	26	GND	GND		**Ground**.
34	27	V_{CC}	PWR		**V_{CC}**. Connect to 3.3V power source.
35	28	GND	GND		**Ground**.

Note:
1. ATA interface pins are not active when ATA_EN is not asserted.

2.2 Pin Descriptions (continued)

SSOP Pin	QFN Pin	Pin Name	Pin Type	Default State at Start-up	Pin Description
36	29	DIOW#[2]	O/Z[1]	Driven high (CMOS)	**ATA Control**.
37	30	DIOR#	O/Z[1]	Driven high (CMOS)	**ATA Control**.
38	31	DMACK#	O/Z[1]	Driven high (CMOS)	**ATA Control**.
39	32	V_{CC}	PWR		**V_{CC}**. Connect to 3.3V power source.
40	33	INTRQ	I[1]	Input	**IDE ATA Interrupt request**.
41	34	DA0	O/Z[1]	Driven high after 2 ms delay	**ATA Address**.
42	35	DA1	O/Z[1]	Driven high after 2 ms delay	**ATA Address**.
43	36	DA2	O/Z[1]	Driven high after 2 ms delay	**ATA Address**.
44	37	CS0#	O/Z[1]	Driven high after 2 ms delay	**ATA Chip Select**.
45	38	CS1#	O/Z[1]	Driven high after 2 ms delay	**ATA Chip Select**.
46	39	VBUS_PWR_VALID	I	Input	**VBUS detection**. Indicates to the EZ-USB AT2 that VBUS power is present.
47	40	ARESET#	O/Z[1]		**ATA Reset**.
48	41	GND	GND		**Ground**.
49	42	RESET#	I		**Active LOW Reset**. Resets the entire chip. This pin is normally tied to VCC through a 100K resistor, and to GND through a 0.1-µF capacitor, supplying a 10-ms reset.
50	43	V_{CC}	PWR		**V_{CC}**. Connect to 3.3V power source.
51	44	ATA_EN	I	Input – If AT2 is not in mfg mode, polled every 20 ms after start-up. If LOW, SSOP: pins 36–38, 41–45 and 47 are three-stated. QFN: pins 29–31, 34–38 and 40 are three-stated.	**Active HIGH**. ATA interface enable. Allows ATA bus sharing with other host devices. Setting ATA_EN=1 enables the ATA interface for normal operation. Disabling ATA_EN three-states (High-Z) the ATA interface and halts the ATA interface state machine logic.
52	45	DD8	I/O[1]	Hi-Z	**ATA Data bit 8**.
53	46	DD9	I/O[1]	Hi-Z	**ATA Data bit 9**.
54	47	DD10	I/O[1]	Hi-Z	**ATA Data bit 10**.
55	48	DD11	I/O[1]	Hi-Z	**ATA Data bit 11**.
56	49	DD12	I/O[1]	Hi-Z	**ATA Data bit 12**.

2.3 Additional Pin Descriptions

2.3.1 DPLUS, DMINUS

DPLUS and DMINUS are the USB signaling pins, and they should be tied to the D+ and D– pins of the USB connector. Because they operate at high frequencies, the USB signals require special consideration when designing the layout of the PCB.

2.3.2 SCL, SDA

The clock and data pins for the I^{2}C-compatible port should be connected to your configuration EEPROM and to V_{CC} through 2.2k resistors.

2.3.3 XTALIN, XTALOUT

The EZ-USB AT2 requires a 24-MHz signal to derive internal timing. Typically a 24-MHz parallel-resonant fundamental mode crystal is used, but a 24-MHz square wave from another source can also be used. If a crystal is used, connect the pins to XTALIN and XTALOUT, and also through 20-pF capacitors to GND. If an alternate clock source is used, apply it to XTALIN and leave XTALOUT open.

Note:
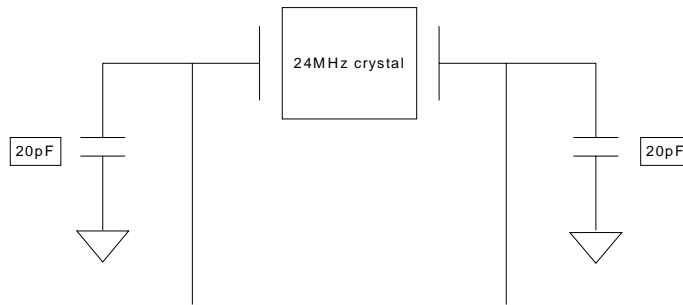 2.   A # sign after the signal name indicates it is an active LOW signal.

Figure 2-3. XTALIN, XTALOUT Diagram

2.3.4   ATA_EN

ATA_EN allows bus sharing with other host devices. Setting ATA_EN = 1 enables the ATA interface for normal operation. Setting ATA_EN = 0 disables (High-Z) the ATA interface pins and removes the EZ-USB AT2 from the USB. The ATA_EN pin is sampled at a rate of 60 times per second by the EZ-USB AT2 internal logic. This pin should be set to a HIGH at start-up. Upon a HIGH to LOW transition all EZ-USB AT2 ATA signals are tri-stated, USB is disconnected, and the EZ-USB AT2 enters an idle state until an active Reset is received, or the ATA_EN pin transitions back to a HIGH state. Upon sensing the LOW to HIGH transition the EZ-USB AT2 will return to the post Reset operational state, and will reconnect to USB. Note that disabling the ATA bus with the ATA_EN pin during the middle of a data transfer will result in data loss and can cause the operating system on the Host computer to crash.

2.3.5   ATA Interface Pins

Design practices as outlined in the ATA/ATAPI-6 Specification for signal integrity should be followed with systems that utilize a ribbon cable interconnect between the EZ-USB AT2's ATA interface and the attached ATA/ATAPI device, especially if Ultra DMA Mode is utilized.

2.3.6   VBUS_PWR_VALID

VBUS_PWR_VALID indicates to the EZ-USB AT2 that power is present on VBUS.

2.3.7   RESET#

Asserting RESET# for 10 ms will reset the entire chip. This pin is normally tied to V_{CC} through a 100k resistor, and to GND through a 0.1-µF capacitor.
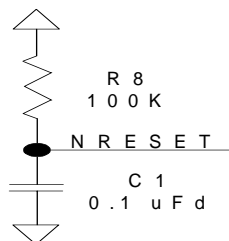
Figure 2-4. Typical Reset Circuit

3.0   Applications

The EZ-USB AT2 is a high-speed USB 2.0 peripheral device that connects ATA or ATAPI storage devices to a USB host using the USB *Mass Storage Class* protocol.

3.1   Additional Resources

• CY4615 EZ-USB AT2 Reference Design Kit

• USB Specification version 2.0

• ATA Specification T13/1410D Rev 3B

• USB *Mass Storage Class Bulk Only Transport Specification*, http://www.usb.org/developers/data/devclass/ usbmassbulk_10.pdf.

4.0 Functional Overview

4.1 USB Signaling Speed

EZ-USB AT2 operates at two of the three rates defined in the USB Specification Revision 2.0 dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbits/sec
- High speed, with a signaling bit rate of 480 Mbits/sec.

EZ-USB AT2 does not support the low-speed signaling rate of 1.5 Mbits/sec.

4.2 ATA Interface

The ATA/ATAPI port on the EZ-USB AT2 is compliant with the Information Technology AT Attachment with Packet Interface 6 (ATA/ATAPI-6) Specification, T13/1410D Rev 3B. The EZ-USB AT2 supports both ATAPI packet commands over USB. Additionally, the EZ-USB AT2 translates ATAPI SFF-8070i commands to ATA commands for seamless integration of ATA devices with generic Mass Storage Class BOT drivers.

5.0 Enumeration

During the power-up sequence, internal logic checks the I²C-compatible port for an EEPROM whose first two bytes are both 0x4D. If a valid signature is found, the EZ-USB AT2 uses the values stored in the EEPROM to configure the USB descriptors for normal operation. If an invalid EEPROM signature is read, or if no EEPROM is detected, the EZ-USB AT2 defaults into Board Manufacturing Test Mode. The two modes of operation are described in subsections 5.1 and 5.2, below.

5.1 Board Manufacturing Test Mode

In Board Manufacturing Test Mode, the chip behaves as a USB 2.0 device but the ATA/ATAPI interface is not active. The EZ-USB AT2 allows for reading and writing an EEPROM and for board level testing through vendor specific ATAPI commands utilizing the CBW Command Block as described in the USB *Mass Storage Class Bulk-Only Transport Specification*. There is a vendor-specific ATAPI command for the EEPROM access (CfgCB) and one for the board level testing (MfgCB).

5.1.1 CfgCB

The cfg_load and cfg_read vendor-specific commands are passed down through the bulk pipe in the CBWCB portion of the CBW. The format of this CfgCB is shown below. Byte 0 will be a vendor-specific command designator whose value is configurable and set in the configuration data (EEPROM address 0x04). Byte 1 must be set to 0x26 to identify CfgCB. Byte 2 is reserved and must be set to zero. Byte 3 is used to determine the memory source to write/read. For the EZ-USB AT2, this byte must be set to 0x02, meaning the EEPROM. Bytes 4 and 5 will be used to determine the start address. For the EZ-USB AT2, this must always be 0x0000. Bytes 6 through 15 are reserved and should be set to zero.

The data transferred to the EEPROM must be in the format specified in *Table 5-6* of this data sheet. Maximum data transfer size is 255 bytes.

The data transfer length is determined by the CBW Data Transfer Length specified in bytes 8 through 11 (dCBWDataTransferLength) of the CBW. The type/direction of the command will be determined by the direction bit specified in byte 12, bit 7 (bmCBWFlags) of the CBW.

Table 5-1. Command Block Wrapper

	7	6	5	4	3	2	1	0
0–3	DCBWSignature							
4–7	dCBWTag							
8–11 (08h-0Bh)	dCBWDataTransferLength							
12 (0Ch)	bwCBWFLAGS							
	Dir	Obsolete	Reserved (0)					
13 (0Dh)	Reserved (0)				bCBWLUN			
14 (0Eh)	Reserved (0)				bCBWCBLength			
15-30 (0Fh1Eh)	CBWCB (CfgCB or MfgCB)							

Table 5-2. Example CfgCB

CfgCB Byte Descriptions	Bits							
	7	6	5	4	3	2	1	0
0 bVSCBSignature (set in configuration bytes)	0	0	1	0	0	1	0	0

Table 5-2. Example CfgCB (continued)

CfgCB Byte Descriptions	Bits							
	7	6	5	4	3	2	1	0
1 bVSCBSubCommand (must be 0x26)	0	0	1	0	0	1	1	0
2 Reserved (must be set to zero)	0	0	0	0	0	0	0	0
3 Data Source (must be set to 0x02)	0	0	0	0	0	0	1	0
4 Start Address (LSB) (must be set to zero)	0	0	0	0	0	0	0	0
5 Start Address (MSB) (must be set to zero)	0	0	0	0	0	0	0	0
6–15 Reserved (must be set to zero)	0	0	0	0	0	0	0	0

5.1.2   MfgCB

The mfg_load and mfg_read vendor-specific commands will be passed down through the bulk pipe in the CBWCB portion of the CBW. The format of this MFGCB is shown below. Byte 0 is a vendor-specific command designator whose value is configurable and set in the configuration data. Byte 1 must be 0x27 to identify MfgCB. Byte 2–15 are reserved and must be set to zero.

The data transfer length will be determined by the CBW Data Transfer Length specified in bytes 8 through 11 (dCBWDataTransferLength) of the CBW. The type/direction of the command is determined by the direction bit specified in byte 12, bit 7 (bmCBWFlags) of the CBW.

Table 5-3. Example MfgCB

MfgCB Byte Description	Bits							
0 bVSCBSignature (set in configuration bytes)	0	0	1	0	0	1	0	0
1 bVSCBSubCommand (hardcoded 0x27)	0	0	1	0	0	1	1	1
2–15 Reserved (must be zero)	0	0	0	0	0	0	0	0

5.1.2.1   Mfg_load

During a mfg_load, the EZ-USB AT2 goes into Manufacturing Test Mode. Manufacturing Test Mode is provided as a means to implement board or system level interconnect tests. During Manufacturing Test Mode operation, all outputs not directly associated with USB operation are controllable. Normal control of the output pins are disabled. Control of the select EZ-USB AT2 IO pins and their three-state controls are mapped to the ATAPI data packet associated with this request. (See the following table for explanation of the required mfg_load data format.) This requires a write of seven bytes. To exit Manufacturing Test Mode, a hard reset (#RESET) is required.

Table 5-4. Mfg_load Data Format

Byte	Bit(s)	Test/Three-state Control Function
0	0	Reserved
0	3:1	DA[2:0]
0	5:4	CS#[1:0]
0	6	Reserved
0	7	ARESET#
1	0	NDIOW
1	1	NDIOR
1	2	NDMACK
1	3:6	Reserved
1	7	DD[15:0] Three-state (0 = three-state DD pins, 1 = enable DD pins).
2	7:0	DD[7:0]
3	7:0	DD[15:8]
4	7:0	Reserved
5	7:0	Reserved
6	7:0	Reserved

5.1.2.2 Mfg_read

This USB request returns a "snapshot in time" of select EZ-USB AT2 input pins. The input pin states are bit-wise mapped to the ATAPI data associated with this request. EZ-USB AT2 input pins not directly associated with USB operation can be sampled at any time during Manufacturing Test Mode operation. See the following table for an explanation of the mfg_read data format. The data length shall always be eight bytes.

Table 5-5. Mfg_read Data Format

Byte	Bit(s)	Test/Three-state Control Function
0	0	INTRQ
0	5:1	Reserved. This data should be ignored.
0	6	VBUS_PWR_VALID
0	7	ARESET# (output value only)
1	2:0	Reserved. This data should be ignored.
1	3	IORDY
1	4	DMARQ
1	5	ATA_EN
1	6	Reserved. This data should be ignored.
1	7	DD[15:0] Tri-state
2	7:0	DD[7:0]
3	7:0	DD[15:8]
4	7:0	Reserved. This data should be ignored.
5	7:0	Reserved. This data should be ignored.
6	7:0	Reserved. This data should be ignored.
7	7:0	Reserved. This data should be ignored.

5.2   Normal Operation Mode

In Normal Operation Mode, the chip behaves as a USB 2.0 to ATA/ATAPI bridge. This includes all typical USB device states (powered, configured, etc.). The USB descriptors are returned according to the values stored in the external EEPROM. An external EEPROM is required for Mass Storage Class Bulk-Only Transport compliance, since a unique serial number is required for each device. Also, Cypress requires customers to use their own Vendor and Product IDs for final products.

5.3   EEPROM Organization

The contents of the 256-byte (2048-bit) two-wire serial EEPROM are arranged as follows. The column labeled "Required Contents" contains the values that must be used for proper operation of the EZ-USB AT2. The column labeled "Suggested Contents" contains suggested values for the bytes that are defined by the manufacturer. Some values, such as the Vendor ID and device and device serial number, must be customized to meet USB compliance. See subsection 5.1 for details on how to use vendor-specific ATAPI commands to read and program the EEPROM. The serial EEPROM must be hard-wired to address 0x04. This means that A0 and A1 of the serial EEPROM must be tied to ground and that A2 must be tied to 3.3V.

Table 5-6. EEPROM Organization

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
Configuration				
0x00	I^{2}C-compatible memory device signature (LSB)	LSB I^{2}C-compatible memory device signature byte.	0x4D	
0x01	I^{2}C-compatible memory device signature (MSB)	MSB I^{2}C-compatible memory device signature byte.	0x4D	
0x02	APM Value	ATA Device Automatic Power Management Value. If an attached ATA device supports APM and this field contains other than 0x00, the EZ-USB AT2 will issue a SET_FEATURES command to Enable APM with this value during the drive initialization process. Setting APM Value to 0x00 disables this functionality. This value is ignored with ATAPI devices.		0x00
0x03	ATA Initialization Timeout	Time in 128-ms granularity before the EZ-USB AT2 stops polling the ALT STAT register for reset complete and restarts the reset process (0x80 = 16.4 seconds).		0x80
0x04	ATA Command Designator	Value in the first byte of the CBW CB field that designates that the CB is t o be decoded as vendor specific ATA commands instead of the ATAPI command block. See section 4.0 for more detail on how this byte is used.		0x24
0x05	Reserved	Bits(7:4) Set to 0		0x07
	BUSY Bit Delay	Bit (3) Enables a delay of up to 120 ms at each read of the DRQ bit where the device data length does not match the host data length. This allows the EZ-USB AT2 to work with most devices that incorrectly clear the BUSY bit before a valid status is present.		
	Short Packet Before Stall	Bit (2) Determines if a short packet is sent prior to the STALL of an IN endpoint. The USB *Mass Storage Class Bulk-Only Specification* allows a device to send a short or zero-length IN packet prior to returning a STALL handshake for certain cases. Certain host controller drivers may require a short packet prior to STALL. 1 = Force a short packet before STALL. 0 = Don't force a short packet before STALL.		
	SRST Enable	Bit (1) Determines if the EZ-USB AT2 is to do a SRST reset during drive initialization.[3] 1 = Perform SRST during initialization. 0 = Don't perform SRST during initialization.		
	Skip Pin Reset	Bit (0) Skip ATA_NRESET assertion.[4] 0 = Allow ARESET# assertion for all resets. 1 = Disable ARESET# assertion except for power-on reset cycles.		

Notes:
3. At least one reset must be enabled. Do not set SRST to 0 and Skip Pin Reset to 1at the same time.
4. SRST Enable must be set in conjunction with Skip Pin Reset. Setting this bit causes the EZ-USB AT2 to bypass ARESET# during initialization. All reset events except a power-on reset utilize SRST as the drive mechanism.

Table 5-6. EEPROM Organization (continued)

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
0x06	ATA UDMA Enable	Bit (7) Enable Ultra DMA data transfer support for ATAPI devices. If enabled, and if the ATAPI device reports UDMA support for the indicated modes, the EZ-USB AT2 will utilize UDMA data transfers at the highest negotiated rate possible. 0 = Disable ATA device UDMA support. 1 = Enable ATA device UDMA support.		0xD4
	ATAPI UDMA Enable	Bit (6) Enable Ultra DMA data transfer support for ATAPI devices. If enabled, and if the ATAPI device reports UDMA support for the indicated modes, the EZ-USB AT2 will utilize UDMA data transfers at the highest negotiated rate possible. 0 = Disable ATAPI device UDMA support. 1 = Enable ATAPI device UDMA support.		
	UDMA Modes	Bit (5:0) These bits select which UDMA modes, if supported, are enabled. Setting to 1 enables. Multiple bits may be set. The EZ-USB AT2 will operate in the highest enabled UDMA mode supported by the device. The EZ-USB AT2 supports UDMA modes 2 and 4 only. Bit Descriptions 5 Reserved. Must be set to 0. 4 Enable UDMA mode 4. 3 Reserved. Must be set to 0. 2 Enable UDMA mode 2. 1 Reserved. Must be set to 0. 0 Reserved. Must be set to 0.		
0x07	Reserved PIO Modes	Bits(7:2) Bits(1:0) These bits select which PIO modes, if supported, are enabled. Setting to 1 enables. Multiple bits may be set. The EZ-USB AT2 will operate in the highest enabled PIO mode supported by the device. The EZ-USB AT2 supports PIO modes 0, 3, and 4 only. PIO mode 0 is always enabled by internal logic. Bit Descriptions 1 Enable PIO mode 4. 0 Enable PIO mode 3.		0x03
0x08	Reserved	Must be set to 0x00.	0x00	
0x09	Reserved	Must be set to 0x00.	0x00	
0x0A	Reserved	Must be set to 0x00.	0x00	
0x0B	Reserved	Must be set to 0x00.	0x00	
0x0C	Reserved	Must be set to 0x00.	0x00	
0x0D	Reserved	Must be set to 0x00.	0x00	
0x0E	Reserved	Must be set to 0x00.	0x00	
0x0F	Reserved	Must be set to 0x00.	0x00	
Device Descriptor				
0x10	bLength	Length of device descriptor in bytes.	0x12	
0x11	bDescriptor Type	Descriptor type.	0x01	
0x12	bcdUSB (LSB)	USB Specification release number in BCD.	0x00	
0x13	bcdUSB (MSB)		0x02	
0x14	bDeviceClass	Device class.	0x00	
0x15	bDeviceSubClass	Device subclass.	0x00	

Table 5-6. EEPROM Organization (continued)

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
0x16	bDeviceProtocol	Device protocol.	0x00	
0x17	bMaxPacketSize0	USB packet size supported for default pipe.	0x40	
0x18	idVendor (LSB)	Vendor ID. Cypress's Vendor ID may only be used for evaluation purposes, and not in released products.		0xB4
0x19	idVendor (MSB)			0x04
0x1A	idProduct (LSB)	Product ID.		0x30
0x1B	idProduct (MSB)			0x68
0x1C	bcdDevice (LSB)	Device release number in BCD LSB (product release number).		0x01
0x1D	bcdDevice (MSB)	Device release number in BCD MSB (silicon release number).		0x00
0x1E	iManufacturer	Index to manufacturer string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x38
0x1F	iProduct	Index to product string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x4E
0x20	iSerialNumber	Index to serial number string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist. The USB *Mass Storage Class Bulk-Only Transport Specification* requires a unique serial number (in upper case, hexidecimal characters) for each device.		0x64
0x21	bNumConfigurations	Number of configurations supported.	0x01	
Device Qualifier				
0x22	bLength	Length of device descriptor in bytes.	0x0A	
0x23	bDescriptor	Type Descriptor type.	0x06	
0x24	bcdUSB (LSB)	USB Specification release number in BCD.	0x00	
0x25	bcdUSB (MSB)	USB Specification release number in BCD.	0x02	
0x26	bDeviceClass	Device class.	0x00	
0x27	bDeviceSubClass	Device subclass.	0x00	
0x28	bDeviceProtocol	Device protocol.	0x00	
0x29	bMaxPacketSize0	USB packet size supported for default pipe.	0x40	
0x2A	bNumConfigurations	Number of configurations supported.	0x01	
0x2B	bReserved	Reserved for future use. Must be set to zero.	0x00	
High-speed Configuration Descriptor				
0x2C	bLength	Length of configuration descriptor in bytes.	0x09	
0x2D	bDescriptorType	Descriptor type.	0x02	
0x2E	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x20	
0x2F	bTotalLength (MSB)		0x00	
0x30	bNumInterfaces	Number of interfaces supported.	0x01	
0x31	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x01.	0x01	
0x32	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x00

Table 5-6. EEPROM Organization (continued)

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
0x33	bmAttributes	Device attributes for this configuration. Bit Descriptions 7 Reserved. Must be set to 1. 6 Self-powered. Must be set to 1. 5 Remote wake-up. Must be set to 0. 4-0 Reserved. Must be set to 0.	0xC0	
0x34	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2(i.e., 0x31 = 98 mA, 0xF9 = 498 mA). 0x00 reported for self-powered devices.		0x00
High-speed Interface and Endpoint Descriptors				
Interface Descriptor				
0x35	bLength	Length of interface descriptor in bytes.	0x09	
0x36	bDescriptorType	Descriptor type.	0x04	
0x37	bInterfaceNumber	Interface number.	0x00	
0x38	bAlternateSetting	Alternate setting.	0x00	
0x39	bNumEndpoints	Number of endpoints.	0x02	
0x3A	bInterfaceClass	Interface class.	0x08	
0x3B	bInterfaceSubClass	Interface subclass.		0x06
0x3C	bInterfaceProtocol	Interface protocol.	0x50	
0x3D	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x00
USB Bulk Out Endpoint				
0x3E	bLength	Length of this descriptor in bytes.	0x07	
0x3F	bDescriptorType	Endpoint descriptor type.	0x05	
0x40	bEndpointAddress	This is an Out endpoint, endpoint number 2.	0x02	
0x41	bmAttributes	This is a bulk endpoint.	0x02	
0x42	wMaxPacketSize (LSB)	Max data transfer size.	0x00	
0x43	wMaxPacketSize (MSB)		0x02	
0x44	bInterval	HS interval for polling (max NAK rate).	0x00	
USB Bulk In Endpoint				
0x45	bLength	Length of this descriptor in bytes.	0x07	
0x46	bDescriptorType	Endpoint descriptor type.	0x05	
0x47	bEndpointAddress	This is an In endpoint, endpoint number 8.	0x88	
0x48	bmAttributes	This is a bulk endpoint.	0x02	
0x49	wMaxPacketSize (LSB)	Max data transfer size.	0x00	
0x4A	wMaxPacketSize (MSB)		0x02	
0x4B	bInterval	HS interval for polling (max NAK rate).	0x00	
Full-speed Configuration Descriptor				
0x4C	bLength	Length of configuration descriptor in bytes.	0x09	
0x4D	bDescriptorType	Descriptor type.	0x02	
0x4E	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x20	
0x4F	bTotalLength (MSB)		0x00	
0x50	bNumInterfaces	Number of interfaces supported.	0x01	
0x51	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration.	0x01	

Table 5-6. EEPROM Organization (continued)

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
0x52	iConfiguration	Index to configuration string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.		0x00
0x53	bmAttributes	Device attributes for this configuration. Bit Descriptions 7 Reserved. Must be set to 1. 6 Self-powered. Must be set to 1. 5 Remote wake-up. Must be set to 0. 4–0 Reserved. Must be set to 0.	0xC0	
0x54	bMaxPower	Maximum power consumption for the second configuration. Units used are mA*2 (i.e., 0x31 = 98 mA, 0xF9 = 498 mA).		0x00
Full-speed Interface and Endpoint Descriptors				
Interface Descriptor				
0x55	bLength	Length of interface descriptor in bytes.	0x09	
0x56	bDescriptorType	Descriptor type.	0x04	
0x57	bInterfaceNumber	Interface number.	0x00	
0x58	bAlternateSettings	Alternate settings.	0x00	
0x59	bNumEndpoints	Number of endpoints.	0x02	
0x5A	bInterfaceClass	Interface class.	0x08	
0x5B	bInterfaceSubClass	Interface subclass.		0x06
0x5C	bInterfaceProtocol	Interface protocol.	0x50	
0x5D	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.	0x00	
USB Bulk Out Endpoint				
0x5E	bLength	Length of this descriptor in bytes.	0x07	
0x5F	bDescriptorType	Endpoint descriptor type.	0x05	
0x60	bEndpointAddress	This is an Out endpoint, endpoint number 2.	0x02	
0x61	bmAttributes	This is a bulk endpoint.	0x02	
0x62	wMaxPacketSize (LSB)	Max data transfer size.	0x40	
0x63	wMaxPacketSize (MSB)		0x00	
0x64	bInterval	Does not apply to FS bulk endpoints. Must be set to 0.	0x00	
USB Bulk In Endpoint				
0x65	bLength	Length of this descriptor in bytes.	0x07	
0x66	bDescriptorType	Endpoint descriptor type.	0x05	
0x67	bEndpointAddress	This is an In endpoint, endpoint number 8.	0x88	
0x68	bmAttributes	This is a bulk endpoint.	0x02	
0x69	wMaxPacketSize (LSB)	Max data transfer size.	0x40	
0x6A	wMaxPacketSize (MSB)		0x00	
0x6B	bInterval	Does not apply to FS bulk endpoints. Must be set to 0.	0x00	
String Descriptor Examples (**Note**: The values in these strings are given as examples only and should not be used in final products. Designers are encouraged to modify the string values to reflect the final product, since they are what users will see with their operating systems.)				
USB String Descriptor–Index 0 (LANGID)				
0x6C	bLength	LANGID string descriptor length in bytes.	0x04	
0x6D	bDescriptorType	Descriptor type.	0x03	

Table 5-6. EEPROM Organization (continued)

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
0x6E	LANGID (LSB)	Language supported. Note: See http://www.usb.org for LANGID documentation (the code for English is 0x0409).		0x09
0x6F	LANGID (MSB)			0x04
USB String Descriptor–Manufacturer				
0x70	bLength	String descriptor length in bytes (including bLength).		0x2C
0x71	bDescriptorType	Descriptor type.	0x03	
0x72	bString	Unicode character.		"C" 0x43
0x73	bString	("NUL")		0x00
0x74	bString	Unicode character.		"y" 0x79
0x75	bString	("NUL")		0x00
0x76	bString	Unicode character.		"p" 0x70
0x77	bString	("NUL")		0x00
0x78	bString	Unicode character.		"r" 0x72
0x79	bString	("NUL")		0x00
0x7A	bString	Unicode character.		"e" 0x65
0x7B	bString	("NUL")		0x00
0x7C	bString	Unicode character.		"s" 0x73
0x7D	bString	("NUL")		0x00
0x7E	bString	Unicode character.		"s" 0x73
0x7F	bString	("NUL")		0x00
0x80	bString	Unicode character.		" " 0x20
0x81	bString	("NUL")		0x00
0x82	bString	Unicode character.		"S" 0x53
0x83	bString	("NUL")		0x00
0x84	bString	Unicode character.		"e" 0x65
0x85	bString	("NUL")		0x00
0x86	bString	Unicode character.		"m" 0x6D
0x87	bString	("NUL")		0x00
0x88	bString	Unicode character.		"i" 0x69
0x89	bString	("NUL")		0x00
0x8A	bString	Unicode character.		"c" 0x63
0x8B	bString	("NUL")		0x00
0x8C	bString	Unicode character.		"o" 0x6F
0x8D	bString	("NUL")		0x00
0x8E	bString	Unicode character.		"n" 0x6E
0x8F	bString	("NUL")		0x00
0x90	bString	Unicode character.		"d" 0x64
0x91	bString	("NUL")		0x00
0x92	bString	Unicode character.		"u" 0x75
0x93	bString	("NUL")		0x00
0x94	bString	Unicode character.		"c" 0x63
0x95	bString	("NUL")		0x00
0x96	bString	Unicode character.		"t" 0x74
0x97	bString	("NUL")		0x00

Table 5-6. EEPROM Organization (continued)

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
0x98	bString	Unicode character.		"o" 0x6F
0x99	bString	("NUL")		0x00
0x9A	bString	Unicode character.		"r" 0x72
0x9B	bString	("NUL")		0x00
USB String Descriptor–Product				
0x9C	bLength	String descriptor length in bytes (including bLength).		0x2C
0x9D	bDescriptorType	Descriptor type.	0x03	
0x9E	bString	Unicode character.		"U" 0x55
0x9F	bString	("NUL")		0x00
0xA0	bString	Unicode character.		"S" 0x53
0xA1	bString	("NUL")		0x00
0xA2	bString	Unicode character.		"B" 0x42
0xA3	bString	("NUL")		0x00
0xA4	bString	Unicode character.		"2" 0x32
0xA5	bString	("NUL")		0x00
0xA6	bString	Unicode character.		"." 0x2E
0xA7	bString	("NUL")		0x00
0xA8	bString	Unicode character.		"0" 0x30
0xA9	bString	("NUL")		0x00
0xAA	bString	Unicode character.		" " 0x20
0xAB	bString	("NUL")		0x00
0xAC	bString	Unicode character.		"S" 0x53
0xAD	bString	("NUL")		0x00
0xAE	bString	Unicode character.		"t" 0x74
0xAF	bString	("NUL")		0x00
0xB0	bString	Unicode character.		"o" 0x6F
0xB1	bString	("NUL")		0x00
0xB2	bString	Unicode character.		"r" 0x72
0xB3	bString	("NUL")		0x00
0xB4	bString	Unicode character.		"a" 0x61
0xB5	bString	("NUL")		0x00
0xB6	bString	Unicode character.		"g" 0x67
0xB7	bString	("NUL")		0x00
0xB8	bString	Unicode character.		"e" 0x65
0xB9	bString	("NUL")		0x00
0xBA	bString	Unicode character.		" " 0x20
0xBB	bString	("NUL")		0x00
0xBC	bString	Unicode character.		"D" 0x44
0xBD	bString	("NUL")		0x00
0xBE	bString	Unicode character.		"e" 0x65
0xBF	bString	("NUL")		0x00
0xC0	bString	Unicode character.		"v" 0x76
0xC1	bString	("NUL")		0x00

Table 5-6. EEPROM Organization (continued)

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
0xC2	bString	Unicode character.		"i" 0x69
0xC3	bString	("NUL")		0x00
0xC4	bString	Unicode character.		"c" 0x63
0xC5	bString	("NUL")		0x00
0xC6	bString	Unicode character.		"e" 0x65
0xC7	bString	("NUL")		0x00
USB String Descriptor–Serial Number (**Note**: The USB Mass Storage Class requires a unique serial number in each device. Not providing a unique serial number will crash the operating system. The serial number must be at least a minimum size of 12 characters. Some hosts will only treat the last 12 characters of the serial number as unique.)				
0xC8	bLength	String descriptor length in bytes (including bLength).		0x22
0xC9	bDescriptor Type	Descriptor type.	0x03	
0xCA	bString	Unicode character.		"1" 0x31
0xCB	bString	("NUL")		0x00
0xCC	bString	Unicode character.		"2" 0x32
0xCD	bString	("NUL")		0x00
0xCE	bString	Unicode character.		"3" 0x33
0xCF	bString	("NUL")		0x00
0xD0	bString	Unicode character.		"4" 0x34
0xD1	bString	("NUL")		0x00
0xD2	bString	Unicode character.		"5" 0x35
0xD3	bString	("NUL")		0x00
0xD4	bString	Unicode character.		"6" 0x36
0xD5	bString	("NUL")		0x00
0xD6	bString	Unicode character.		"7" 0x37
0xD7	bString	("NUL")		0x00
0xD8	bString	Unicode character.		"8" 0x38
0xD9	bString	("NUL")		0x00
0xDA	bString	Unicode character.		"9" 0x39
0xDB	bString	("NUL")		0x00
0xDC	bString	Unicode character.		"0" 0x30
0xDD	bString	("NUL")		0x00
0xDE	bString	Unicode character.		"A" 0x41
0xDF	bString	("NUL")		0x00
0xE0	bString	Unicode character.		"B" 0x42
0xE1	bString	("NUL")		0x00
0xE2	bString	Unicode character.		"C" 0x43
0xE3	bString	("NUL")		0x00
0xE4	bString	Unicode character.		"D" 0x44
0xE5	bString	("NUL")		0x00
0xE6	bString	Unicode character.		"E" 0x45
0xE7	bString	("NUL")		0x00
0xE8	bString	Unicode character.		"F" 0x46
0xE9	bString	("NUL")		0x00

Table 5-6. EEPROM Organization (continued)

EEPROM Address	Field Name	Field Description	Required Contents	Suggested Contents
0xEA to 0xFF	Unused ROM Space	Amount of unused ROM space will vary depending on strings.		0xFF

6.0   Absolute Maximum Ratings

Storage Temperature ....–65°C to +150°C

Ambient Temperature with power supplied...0°C to +55.4°C

Supply Voltage to Ground Potential...–0.5V to +4.0V

DC Input Voltage to Any Input Pin 5.25V

DC Voltage Applied to Outputs in High-Z State .... > –0.5V to V_{CC} + 0.5V

Power Dissipation .... > 936 mW

Static Discharge Voltage 2000V

Max Output Current per IO port .... 10 mA

7.0   Operating Conditions[5]

T_A (Ambient Temperature Under Bias) ....0°C to +70°C

Supply Voltage...+3.0V to +3.6V

Ground Voltage 0V

F_{osc} (Oscillator or Crystal Frequency) .... 24 MHz ± 100 ppm

.... Parallel Resonant

8.0   DC Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	Input High Voltage		2		5.25	V
V_{IL}	Input Low Voltage		–0.5		0.8	V
I_I	Input Leakage Current	$0 < V_{IN} < V_{CC}$			+ 10	µA
V_{OH}	Output Voltage High	I_{OUT} = 4 mA	2.4			V
V_{OL}	Output Voltage Low	I_{OUT} = –4 mA			0.4	V
I_{OH}	Output Current High				4	mA
I_{OL}	Output Current Low				4	mA
C_{IN}	Input Pin Capacitance	All but D+/D–			10	pF
		Only D+/D–			15	pF
I_{CC}	Supply Current	USB High Speed		235	260	mA
I_{CC}	Supply Current	USB Full Speed		90	150	mA

9.0   AC Electrical Characteristics

9.1   USB Transceiver

Complies with the USB 2.0 specification.

9.2   ATA Timing

The ATA interface supports ATA PIO modes 0, 3, and 4, and Ultra DMA modes 2 and 4 per the ATA Specification T13/1410D Rev. 3B.

Note:
5.   If an alternate clock source is input on XTALIN it must be supplied with standard 3.3V signaling characteristics and XTALOUT must be left floating.

10.0 Ordering Information

Part Number	Package Type
CY7C68300	56 SSOP
CY7C68300	56 QFN
CY4615	EZ-USB AT2 Reference Design Kit

11.0 Package Diagrams

DIMENSIONS IN INCHES MIN.
MAX.
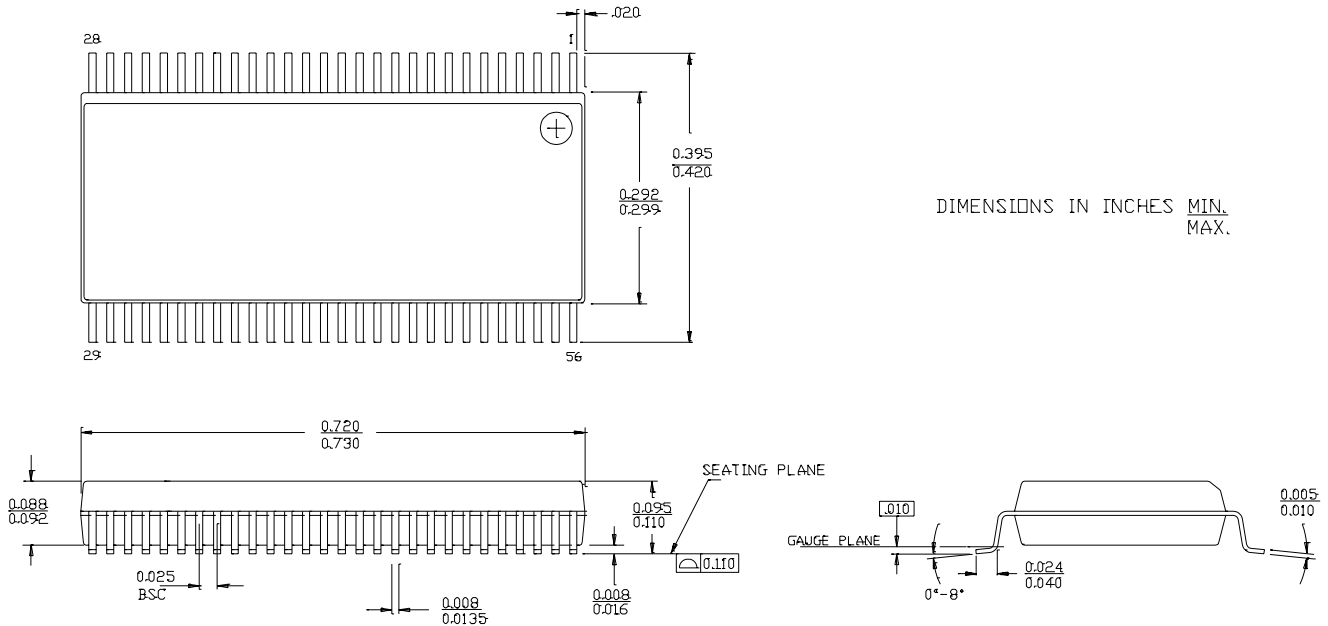
Figure 11-1. 56-lead Shrunk Small Outline Package 056

51-85062-*C

56-lead QFN (8 x 8 mm)

TOP VIEW

SIDE VIEW

BOTTOM VIEW
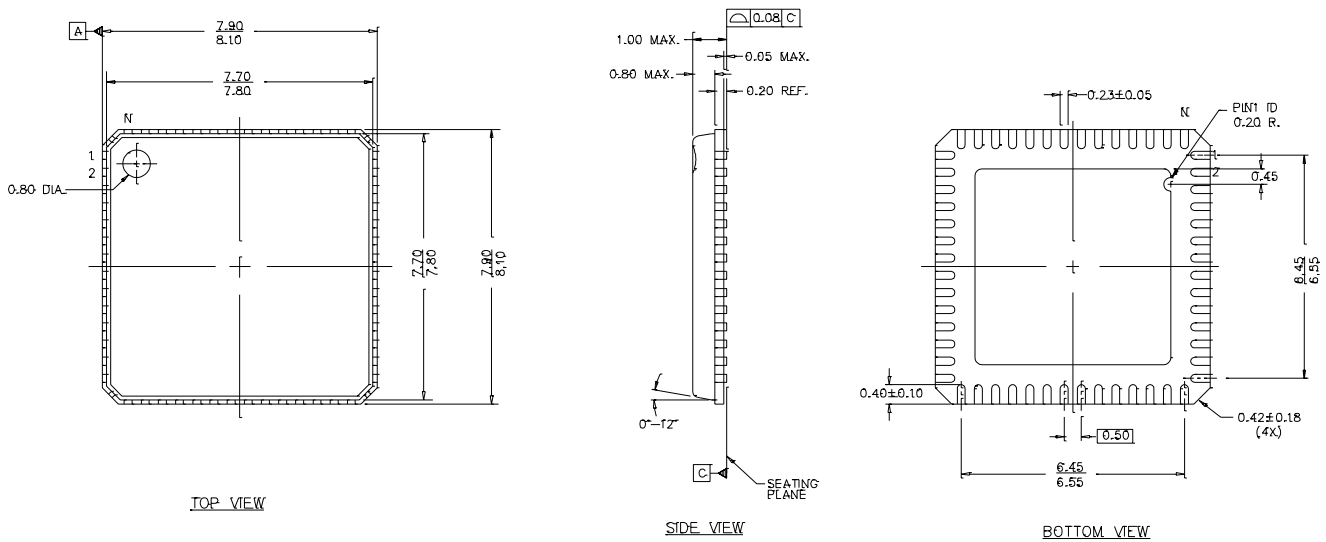
DIMENSIONS IN mm MIN.
MAX.

51-85144-*B

Figure 11-2. 56-lead Quad Flatpack No Lead (8 x 8 mm) LF56

12.0 PCB Layout Recommendations

The following recommendations should be followed to ensure reliable high-performance operation.

- At least a four-layer impedance controlled boards are required to maintain signal quality.
- Specify impedance targets (ask your board vendor what they can achieve).
- To control impedance, maintain trace widths and trace spacing.
- Minimize stubs to minimize reflected signals.
- Connections between the USB connector shell and signal ground must be done near the USB connector.
- Bypass/flyback caps on VBus, near connector, are recommended.
- DPLUS and DMINUS trace lengths should be kept to within 2 mm of each other in length, with preferred length of 20-30mm.
- Maintain a solid ground plane under the DPLUS and DMINUS traces. Do not allow the plane to be split under these traces.
- It is preferred is to have no vias placed on the DPLUS or DMINUS trace routing.
- Isolate the DPLUS and DMINUS traces from all other signal traces by no less than 10 mm.

Source for recommendations:
- EZ-USB FX2™ PCB Design Recommendations, http:///www.cypress.com/cfuploads/support/app_notes/FX2_PCB.pdf.
- High-speed USB Platform Design Guidelines, http://www.usb.org/developers/data/hs_usb_pdg_r1_0.pdf.

13.0 Quad Flat Package No Leads (QFN) Package Design Notes

Electrical contact of the part to the Printed Circuit Board (PCB) is made by soldering the leads on the bottom surface of the package to the PCB. Hence, special attention is required to the heat transfer area below the package to provide a good thermal bond to the circuit board. A Copper (Cu) fill is to be designed into the PCB as a thermal pad under the package. Heat is transferred from the AT2 through the device's metal paddle on the bottom side of the package. Heat from here is conducted to the PCB at the thermal pad. It is then conducted from the thermal pad to the PCB inner ground plane by a 5 x 5 array of Via. A Via is a plated through-hole in the PCB with a finished diameter of 13 mil. The QFN's metal die paddle must be soldered to the PCB's thermal pad. Solder mask is placed on the board top side over each Via to resist solder flow into the Via. The mask on the top side also minimizes outgassing during the solder reflow process.

For further information on this package design please refer to the application note "Surface Mount Assembly of AMKOR's MicroLeadFrame (MLF) Technology." This application note can be downloaded from AMKOR's website from the following URL http://www.amkor.com/products/notes_papers/MLF_AppNote_0301.pdf. The application note provides detailed information on board mounting guidelines, soldering flow, rework process, etc.

Figure 13-1 below display a cross-sectional area underneath the package. The cross section is of only one via. The solder paste template needs to be designed to allow at least 50% solder coverage. The thickness of the solder paste template should be 5 mil. It is recommended that "No Clean", type 3 solder paste is used for mounting the part. Nitrogen purge is recommended during reflow.
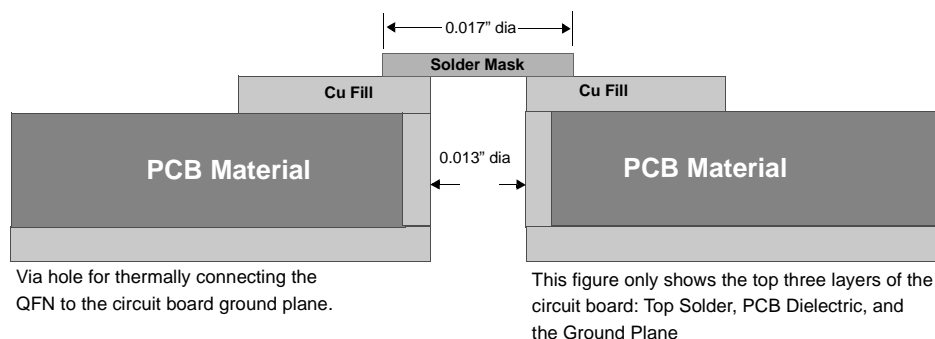

Via hole for thermally connecting the QFN to the circuit board ground plane.

This figure only shows the top three layers of the circuit board: Top Solder, PCB Dielectric, and the Ground Plane

Figure 13-1. Cross-Section of the Area Underneath the QFN Package

Figure 13-2 is a plot of the solder mask pattern and *Figure 13-3* displays an X-Ray image of the assembly (darker areas indicate solder.)
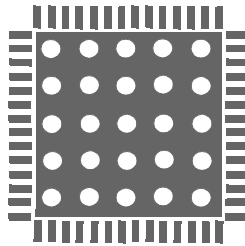
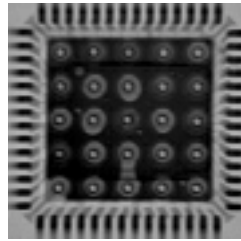**Figure 13-2. Plot of the Solder Mask (White Area)**

Figure 13-3. X-ray Image of the Assembly

14.0 Other Design Considerations

Certain design considerations must be followed to ensure proper operation of the EZ-USB AT2. The following items should be taken into account when designing a USB device with the EZ-USB AT2.

14.1 Proper Power-up Sequence

Power must be applied to the EZ-USB AT2 before, or at the same time as the ATA/ATAPI device. If power is supplied to the drive first, the EZ-USB AT2 will start up in an undefined state. Designs that utilize separate power supplies for the EZ-USB AT2 and the ATA/ATAPI device are not recommended.

14.2 IDE Removable Media Devices

The EZ-USB AT2 does not fully support IDE removable media devices. Changes in media state are not reported to the operating system so users will be unable to eject/reinsert media properly. This may result in lost or corrupted data.

14.3 Devices With Small Buffers

The size of the ATA/ATAPI device's buffer can greatly affect the overall data transfer performance. Care should be taken to ensure that devices have large enough buffers to handle the flow of data to/from the drive. The exact buffer size needed depends on a number of variables, but a good rule of thumb is:

(aprox min buffer size) = (data rate) * (seek time + rotation time + other)

where (other) may include things like time to switch heads, power-up a laser, etc. Devices with buffers that are too small to handle the extra data may perform considerably slower than expected.

14.4 USB Idle Mode

When the AT2 detects a lack of USB activity from the host, it enters an idle mode and waits for USB host activity to resume. While in this idle mode, the core logic is still functioning and power consumption remains at its active level. Because of this, the AT2 is not intended for use in battery or bus powered designs. Also, care should be taken to ensure that the AT2 does not draw power from VBUS, since such a design will not meet USB specifications for standby current.

15.0 Disclaimers, Trademarks, and Copyrights

Purchase of I^{2}C components from Cypress, or one of its sublicensed Associated Companies, conveys a license under the Philips I^{2}C Patent Rights to use these components in an I^{2}C system, provided that the system conforms to the I^{2}C Standard Specification as defined by Philips. EZ-USB AT2 is a trademark, and EZ-USB is a registered trademark, of Cypress Semiconductor. All product and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

				Description Title: CY7C68300 EZ-USB AT2™ USB 2.0 to ATA/ATAPI Bridge Document Number: 38-08011
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111608	05/15/02	BHA	New Data Sheet
*A	116660	08/30/02	BHA	Added new 56-pin Quad Flatpack No Lead package and pinout. Revised pin description table to reflect new package. Added typical reset diagram. Removed Advance Information.
*B	121518	12/17/02	GIR	Added section regarding idle current. Removed Isup row in power table. Revised PCB layout section.