CY7C1062DV33

16-Mbit (512 K × 32) Static RAM

Features

- High speed
  - ❐ t_{AA} = 10 ns
- Low active power
  - ❐ I_{CC} = 175 mA at 100 MHz
- Low complementary metal oxide semiconductor (CMOS) standby power
  - ❐ I_{SB2} = 25 mA
- Operating voltages of 3.3 ± 0.3 V
- 2.0 V data retention
- Automatic power down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ features
- Available in Pb-free 119-ball plastic ball grid array (PBGA) package

Functional Description

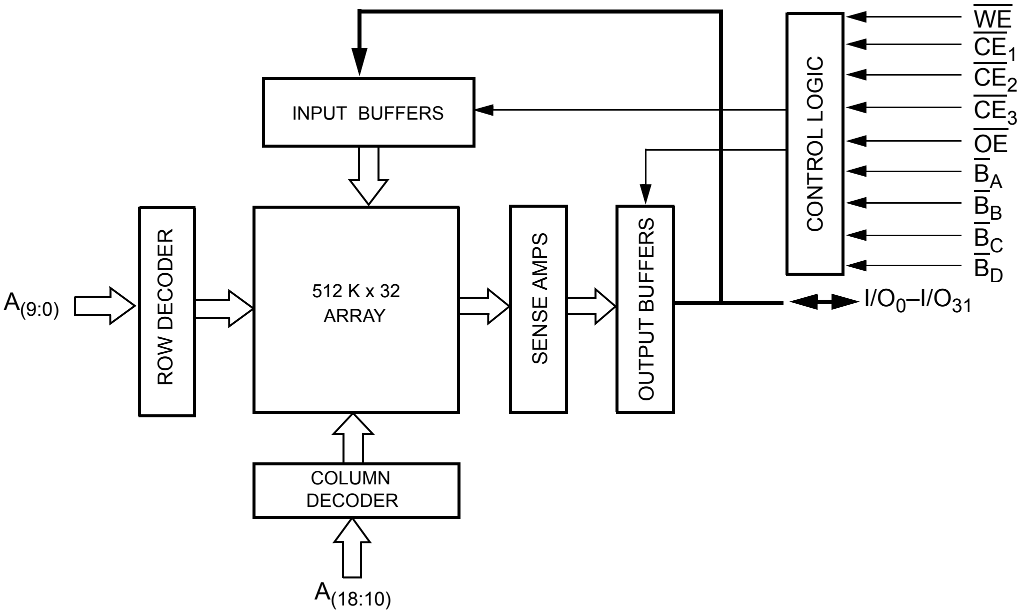
The CY7C1062DV33 is a high performance CMOS Static RAM organized as 524,288 words by 32 bits.

To write to the device, take Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW) and Write Enable ($\overline{WE}$) input LOW. If Byte Enable A ($\overline{B}_A$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{18}). If Byte Enable B ($\overline{B}_B$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}). Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond with the I/O pins I/O_{16} to I/O_{23} and I/O_{24} to I/O_{31}, respectively.

To read from the device, take Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If the first $\overline{B}_A$ is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If $\overline{B}_B$ is LOW, then data from memory appears on I/O_8 to I/O_{15}. Likewise, $\overline{B}_c$ and $\overline{B}_D$ correspond to the third and fourth bytes. See Truth Table on page 10 for a complete description of read and write modes.

The input and output pins (I/O_0 through I/O_{31}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the byte selects are disabled ($\overline{B}_{A-D}$ HIGH), or during a write operation ($\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$ LOW and $\overline{WE}$ LOW).

Logic Block Diagram



Contents

Selection Guide

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	175	mA
Maximum CMOS standby current	25	mA

Pin Configuration

Figure 1. 119-ball PBGA (Top View) [1]

	1	2	3	4	5	6	7
A	I/O$_{16}$	A	A	A	A	A	I/O$_{0}$
B	I/O$_{17}$	A	A	$\overline{CE}_1$	A	A	I/O$_{1}$
C	I/O$_{18}$	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O$_{2}$
D	I/O$_{19}$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O$_{3}$
E	I/O$_{20}$	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O$_{4}$
F	I/O$_{21}$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O$_{5}$
G	I/O$_{22}$	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O$_{6}$
H	I/O$_{23}$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O$_{7}$
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	NC
K	I/O$_{24}$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O$_{8}$
L	I/O$_{25}$	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O$_{9}$
M	I/O$_{26}$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O$_{10}$
N	I/O$_{27}$	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O$_{11}$
P	I/O$_{28}$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O$_{12}$
R	I/O$_{29}$	A	$\overline{B}_d$	NC	$\overline{B}_b$	A	I/O$_{13}$
T	I/O$_{30}$	A	A	$\overline{WE}$	A	A	I/O$_{14}$
U	I/O$_{31}$	A	A	$\overline{OE}$	A	A	I/O$_{15}$

Note

[1] NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [2] ....–0.5 V to +4.6 V

DC voltage applied to outputs in High Z state [2] ....–0.5 V to V_{CC} + 0.5 V

DC input voltage [2] ....–0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ....>2001 V

Latch-up current ....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions [3]	-10		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC}, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC}, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage [2]		–0.3	0.8	V
I_{IX}	Input leakage current	GND $\leq V_{IN} \leq V_{CC}$	–1	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_{OUT} \leq V_{CC}$, output disabled	–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = 1/t_{RC}, I_{OUT} = 0 mA, CMOS levels	–	175	mA
I_{SB1}	Automatic CE power-down current – TTL Inputs	Max V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	–	30	mA
I_{SB2}	Automatic CE power-down current – CMOS Inputs	Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3 V, $V_{IN} \geq V_{CC}$ – 0.3 V, or $V_{IN} \leq$ 0.3 V, f = 0	–	25	mA

Notes

2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
3. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.

Capacitance

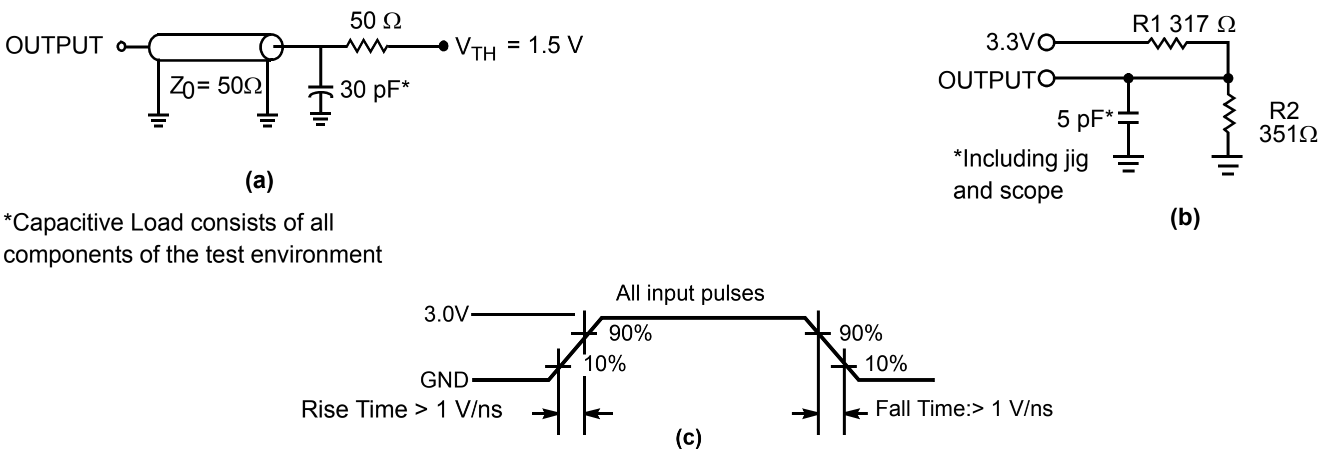
Parameter [4]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter [4]	Description	Test Conditions	119-ball PBGA	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board.	20.31	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		8.35	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [5]



*Capacitive Load consists of all components of the test environment

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Notes

4. Tested initially and after any design or process changes that may affect these parameters.
5. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.

AC Switching Characteristics

Over the Operating Range

Parameter [6]	Description	-10		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(typical) to the first access [7]	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{\text{CE}}$ Active LOW to data valid [8]	–	10	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to data valid	–	5	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to low Z [9]	1	–	ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to high Z [9]	–	5	ns
t_{LZCE}	$\overline{\text{CE}}$ Active LOW to low Z [8, 9]	3	–	ns
t_{HZCE}	$\overline{\text{CE}}$ Deselect HIGH to high Z [8, 9]	–	5	ns
t_{PU}	$\overline{\text{CE}}$ Active LOW to power-up [8, 10]	0	–	ns
t_{PD}	$\overline{\text{CE}}$ Deselect HIGH to power-down [8, 10]	–	10	ns
t_{DBE}	Byte enable to data valid		5	ns
t_{LZBE}	Byte enable to low Z [9]	1	–	ns
t_{HZBE}	Byte disable to high Z [9]	–	5	ns
Write Cycle [11, 12]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{\text{CE}}$ Active LOW to write end [8]	7	–	ns
t_{AW}	Address setup to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{\text{WE}}$ pulse width	7	–	ns
t_{SD}	Data setup to write end	5.5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to low Z [9]	3	–	ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to high Z [9]	–	5	ns
t_{BW}	Byte enable to end of write	7	–	ns

Notes

[6] Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V. Test conditions for the read cycle use output loading as shown in (a) of Figure 2 on page 5, unless specified otherwise.

[7] t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.

[8] $\overline{\text{CE}}$ indicates a combination of all three chip enables. When active LOW, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$,and $\overline{\text{CE}}_3$ LOW. When HIGH, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ HIGH.

[9] t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 2 on page 5. Transition is measured ±200 mV from steady state voltage.

[10] These parameters are guaranteed by design and are not tested.

[11] The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}_1$ LOW, $\overline{\text{CE}}_2$ LOW, $\overline{\text{CE}}_3$ LOW and $\overline{\text{WE}}$ LOW. Chip enables must be active and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.

[12] The minimum write cycle time for Write Cycle No.2 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD}.

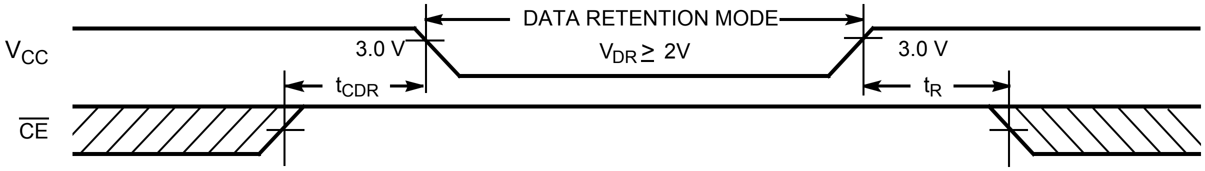
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions [13]	Min	Typ [14]	Max	Unit
V_{DR}	V_{CC} for data retention		2	–	–	V
I_{CCDR}	Data retention current	$V_{CC} = 2\ V$, $\overline{CE} \geq V_{CC} - 0.2\ V$, $V_{IN} \geq V_{CC} - 0.2\ V$, or $V_{IN} \leq 0.2\ V$	–	–	25	mA
t_{CDR} [15]	Chip deselect to data retention time		0	–	–	ns
t_R [16]	Operation recovery time		t_{RC}	–	–	ns

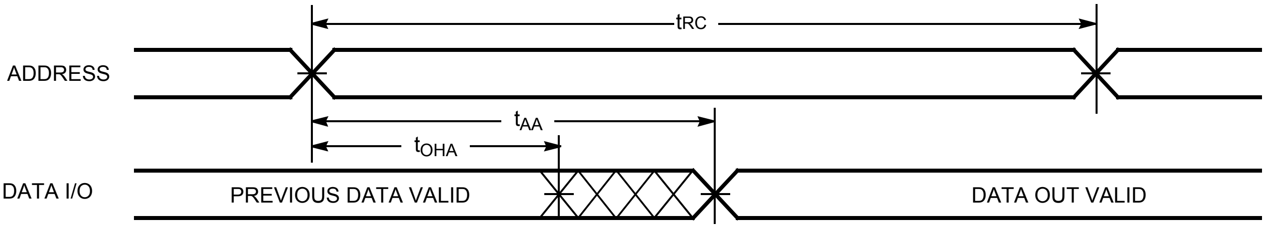
Data Retention Waveform

Figure 3. Data Retention Waveform



Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [17, 18]



Notes

13. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH
14. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\ °C$.
15. Tested initially and after any design or process changes that affects these parameters.
16. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50\ \mu s$ or stable at $V_{CC(min)} \geq 50\ \mu s$.
17. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D = V_{IL}$.
18. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [19, 20, 21]

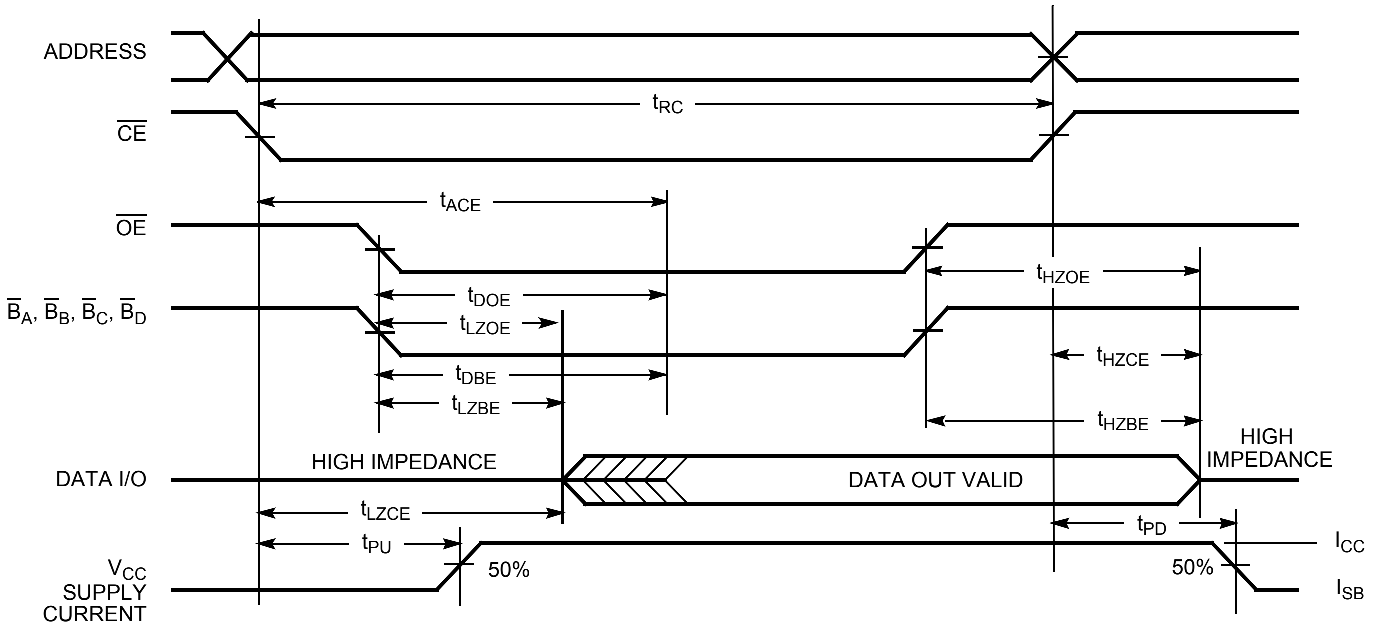
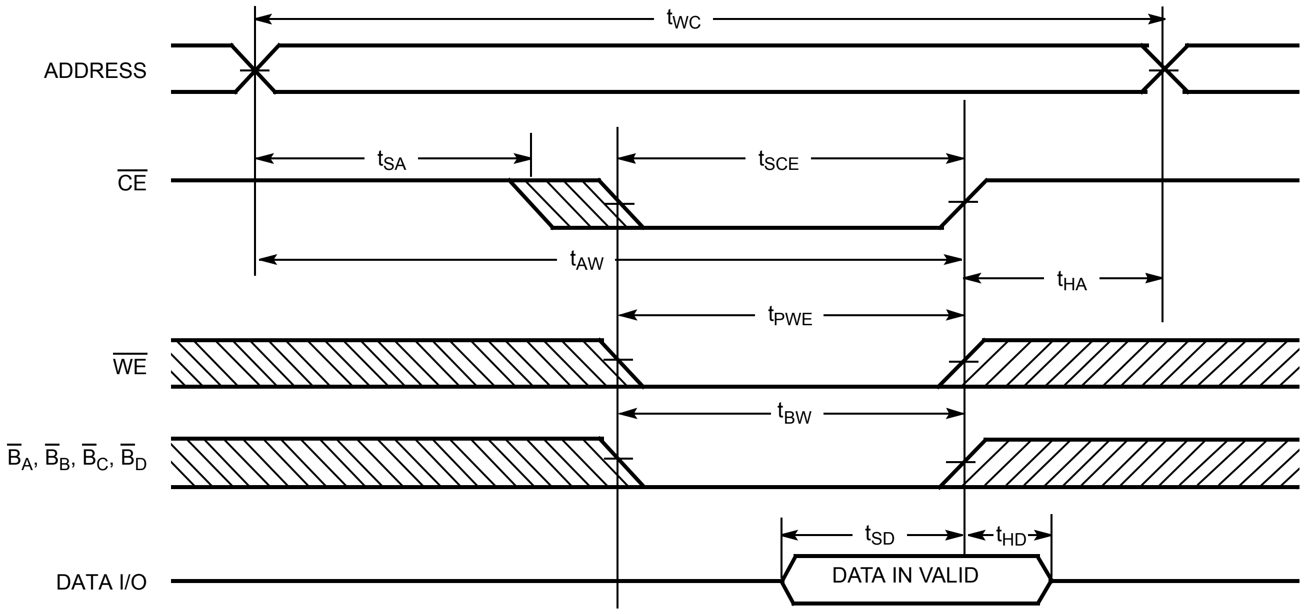


Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [19, 21, 22, 23]



Notes

19. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, CE_2 , and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, CE_2, or $\overline{CE}_3$ HIGH.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE}$ transition LOW.
22. Data I/O is high impedance if $\overline{OE}$ or $\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$ = V_{IH}.
23. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [24, 25, 26, 27]

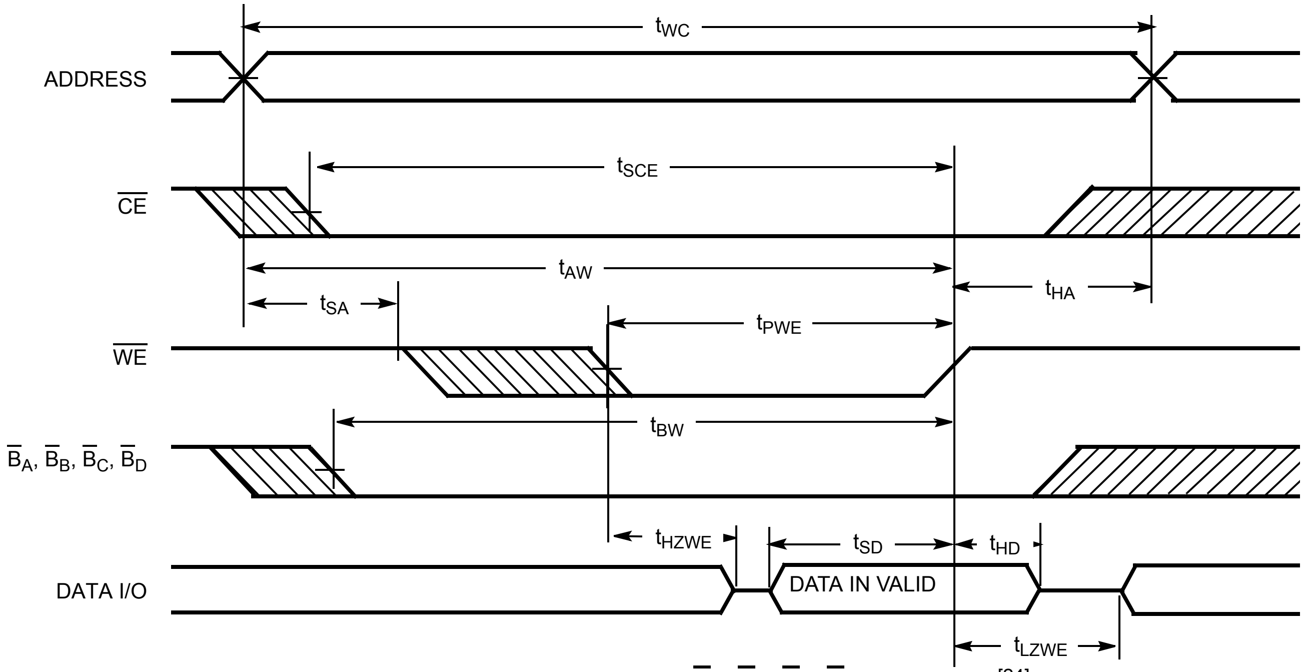
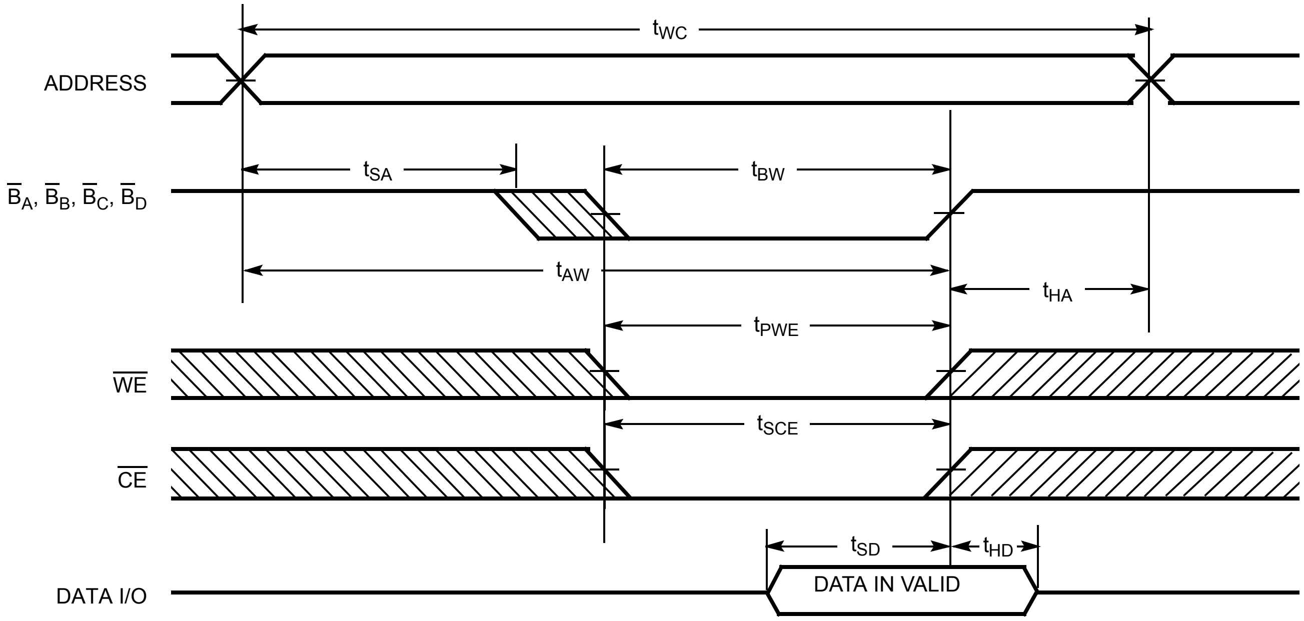


Figure 8. Write Cycle No. 3 ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ Controlled) [24]



Notes

[24] $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.

[25] Address valid before or similar to $\overline{CE}$ transition LOW.

[26] Data I/O is high impedance if $\overline{OE}$ or $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ = V_{IH}.

[27] If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{CE}_3$	$\overline{OE}$	$\overline{WE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_c$	$\overline{B}_D$	I/O_0–I/O_7	I/O_8–I/O_{15}	I/O_{16}–I/O_{23}	I/O_{24}–I/O_{31}	Mode	Power
H	X	X	X	X	X	X	X	X	High Z	High Z	High Z	High Z	power-down	(I_{SB})
X	H	X	X	X	X	X	X	X	High Z	High Z	High Z	High Z	power-down	(I_{SB})
X	X	H	X	X	X	X	X	X	High Z	High Z	High Z	High Z	power-down	(I_{SB})
L	L	L	L	H	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	(I_{CC})
L	L	L	L	H	L	H	H	H	Data out	High Z	High Z	High Z	Read byte A bits only	(I_{CC})
L	L	L	L	H	H	L	H	H	High Z	Data out	High Z	High Z	Read byte B bits only	(I_{CC})
L	L	L	L	H	H	H	L	H	High Z	High Z	Data out	High Z	Read byte C bits only	(I_{CC})
L	L	L	L	H	H	H	H	L	High Z	High Z	High Z	Data out	Read Byte D bits only	(I_{CC})
L	L	L	X	L	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	(I_{CC})
L	L	L	X	L	L	H	H	H	Data in	High Z	High Z	High Z	Write byte A bits only	(I_{CC})
L	L	L	X	L	H	L	H	H	High Z	Data in	High Z	High Z	Write byte B bits only	(I_{CC})
L	L	L	X	L	H	H	L	H	High Z	High Z	Data in	High Z	Write byte C bits only	(I_{CC})
L	L	L	X	L	H	H	H	L	High Z	High Z	High Z	Data in	Write byte D bits only	(I_{CC})
L	L	L	H	H	X	X	X	X	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I_{CC})
L	L	L	X	X	H	H	H	H	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1062DV33-10BGI	51-85115	119-ball Plastic Ball Grid Array (14 × 22 × 2.4 mm)	Industrial
	CY7C1062DV33-10BGXI		119-ball Plastic Ball Grid Array (14 × 22 × 2.4 mm) (Pb-free)	

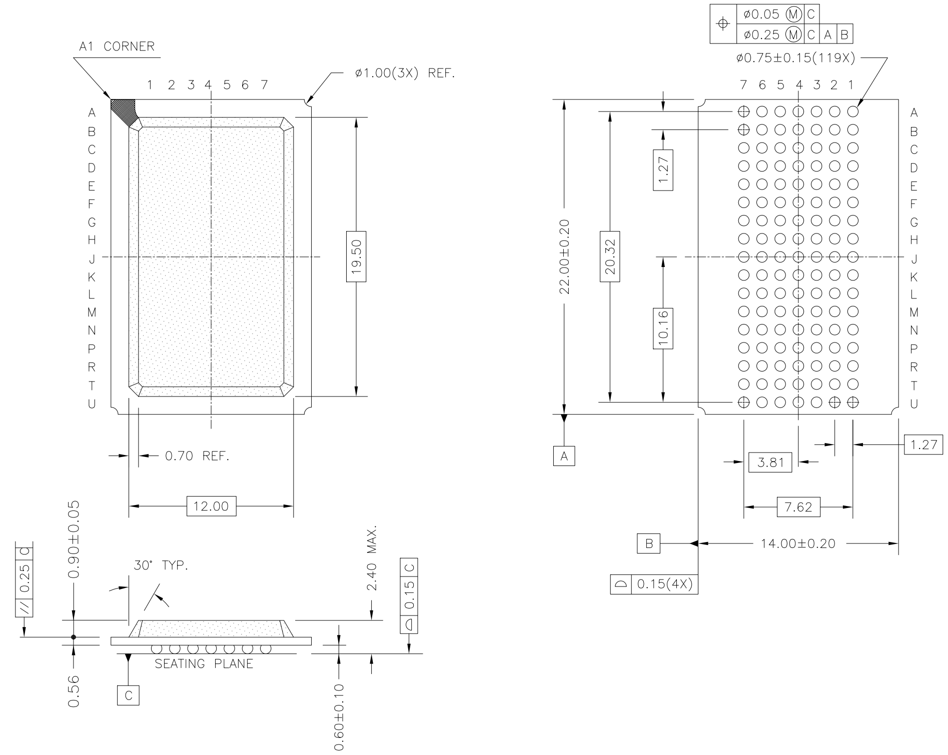
Ordering Code Definitions

CY 7 C 1 06 2 D V33 - 10 BG X I

Temperature Range:
I = Industrial
Pb-free
Package Type:
BG = 119-ball PBGA
Speed: 10 ns
Voltage range: V33 = 3 V to 3.6 V
Process Technology: D = C9, 90 nm
Data width: 2 = × 32-bits
06 = 16-Mbit density
1 = Fast Asynchronous SRAM family
Technology Code: C = CMOS
Marketing Code: 7 = SRAM
Company ID: CY = Cypress

Package Diagram

Figure 9. 119-ball PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115



51-85115 *C

Acronyms

Acronym	Description
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
PBGA	plastic ball grid array
SRAM	static random access memory
TTL	transistor-transistor logic
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History

Document Title: CY7C1062DV33, 16-Mbit (512 K × 32) Static RAM
Document Number: 38-05477

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance data sheet for C9 IPP
*A	233748	RKF	See ECN	AC, DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in the Ordering Information
*B	469420	NXR	See ECN	Converted from Advance Information to Preliminary Removed –8 and –12 speed bins from product offering Removed Commercial operating Range Changed J7 Ball of PBGA from DNU to NC in the pinout diagram Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page 2 Changed $I_{CC(Max)}$ from 220 mA to 150 mA Changed $I_{SB1(Max)}$ from 70 mA to 30 mA Changed $I_{SB2(Max)}$ from 40 mA to 25 mA Specified the Overshoot specification in footnote 1 Changed t_{SD} from 5.5 ns to 5 ns Added Data Retention Characteristics table and waveform on page 5. Updated the 48-pin FBGA package Updated the Ordering Information Table
*C	499604	NXR	See ECN	Added note 1 for NC pins Updated Test Condition for I_{CC} in DC Electrical Characteristics table Added note for t_{ACE}, t_{LZCE}, t_{HZCE}, t_{PU}, t_{PD}, and t_{SCE} in AC Switching Characteristics Table on page 4
*D	1462583	VKN / AESA	See ECN	Converted from preliminary to final Updated block diagram Changed I_{CC} spec from 150 mA to 175 mA Updated thermal specs
*E	2541850	VKN / PYRS	07/22/08	Added -10BGI part in the Ordering Information table
*F	3109102	AJU	12/13/2010	Added Ordering Code Definitions. Updated Package Diagram.
*G	3137613	PRAS	01/13/2011	Added Acronyms and Units of Measure. Updated datasheet as per template Updated all footnotes sequentially
*H	3416006	TAVA	10/20/2011	Updated Features. Updated DC Electrical Characteristics. Updated Switching Waveforms. Updated in new template.

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