CY7C1069DV33

16-Mbit (2 M × 8) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 175 mA at 100 MHz
- Low complementary metal oxide semiconductor (CMOS) standby power
  - I_{SB2} = 25 mA
- Operating voltages of 3.3 ± 0.3 V
- 2.0 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$ and CE_2 features
- Available in Pb-free 54-pin thin small outline package (TSOP) Type II and 48-ball very fine-pitch ball grid array (VFBGA) packages.

Functional Description

The CY7C1069DV33 is a high performance CMOS Static RAM organized as 2,097,152 words by 8 bits.

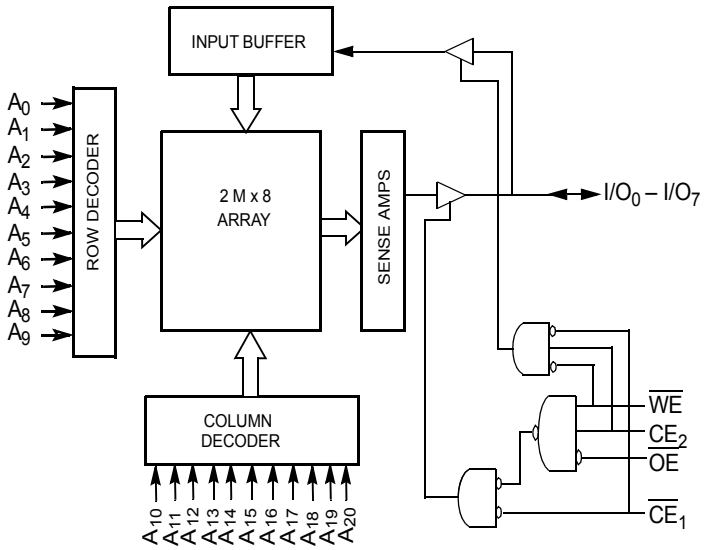
To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{20}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. See Truth Table on page 10 for a complete description of Read and Write modes.

The input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C1069DV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 48-ball very fine-pitch ball grid array (VFBGA) package.

Logic Block Diagram



Contents

Selection Guide

	-10	Unit
Maximum access time	10	ns
Maximum operating current	175	mA
Maximum CMOS standby current	25	mA

Pin Configurations

Figure 1. 54-pin TSOP II (Top View) [1]

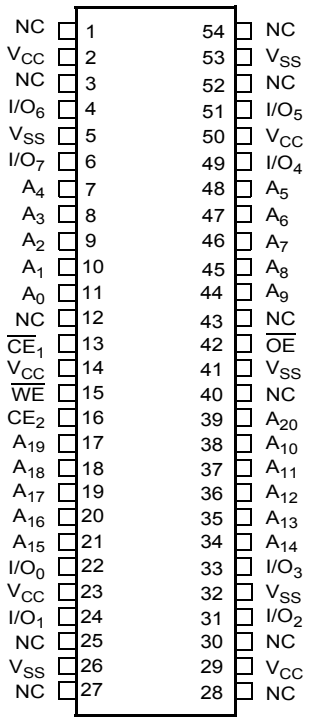
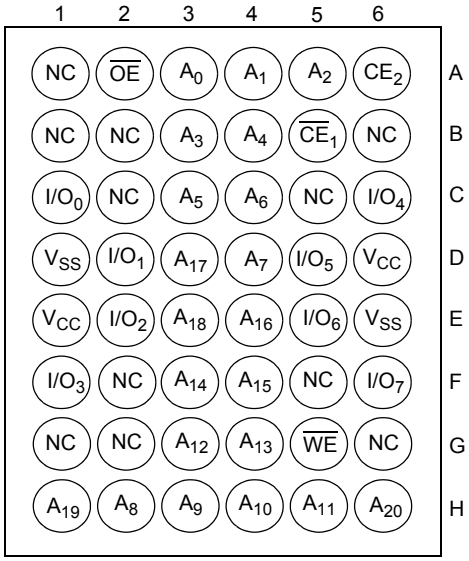


Figure 2. 48-ball VFBGA (Top View) [1]



Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [2] .....–0.5 V to +4.6 V

DC voltage applied to outputs in High Z state [2] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [2] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC}, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC}, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage	–	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage [2]	–	–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$, I_{OUT} = 0 mA, CMOS levels	–	175	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	30	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3 V, CE_2 ≤ 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0	–	25	mA

Note
2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.

Capacitance

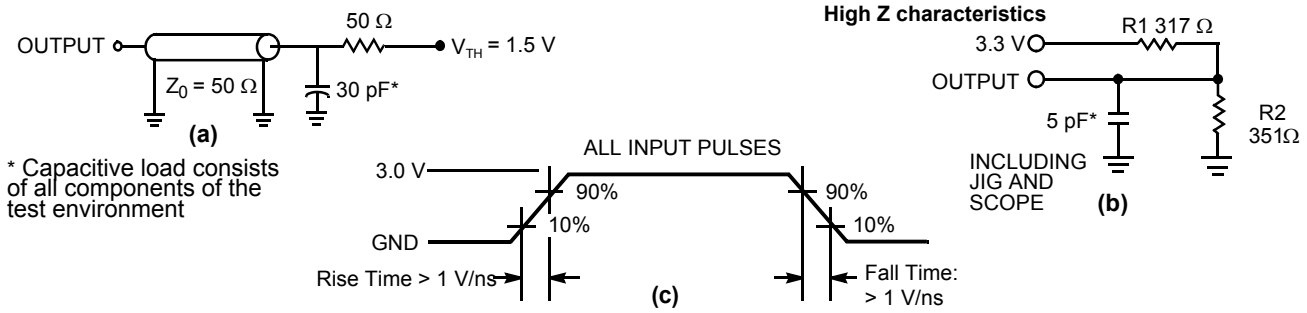
Parameter [3]	Description	Test Conditions	TSOP II	VFBGA	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	6	8	pF
C_{OUT}	IO capacitance		8	10	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	TSOP II	VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	24.18	28.37	°C/W
Θ_{JC}	Thermal resistance (junction to case)		5.40	5.79	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [4]



Notes
3. Tested initially and after any design or process changes that may affect these parameters.
4. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.

AC Switching Characteristics

Over the Operating Range

Parameter [5]	Description	-10		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(typical) to the first access [6]	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}_1$ LOW/CE_2 HIGH to data valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [7]	1	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [7]	–	5	ns
t_{LZCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to low Z [7]	3	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH/CE_2 LOW to high Z [7]	–	5	ns
t_{PU}	$\overline{CE}_1$ LOW/CE_2 HIGH to power-up [8]	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH/CE_2 LOW to power-down [8]	–	10	ns
Write Cycle [9, 10]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to write end	7	–	ns
t_{AW}	Address setup to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data setup to write end	5.5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [7]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [7]	–	5	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in (a) of Figure 3 on page 5, unless specified otherwise.
6. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
7. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 5. Transition is measured ±200 mV from steady state voltage.
8. These parameters are guaranteed by design and are not tested.
9. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. $\overline{CE}_1$ and $\overline{WE}$ are LOW along with CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

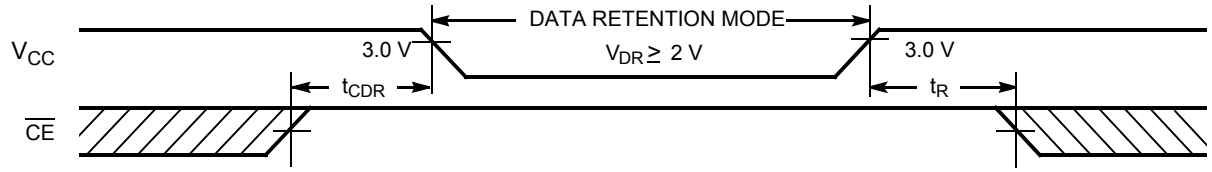
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2	–	V
I_{CCDR}	Data retention current	V_{CC} = 2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	25	mA
t_{CDR} [11]	Chip deselect to data retention time		0	–	ns
t_R [12]	Operation recovery time		t_{RC}	–	ns

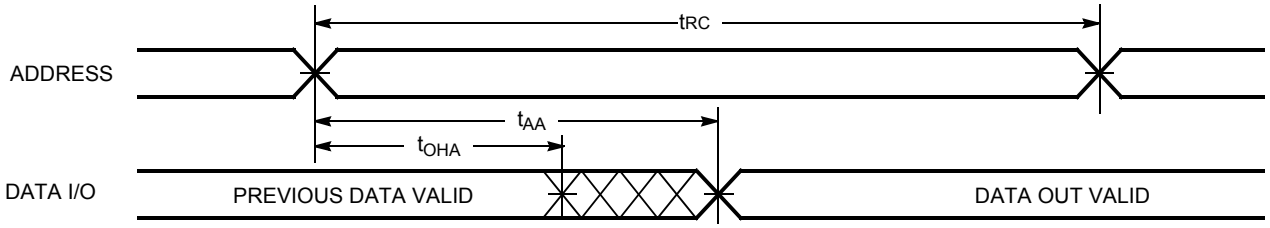
Data Retention Waveform

Figure 4. Data Retention Waveform



Switching Waveforms

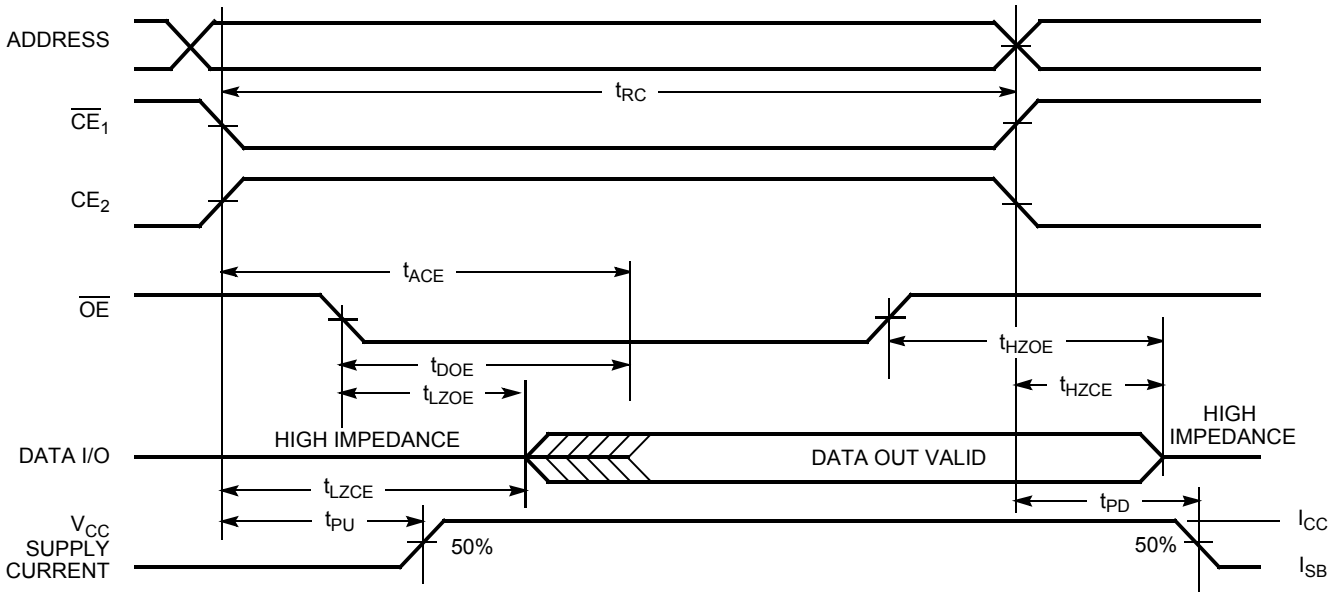
Figure 5. Read Cycle No. 1 (Address Transition Controlled) [13, 14]



Notes
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.
13. The device is continuously selected. $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$.
14. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [15, 16]



Notes
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid before or similar to $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18, 19]

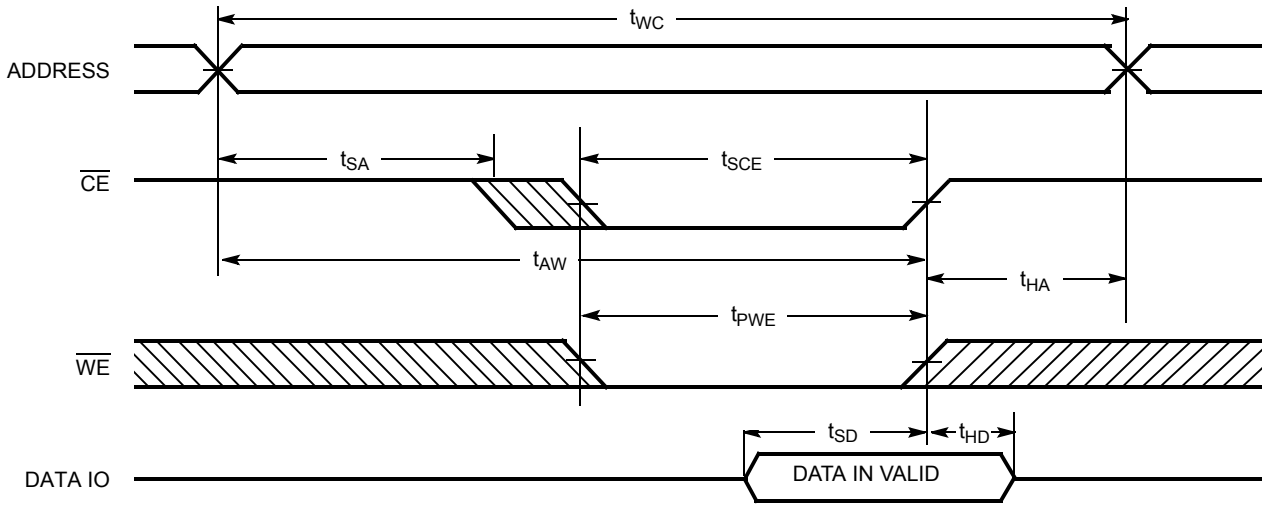
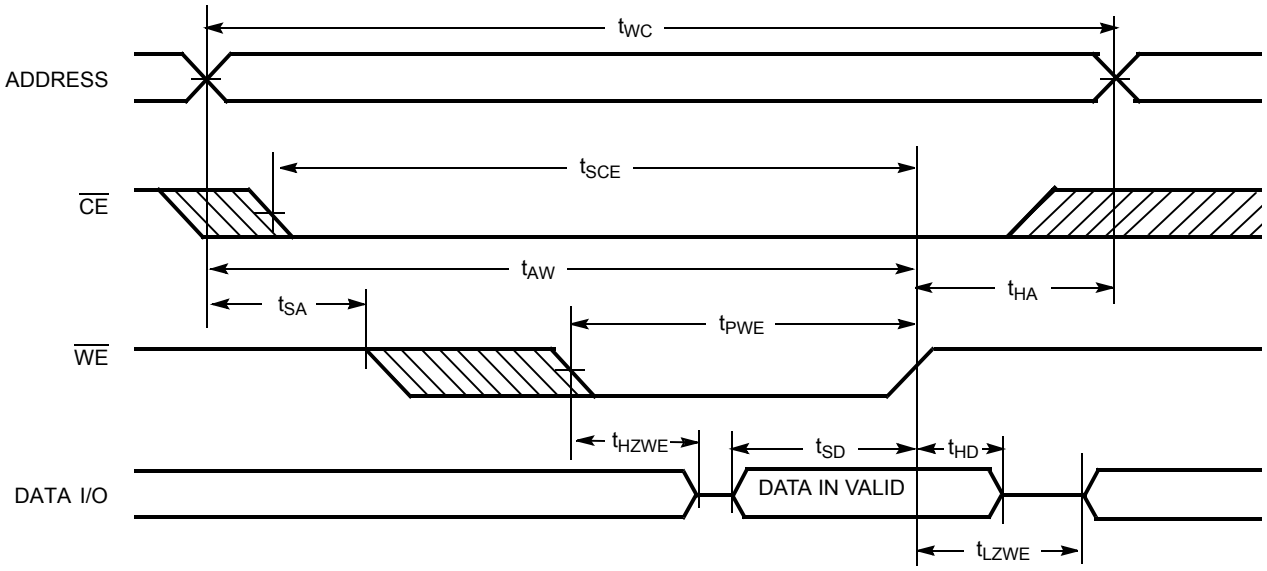


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [17, 18, 19]



Notes
17. $\overline{CE}$ is a shorthand combination of both $\overline{CE}_1$ and CE_2 combined. It is active LOW.
18. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

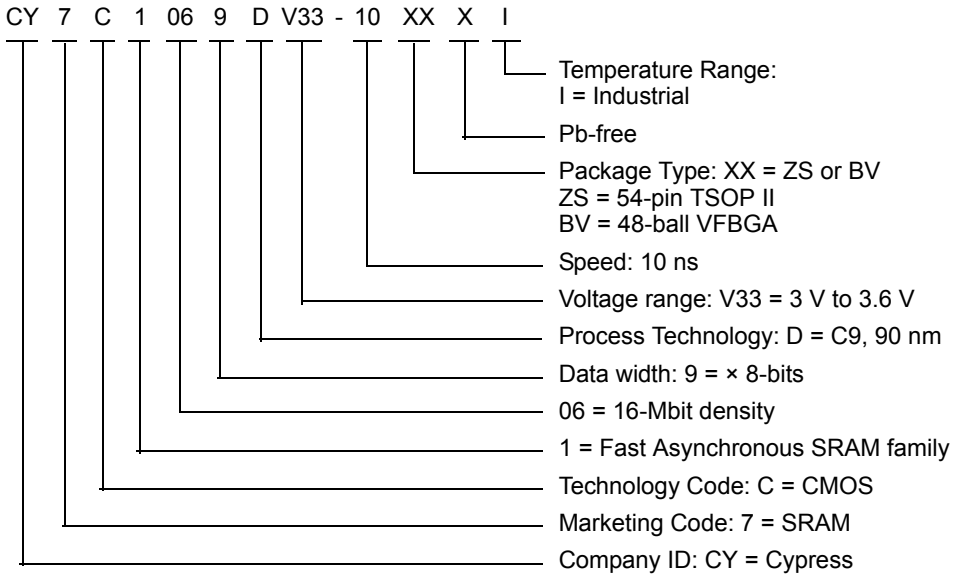
Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I_{SB})
X	L	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	H	Data out	Read all bits	Active (I_{CC})
L	H	X	L	Data in	Write all bits	Active (I_{CC})
L	H	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

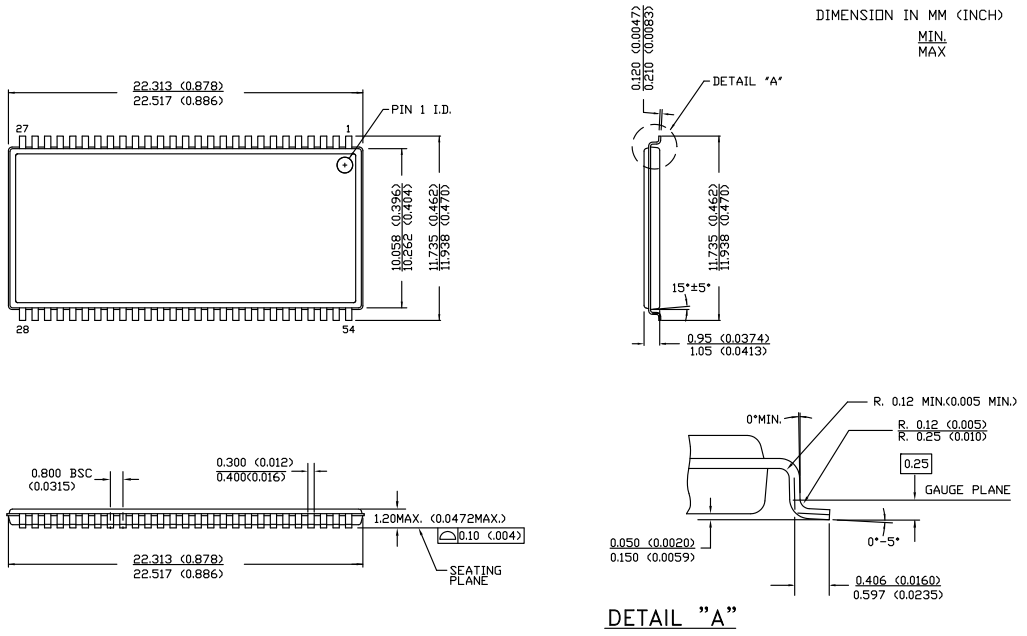
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1069DV33-10ZSXI	51-85160	54-pin TSOP II (Pb-free)	Industrial
	CY7C1069DV33-10BVXI	51-85178	48-ball VFBGA (Pb-free)	

Ordering Code Definitions



Package Diagrams

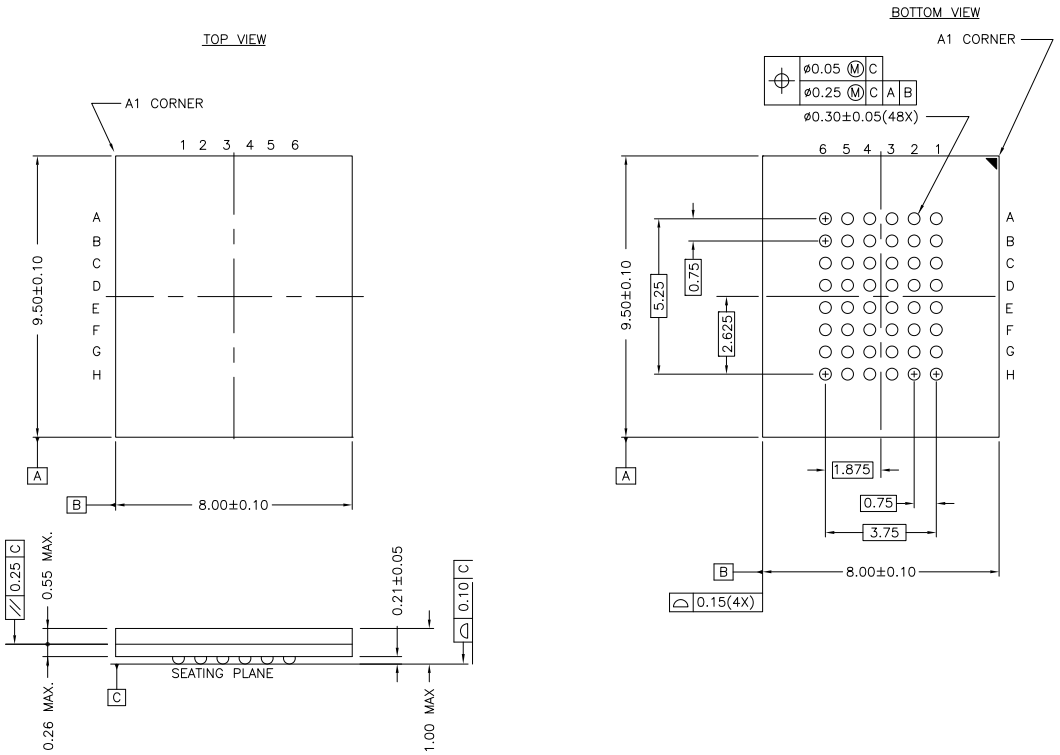
Figure 9. 54-pin TSOP Type II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 *C

Package Diagrams (continued)

Figure 10. 48-ball VFBGA (8 × 9.5 × 1.0 mm) BV48B Package Outline, 51-85178



51-85178 *A

Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
VFBGA	very fine-pitch ball grid array
TSOP	thin small outline package
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1069DV33, 16-Mbit (2 M × 8) Static RAM Document Number: 38-05478				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance datasheet for C9 IPP
*A	233748	See ECN	RKF	Modified AC, DC parameters as per EROS (Specification 01-2165) Pb-free Offering in the Ordering Information
*B	469420	See ECN	NXR	Converted from Advance Information to Preliminary Removed -8 and -12 speed bins from product offering Removed Commercial Operating Range Changed 2G Ball of FBGA and pin 40 of TSOPII from DNU to NC Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page 3 Changed $I_{CC(Max)}$ from 220 mA to 100 mA Changed $I_{SB1(Max)}$ from 70 mA to 30 mA Changed $I_{SB2(Max)}$ from 40 mA to 25 mA Specified the Overshoot specification in footnote 1 Added Data Retention Characteristics table on page 5 Updated the 48-pin FBGA package Updated the Ordering Information table.
*C	499604	See ECN	NXR	Added note 1 for NC pins Updated Test Condition for I_{CC} in DC Electrical Characteristics table Updated the 48-ball FBGA Package
*D	1462585	See ECN	VKN / AESA	Converted from preliminary to final Changed I_{CC} spec from 125 mA to 175 mA Updated thermal specs
*E	3109063	12/13/2010	AJU	Added Ordering Code Definitions. Updated Package Diagrams.
*F	3147335	01/19/2011	PRAS	Added Acronyms and Units of Measure table. Updated the datasheet as per template.
*G	3417274	10/21/2011	TAVA	Updated Features. Updated DC Electrical Characteristics. Updated Switching Waveforms.

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