18-Mb 4-Word Burst SRAM with DDR-I Architecture

Features

- **18-Mb Density (2M x 8, 1M x 18, 512K x 36)**
  - **Supports concurrent transactions**
- **300-MHz Clock for High Bandwidth**
- **4-Word Burst for reducing address bus frequency**
- **Double Data Rate (DDR) interfaces (data transferred at 600 MHz) @300 MHz**
- **Two input clocks (K and $\overline{K}$) for precise DDR timing**
  - **SRAM uses rising edges only**
- **Two output clocks (C and $\overline{C}$) accounts for clock skew and flight time mismatches**
- **Separate Port Selects for depth expansion**
- **Synchronous internally self-timed writes**
- **1.8V core power supply with HSTL Inputs and Outputs**
- **Variable drive HSTL output buffers**
- **Expanded HSTL output voltage (1.4V–V_{DD})**
- **13x15 mm 1.0 mm pitch fBGA package, 165 ball (11x15 matrix)**
- **JTAG Interface**

Configurations

CY7C1398V25 – 1M x 18

CY7C1323V25 – 512K x 36

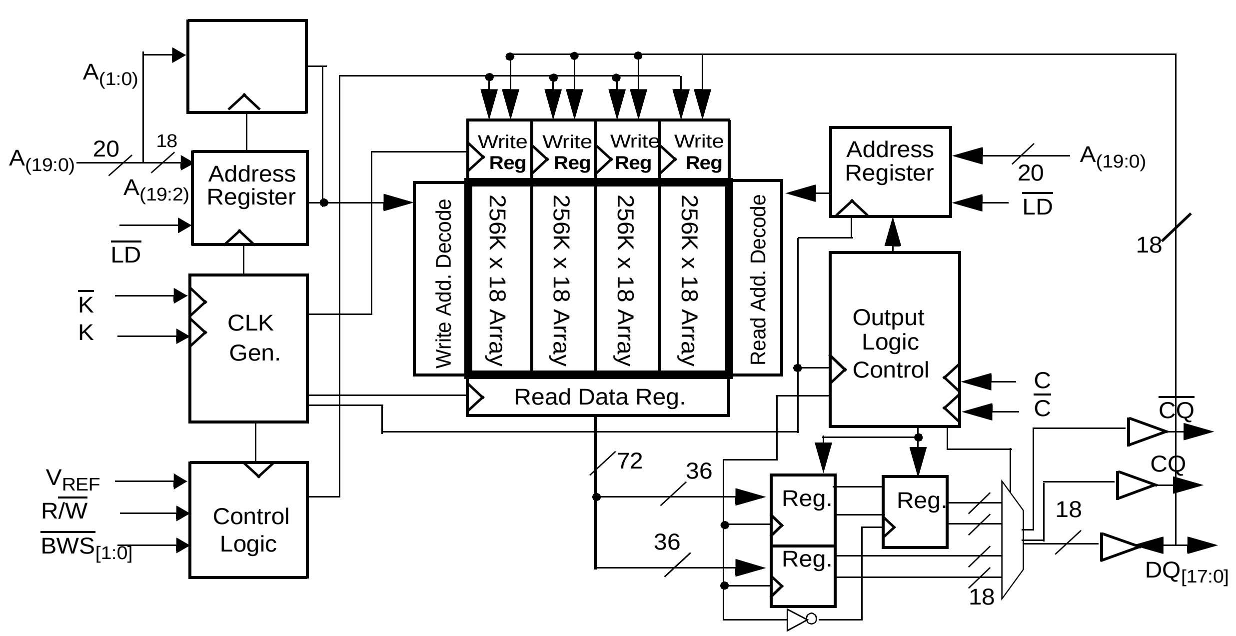
Functional Description

The CY7C1398V25/CY7C1323V25 are 2.5V Synchronous Pipelined SRAMs equipped with DDR-I (Double Data Rate) architecture. The DDR-I consists of an SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. Addresses for Read and Write are latched on alternate rising edges of the input (K) clock.Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of C and $\overline{C}$ if provided, or on the rising edge of K and $\overline{K}$ if C/$\overline{C}$ are not provided. Every read or write operation is associated with four words that burst sequentially into or out of the device. The burst counter takes in the least two significant bits of the external address and bursts four 18-bit words in the case of CY7C1398V25 and four 36-bit words in the case of CY7C1323V25. Depth expansion is accomplished with Port Selects for each port. Port selects allow each port to operate independently.

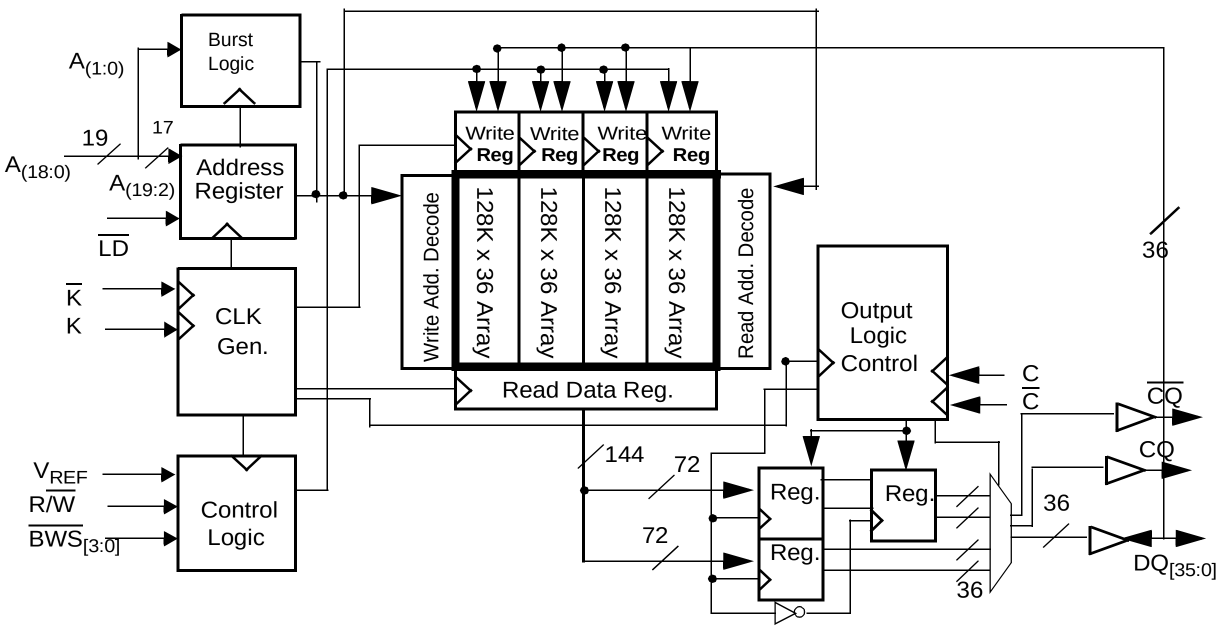
Asynchronous inputs include impedance match (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need to separately capture data from each individual DDR SRAM in the system design. Output data clocks (C/$\overline{C}$) are also provided for maximum system clocking and data synchronization flexibility.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the C or $\overline{C}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Logic Block Diagram (CY7C1398V25)



Logic Block Diagram (CY7C1323V25)



Selection Guide

	300 MHz	250 MHz	200 MHz	167 MHz
Maximum Operating Frequency (MHz)	300	250	200	167
Maximum Operating Current (mA)	TBD	TBD	TBD	TBD

Pin Configurations

CY7C1398V25 (1M x 18) - 11 x 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	GND/72M	A	$\overline{WE}$	$\overline{BWS_1}$	$\overline{K}$	NC	$\overline{LD}$	A	GND/36M	CQ
B	NC	DQ9	NC	A	NC	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	VSS	A	A0	A1	VSS	NC	DQ7	NC
D	NC	NC	DQ10	VSS	VSS	VSS	VSS	VSS	NC	NC	NC
E	NC	NC	DQ11	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ6
F	NC	DQ12	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ5
G	NC	NC	DQ13	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
H	NC	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ4	NC
K	NC	NC	DQ14	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ3
L	NC	DQ15	NC	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ2
M	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	NC	DQ1	NC
N	NC	NC	DQ16	VSS	A	A	A	VSS	NC	NC	NC
P	NC	NC	DQ17	A	A	C	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

CY7C1323V25 (512K x 36) - 11 x 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	GND/144M	NC/36M	$\overline{WE}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{LD}$	A	GND/72M	CQ
B	NC	DQ27	DQ18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	DQ28	VSS	A	A0	A1	VSS	NC	DQ17	DQ7
D	NC	DQ29	DQ19	VSS	VSS	VSS	VSS	VSS	NC	NC	DQ16
E	NC	NC	DQ20	VDDQ	VSS	VSS	VSS	VDDQ	NC	DQ15	DQ6
F	NC	DQ30	DQ21	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ5
G	NC	DQ31	DQ22	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ14
H	NC	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	DQ32	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ13	DQ4
K	NC	NC	DQ23	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ12	DQ3
L	NC	DQ33	DQ24	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ2
M	NC	NC	DQ34	VSS	VSS	VSS	VSS	VSS	NC	DQ11	DQ1
N	NC	DQ35	DQ25	VSS	A	A	A	VSS	NC	NC	DQ10
P	NC	NC	DQ26	A	A	C	A	A	NC	DQ9	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Pin Definitions

Name	I/O	Description
$DQ_{[x:0]}$	Input/Output-Synchronous	Data Input/Output signals: Inputs are sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. These pins drive out the requested data during a Read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during Read operations or K and $\overline{K}$ when in single clock mode. When the Read port is deselected, $Q_{[x:0]}$ are automatically three-stated. CY7C1398V25—$DQ_{[17:0]}$ CY7C1323V25—$DQ_{[35:0]}$
$\overline{LD}$	Input-Synchronous	Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of 4 data (two clock periods of bus activity).
$\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$, $\overline{BWS}_3$	Input-Synchronous	Byte Write Select 0, 1, 2, and 3—active LOW. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C1398V25—$\overline{BWS}_0$ controls $D_{[8:0]}$ and $\overline{BWS}_1$ controls $D_{[17:9]}$. CY7C1323V25—$\overline{BWS}_0$ controls $D_{[8:0]}$, $\overline{BWS}_1$ controls $D_{[17:9]}$, $\overline{BWS}_2$ controls $D_{[26:18]}$ and $\overline{BWS}_3$ controls $D_{[35:27]}$ All the byte writes are sampled on the same edge as the data. Deselecting a Byte Write Select will cause the corresponding byte of data to be ignored and not written into the device.
A, A0, A1	Input-Synchronous	Address inputs. These address inputs are multiplexed for both Read and Write operations. Internally, the device is organized as 1M x 18 4 arrays each of 256K x 18) for CY7C1323V25 and 256K x 36 (4 arrays each of 128K x 36) for CY7C1398V25. CY7C1323V25—A0 and A1 are the inputs to the burst counter. These are incremented in a linear fashion internally. 20 address inputs are needed to access the entire memory array. CY7C1398V25—A0 and A1 are the inputs to the burst counter. These are incremented in a linear fashion internally. 19 address inputs are needed to access the entire memory array. All the address inputs are ignored when the appropriate port is deselected.
$R/\overline{W}$	Input-Synchronous	Synchronous Read/Write Input: When $\overline{LD}$ is LOW, this input designates the access type (Read when $R/\overline{W}$ is HIGH, Write when $R/\overline{W}$ is LOW) for loaded address. $R/\overline{W}$ must meet the setup and hold times around edge of K.
C	Input-Clock	Positive Output Clock Input. C is used in conjunction with $\overline{C}$ to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
$\overline{C}$	Input-Clock	Negative Output Clock Input. $\overline{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
K	Input-Clock	Positive Input Clock Input. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input-Clock	Negative Input Clock Input. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.
CQ, $\overline{CQ}$	Output-Clock	Synchronous Echo clock outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals are free running and do not stop when the output data bus (which is shared with the inputs) is three-stated.
ZQ	Input	Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternately, this pin can be connected directly to V_{DD}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
TDO	Output	TDO for JTAG.
TCK	Input	TCK pin for JTAG.

Pin Definitions (continued)

Name	I/O	Description
TDI	Input	TDI pin for JTAG.
TMS	Input	TMS pin for JTAG.
NC	Input	No connects. Can be tied to any voltage level.
NC/36M	Input	Address expansion for 36M. This is not connected to the die.
GND/72M	Input	Address expansion for 72M. This should be tied LOW on the 18M devices.
GND/144M	Input	Address expansion for 144M. This should be tied LOW on the 18M devices.
V_{REF}	Input-Reference	Reference Voltage Input. Static input used to set the reference level for HSTL inputs and Outputs as well as AC measurement points.
V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 2.5V power supply.
V_{SS}	Ground	Ground for the device. Should be connected to ground of the system.
V_{DDQ}	Power Supply	Power supply inputs for the outputs of the device. Should be connected to 1.5V power supply.
NC	NC	No connect

Introduction

Functional Overview

The CY7C1398V25/CY7C1323V25 are synchronous pipelined Burst SRAMs equipped with DDR-I interface.

Accesses are initiated on the Positive Input Clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and $\overline{K}$) and all output timing is referenced to the output clocks (C and $\overline{C}$ or K and $\overline{K}$ when in single clock mode).

All synchronous data inputs ($D_{[x:0]}$) inputs pass through input registers controlled by the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the output clocks (C and $\overline{C}$ or K and $\overline{K}$ when in single clock mode).

All synchronous control (R/$\overline{W}$, $\overline{LD}$, $\overline{BWS}_0$, $\overline{BWS}_1$) inputs pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

The following descriptions take CY7C1398V25 as an example. However, the same is true for the other DDR-I SRAM, CY7C1323V25.

Read Operations

The CY7C1398V25 is organized internally as a 256K x 72 SRAM. Accesses are completed in a burst of four sequential 18-bit data words. Read operations are initiated by asserting R/$\overline{W}$ HIGH and $\overline{LD}$ LOW at the rising edge of the Positive Input Clock (K). The address presented to the Address inputs is stored in the Read address register and the least two significant bits of the address are presented to the burst counter. The burst counter increments the address in a linear fashion. Following the next K clock rise the corresponding 18-bit word of data from this address location is driven onto the $Q_{[17:0]}$ using C as the output timing reference. On the subsequent rising edge of $\overline{C}$ the next 18-bit data word from the address location generated by the burst counter is driven onto the $Q_{[17:0]}$. This process continues until all four 18-bit data words have been driven out onto $Q_{[17:0]}$. The requested data will be valid 1.8 ns from the rising edge of the output clock (C or $\overline{C}$, 300-MHz device). In order to maintain the internal logic, each read access must be allowed to complete. Each Read access consists of four 18-bit data words and takes two clock cycles to complete. Therefore, Read accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device will ignore the second Read request. Read accesses can be initiated on every other K clock rise. Doing so will pipeline the data flow such that data is transferred out of the device on every rising edge of the output clocks (C and $\overline{C}$ or K and $\overline{K}$ when in single clock mode).

When the read port is deselected, the CY7C1398V25 will first complete the pending read transactions. Synchronous internal circuitry will automatically three-state the outputs following the next rising edge of the Positive Output Clock (C). This will allow for a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting R/$\overline{W}$ LOW and $\overline{LD}$ LOW at the rising edge of the Positive Input Clock (K). The address presented to Address inputs is stored in the Write address register and the least two significant bits of the address are presented to the burst counter. The burst counter increments the address in a linear fashion. On the following K clock rise the data presented to $D_{[17:0]}$ is latched and stored into the 18-bit Write Data register provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the Negative Input Clock ($\overline{K}$) the information presented to $D_{[17:0]}$ is also stored into the Write Data Register provided $\overline{BWS}_{[1:0]}$ are both asserted active. This process continues for one more cycle until four 18-bit words (a total of 72 bits) of data are stored in the SRAM. The 72 bits of data are then written into the memory array at the specified location. Therefore, Write accesses to the device can not be initiated on two consecutive K clock rises. The internal logic of the device will ignore the second Write request. Write accesses can be initiated on every other rising edge of the Positive Input Clock (K). Doing so will pipeline the data flow such that 18-bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When deselected, the write port will ignore all inputs after the pending Write operations have been completed.

Byte Write Operations

Byte Write operations are supported by the CY7C1398V25. A write operation is initiated as described in the Write Operation section above. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$, which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write will allow the data being presented to be latched and written into the device. Deasserting the Byte Write Select input during the data portion of a write will allow the data stored in the device for that byte to remain unaltered. This feature can be used to simplify Read/Modify/Write operations to a Byte Write operation.

Single Clock Mode

The CY7C1398V25 can be used with a single clock that controls both the input and output registers. In this mode the device will recognize only a single pair of input clocks (K and $\overline{K}$) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/$\overline{K}$ and C/$\overline{C}$ clocks. All timing parameters remain the same in this mode. To use this mode of operation, the user must tie C and $\overline{C}$ HIGH at power-on. This function is a strap option and not alterable during device operation.

DDR Operation

The CY7C1398V25 enables high-performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation. At slower frequencies, the CY7C1398V25 requires a single No Operation (NOP) cycle when transitioning from a Read to a Write cycle. At higher frequencies, a second NOP cycle may be required to prevent bus contention.

If a Read occurs after a Write cycle, address and data for the Write are stored in registers. The write information must be stored because the SRAM can not perform the last word Write to the array without conflicting with the Read. The data stays in this register until the next Write cycle occurs. On the first Write cycle after the Read(s), the stored data from the earlier Write will be written into the SRAM array. This is called a Posted Write.

Depth Expansion

Depth expansion requires replicating the $\overline{LD}$ control signal for each bank. All other control signals can be common between banks as appropriate.

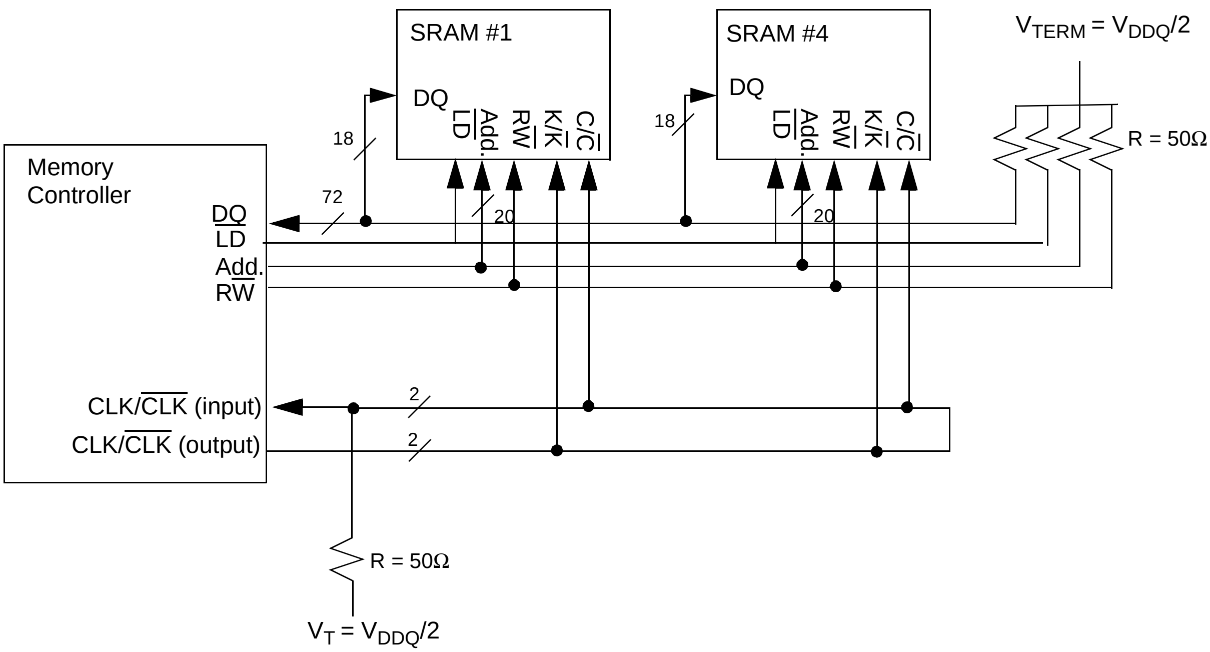
Programmable Impedance

An external resistor, RQ must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±10% is between 175Ω and 350Ω, with V_{DDQ} = 1.5V. The output impedance is adjusted every 1024 cycles to adjust for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the DDR-I to simplify data capture on high speed systems. Two echo clocks are generated by the DDR-I. CQ is referenced with respect to C and $\overline{CQ}$ is referenced with respect to $\overline{C}$. These are free-running clocks and are synchronized to the output clock of the DDR-I. In the single clock mode, CQ is generated with respect to K and $\overline{CQ}$ is generated with respect to $\overline{K}$. The timings for the echo clocks are shown in the AC Timing table.

Application Example[1]



Truth Table[2, 3, 4, 5, 6, 7]

Operation	K	LD	R/W	DQ	DQ	DQ	DQ
Write Cycle: Load address; input write data on 2 consecutive K and K rising edges.	L-H	L	L	D(A1)at K(t + 1) ↑	D(A2) at K(t + 1) ↑	D(A3) at K(t + 2) ↑	D(A4) at K(t + 2) ↑
Read Cycle: Load address; wait one cycle; read data on 2 consecutive C and C rising edges.	L-H	L	H	Q(A1) at C(t + 1)↑	Q(A2) at C(t + 1) ↑	Q(A3) at C(t + 2)↑	Q(A4) at C(t + 2) ↑
NOP: No Operation	L-H	H	X	High-Z	High-Z	High-Z)	High-Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State	Previous State	Previous State

Note:

1. The above application shows 4 of CY7C1398V25 being used. This holds true for CY7C1323V25 as well.
2. X = "Don't Care," H = Logic HIGH, L = Logic LOW ↑ represents rising edge.
3. Device will power-up deselected and the outputs in a three-state condition.
4. "A1" represents address location latched by the devices when transaction was initiated. A2, A3, and A4 represents the addresses sequence in the burst.
5. "t" represents the cycle at which a read/write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the "t" clock cycle.
6. Data inputs are registered at K and K rising edges. Data outputs are delivered on C and C rising edges, except when in single clock mode.
7. It is recommended that K = K and C = C when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

Linear Burst Address Table

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X..X00	X..X01	X..X10	X..X11
X..X01	X..X10	X..X11	X..X00
X..X10	X..X11	X..X00	X..X01
X..X11	X..X00	X..X01	X..X10

Write Cycle Descriptions[2, 8] (CY7C1398V25)

$\overline{BWS_0}$	$\overline{BWS_1}$	K	$\overline{K}$	Comments
L	L	L-H	-	During the Data portion of a Write sequence : CY7C1398V25 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	-	L-H	During the Data portion of a Write sequence : CY7C1398V25 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L-H	-	During the Data portion of a Write sequence : CY7C1398V25 – only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
L	H	-	L-H	During the Data portion of a Write sequence : CY7C1398V25 – only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
H	L	L-H	-	During the Data portion of a Write sequence : CY7C1398V25 – only the upper byte ($D_{17:9]}$) is written into the device. $D_{[8:0]}$ will remain unaltered.
H	L	-	L-H	During the Data portion of a Write sequence : CY7C1398V25 – only the upper byte ($D_{17:9]}$) is written into the device. $D_{[8:0]}$ will remain unaltered.
H	H	L-H	-	No data is written into the devices during this portion of a write operation.
H	H	-	L-H	No data is written into the devices during this portion of a write operation.

Note:

8. Assumes a Write cycle was initiated per the Write Port Cycle Description Truth Table. $\overline{BWS_0}$, $\overline{BWS_1}$ in the case of CY7C1398V25 and also $\overline{BWS_2}$, $\overline{BWS_3}$ in the case of CY7C1323V25 can be altered on different portions of a write cycle, as long as the set-up and hold requirements are achieved.

Write Cycle Descriptions[2, 8](CY7C1323V25)

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L-H	-	During the Data portion of a Write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	-	L-H	During the Data portion of a Write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L-H	-	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ will remain unaltered.
L	H	H	H	-	L-H	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
H	L	H	H	L-H	-	During the Data portion of a Write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ will remain unaltered.
H	L	H	H	-	L-H	During the Data portion of a Write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ will remain unaltered.
H	H	L	H	L-H	-	During the Data portion of a Write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ will remain unaltered.
H	H	L	H	-	L-H	During the Data portion of a Write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ will remain unaltered.
H	H	H	L	L-H		During the Data portion of a Write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ will remain unaltered.
H	H	H	L	-	L-H	During the Data portion of a Write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ will remain unaltered.
H	H	H	H	L-H	-	No data is written into the device during this portion of a write operation.
H	H	H	H	-	L-H	No data is written into the device during this portion of a write operation.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1398V25 incorporates a serial boundary scan test access port (TAP) in the FBGA package. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

Disabling the JTAP Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state that will not interfere with the operation of the device.

Test Access Port (TAP) - Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction codes). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD;

rather it performs a capture of the Input and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction that is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock inputs might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the K, $\overline{K}$, C and $\overline{C}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

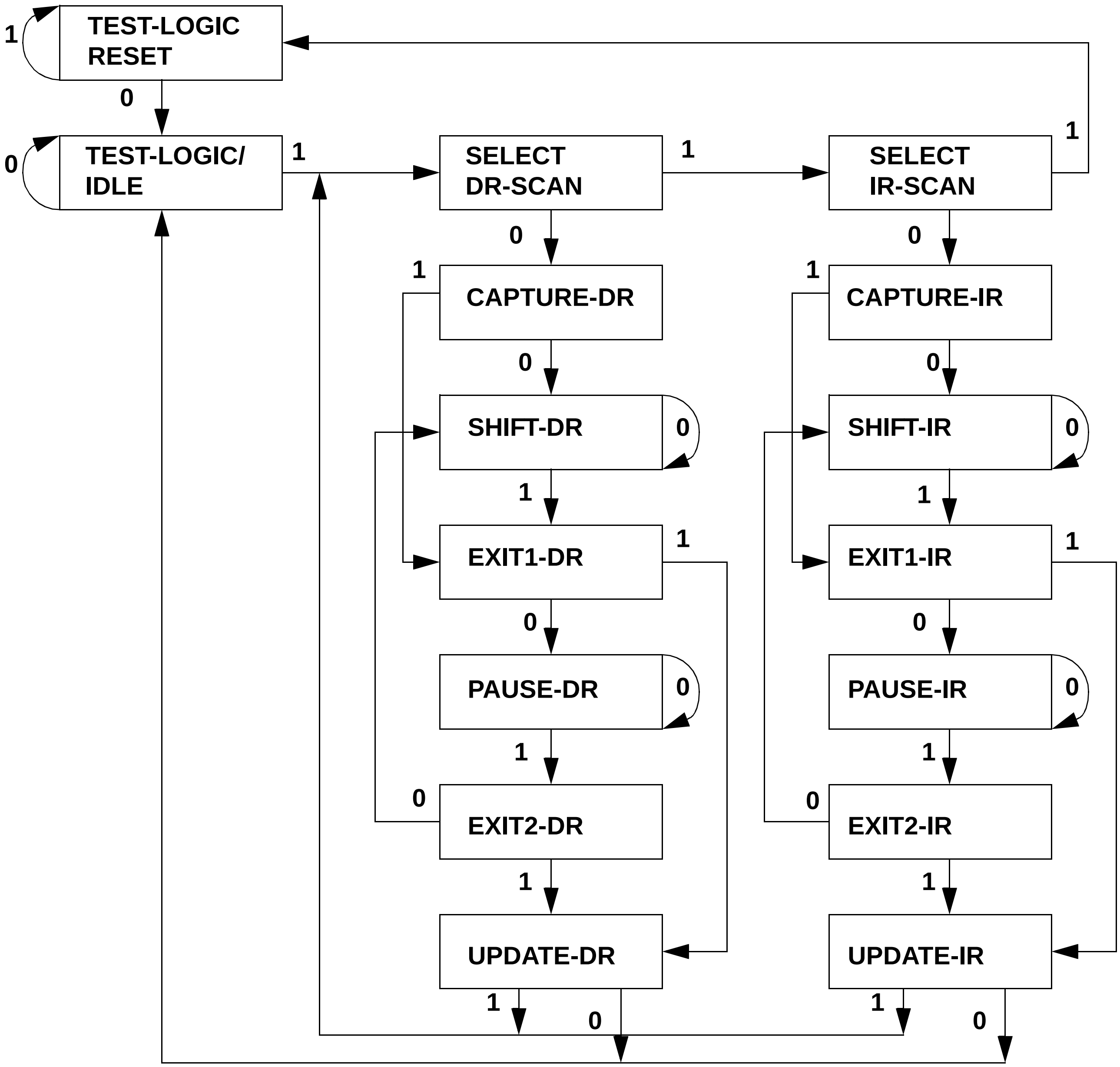
Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

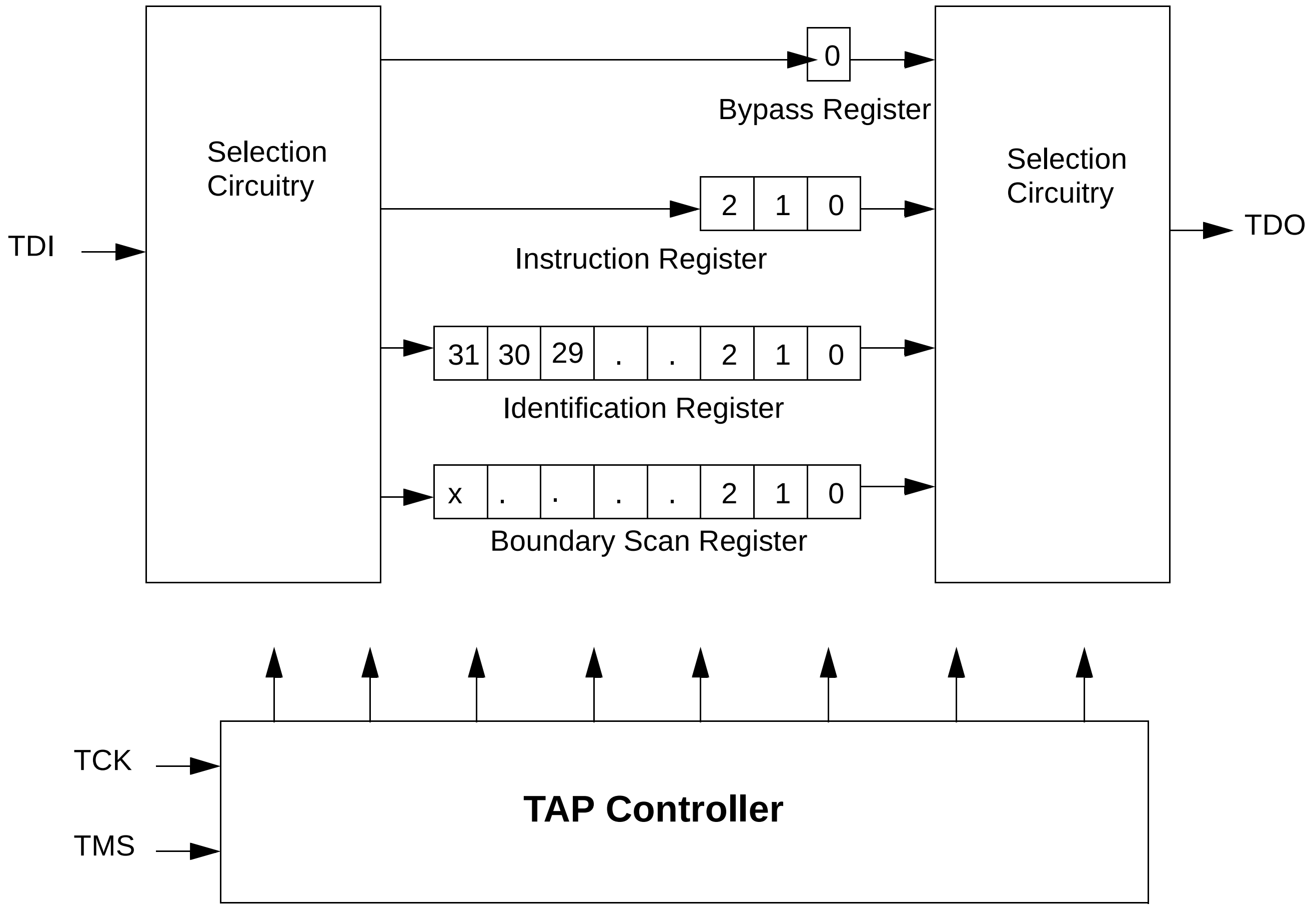
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



Note: The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[9, 10, 11]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	$I_{OH} = -2.0$ mA	1.7		V
V_{OH2}	Output HIGH Voltage	$I_{OH} = -100$ µA	2.1		V
V_{OL1}	Output LOW Voltage	$I_{OL} = 2.0$ mA		0.7	V
V_{OL2}	Output LOW Voltage	$I_{OL} = 100$ µA		0.2	V
V_{IH}	Input HIGH Voltage		1.7	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_X	Input and OutputLoad Current	$GND \leq V_I \leq V_{DDQ}$	–5	5	µA

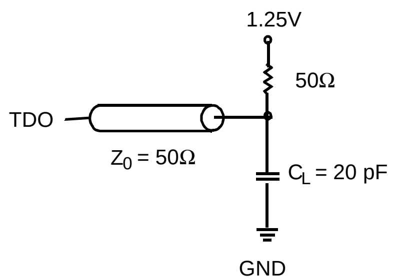
Notes:
9. All Voltage referenced to Ground.
10. Overshoot: $V_{IH}(AC) \leq V_{DD}+1.5V$ for $t \leq t_{TCYC}/2$, Undershoot $V_{IL}(AC) \leq 0.5V$ for $t \leq t_{TCYC}/2$, Power-up: $V_{IH} < 2.6V$ and $V_{DD} < 2.4V$ and $V_{DDQ} < 1.4V$ for $t < 200$ ms.
11. These characteristic pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics Table.

TAP AC Switching Characteristics Over the Operating Range[12, 13]

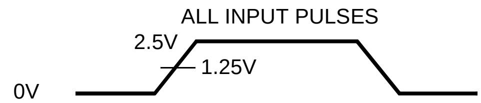
Parameter	Description	Min.	Max.	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}	Capture Set-up to TCK Rise	10		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after Clock Rise	10		ns
t_{CH}	Capture Hold after Clock Rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

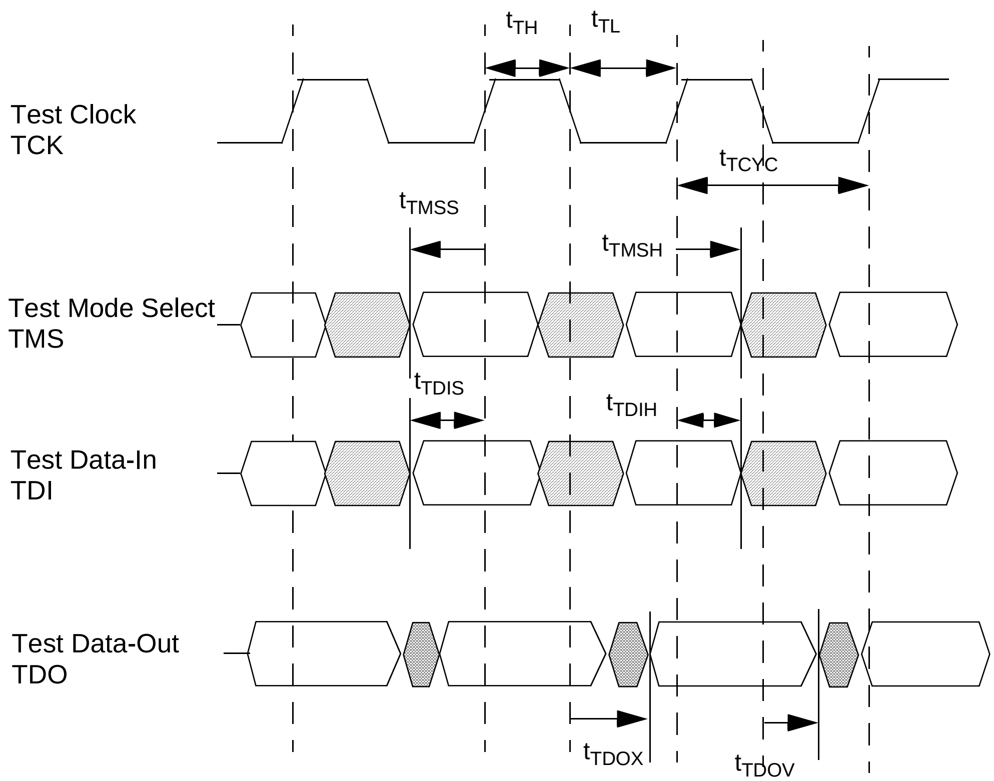
Notes:
12. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
13. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions[13]



(a)





Identification Register Definitions (To be Updated)

Instruction Field	Value	Description
	CY7CxxxxV25	
Revision Number (31:29)	000	Version number.
Cypress Device ID (28:12)	01011010011010110	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	Indicate the presence of an ID register.

Scan Register Sizes (To be Updated)

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	x

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. This instruction is not 1149.1 compliant. **The EXTEST command implemented by these devices will NOT place the output buffers into a high-Z condition. If the output buffers need to be in high-Z condition, this can be accomplished by deselecting the Read port.**
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. **The SAMPLE Z command implemented by these devices will place the output buffers into a high-Z condition.**
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement the 1149.1 preload function and is therefore not 1149.1 compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order (To be Updated)

Bit #	Signal Name	Bump ID
1	$\overline{C}$	6R
2	C	6P
3	A	6N
4	A	7P
5	A	7N
6	A	7R
7	A	8R
8	A	8P
9	A	9R
10	D0	10P
11	Q0	11P
12	D1	11N
13	Q1	10M
14	D2	11M
15	Q2	11L
16	D3	10K
17	Q3	11K
18	D4	11J
19	ZQ	11H
20	Q4	10J
21	D5	11G
22	Q5	11F
23	D6	10E
24	Q6	11E
25	D7	11D
26	Q7	10C
27	D8	11C
28	Q8	11B
29	Reserved	12A (Don’t Care)
30	GND/72M	10A
31	NC/18M(1)	9A
32	A	8B
33	A	7C
34	NC (0)	6C
35	$\overline{RPS}$	8A
36	$\overline{BWS0}$	7B

Boundary Scan Order (To be Updated)

Bit #	Signal Name	Bump ID
37	K	6B
38	$\overline{K}$	6A
39	$\overline{BWS1}$	5A
40	$\overline{WPS}$	4A
41	A	5C
42	A	4B
43	NC/36M(1)	3A
44	GND/144M	2A
45	Reserved	1A (Don’t Care)
46	D9	3B
47	Q9	2B
48	D10	3C
49	Q10	3D
50	D11	2D
51	Q11	3E
52	D12	3F
53	Q12	2F
54	D13	2G
55	Q13	3G
56	D14	3J
57	Q14	3K
58	D15	3L
59	Q15	2L
60	D16	3M
61	Q16	3N
62	D17	2N
63	Q17	3P
64	A	3R
65	A	4R
66	A	4P
67	A	5P
68	A	5N
69	A	5R

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND .... –0.5V to +3.6V

DC Voltage Applied to Outputs
in High Z State[14] .... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage[14] .... –0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA

Operating Range

Range	Ambient Temperature[15]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	1.8 ± 100 mV	1.4V to V_{DD}

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			1.7	1.9	V
V_{DDQ}	I/O Supply Voltage			1.4	V_{DD}	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, Nominal Impedance		V_{DDQ} – 0.2	V_{DDQ}	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA, Nominal Impedance		V_{SS}	0.2	V
V_{IH}	Input HIGH Voltage			V_{REF} + 0.1	V_{DDQ} + 0.3	V
V_{IL}	Input LOW Voltage[14]			–0.3	V_{REF} – 0.1	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
V_{REF}	Input Reference Voltage[16]	Typical Value = 0.75V		0.68	0.95	V
I_{DD}	V_{DD} Operating Supply x8, x18	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	167 MHz		TBD	mA
			200 MHz		TBD	mA
			250 MHz		TBD	mA
			300 MHz		TBD	mA
I_{DD}	V_{DD} Operating Supply x36	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	167 MHz		TBD	mA
			200 MHz		TBD	mA
			250 MHz		TBD	mA
			300 MHz		TBD	mA
I_{SB1}	Automatic Power-Down Current, x8, x18	Max. V_{DD}, Both Ports Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC}, Inputs Static	167 MHz		TBD	mA
			200 MHz		TBD	mA
			250 MHz		TBD	mA
			300 MHz		TBD	mA
I_{SB1}	Automatic Power-Down Current, x36	Max. V_{DD}, Both Ports Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC}, Inputs Static	167 MHz		TBD	mA
			200 MHz		TBD	mA
			250 MHz		TBD	mA
			300 MHz		TBD	mA

Note:

14. Minimum voltage equals –0.9V for pulse duration less than 20 ns.
15. T_A is the case temperature.
16. V_{REF} Min. = 0.68V or 0.46V_{DDQ}, whichever is larger, V_{REF} max = 0.95V or 0.54V_{DDQ}, whichever is smaller.

Switching Characteristics Over the Operating Range[18]

Parameter	Description	300		250		200		167		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	K Clock and C Clock Cycle Time	3.3	4.0	4.0	5.0	5.0	6.0	6.0	7.5	ns
t_{KH}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH	1.3	-	1.6	-	2.0	-	2.4	-	ns
t_{KL}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) LOW	1.3	-	1.6	-	2.0	-	2.4	-	ns
t_{KHKH}	K/$\overline{K}$ Clock Rise to $\overline{K}$/K Clock Rise and C/$\overline{C}$ to C/$\overline{C}$ Rise (rising edge to rising edge)	1.55	1.75	1.9	2.1	2.4	2.6	2.8	3.2	ns
t_{KHCH}	K/$\overline{K}$ Clock Rise to C/$\overline{C}$ Clock Rise (rising edge to rising edge)	0.0	0.8	0.0	1.0	0.0	1.5	0.0	2.0	ns
Set-up Times										
t_{SA}	Address Set-up to K Clock Rise	0.4	-	0.5	-	0.6	-	0.7	-	ns
t_{SC}	Control Set-up to Clock (K, $\overline{K}$, C, $\overline{C}$) Rise (R/$\overline{W}$, $\overline{LD}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.4	-	0.5	-	0.6	-	0.7	-	ns
t_{SD}	$D_{[17:0]}$ Set-up to Clock (K and $\overline{K}$) Rise	0.4	-	0.5	-	0.6	-	0.7	-	ns
Hold Times										
t_{HA}	Address Hold after Clock (K and $\overline{K}$) Rise	0.4	-	0.5	-	0.6	-	0.7	-	ns
t_{HC}	Control Hold after Clock (K and $\overline{K}$) Rise (R/$\overline{W}$, $\overline{LD}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.4	-	0.5	-	0.6	-	0.7	-	ns
t_{HD}	$D_{[17:0]}$ Hold after Clock (K and $\overline{K}$) Rise	0.4	-	0.5	-	0.6	-	0.7	-	ns
Output Times										
t_{CO}	C/$\overline{C}$ Clock Rise (or K/$\overline{K}$ in single clock mode) to Data Valid[17]	-	1.8	-	2.2	-	2.4	-	3.0	ns
t_{DOH}	Data Output Hold after Output C/$\overline{C}$ Clock Rise (Active to Active)	0.8	-	0.8	-	0.8	-	0.8	-	ns
t_{CCQO}	C/$\overline{C}$ Clock Rise to Echo Clock Valid	0.8	2.0	0.8	2.4	0.8	2.6	0.8	3.2	ns
t_{CQD}	Echo Clock (CQ/$\overline{CQ}$) Rise to Data Valid	-	0.25	-	0.30	-	0.35	-	0.40	ns
t_{CQOH}	Echo Clock (CQ/$\overline{CQ}$) Rise to Data Hold	–0.25	-	–0.30	-	–0.35	-	–0.40	-	ns
t_{CLZ}	C Clock Rise to Low-Z[18, 19]	0.8	-	0.8	-	0.8	-	0.8	0.8	ns
t_{CHZ}	C Clock Rise to High-Z (Active to High-Z)[18, 19]	-	1.8	-	2.2	-	2.4	-	3.0	ns
DLL Timing										
t_{KC}	Clock Phase Jitter	-	0.08	-	0.10	-	0.13		0.15	ns
$t_{KC\ lock}$	DLL Lock Time (K, C)	1024	-	1024	-	1024	-	1024	-	Cls

Notes:

17. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75V, V_{REF} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC test loads.
18. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 100 mV from steady-state voltage.
19. At any given voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.

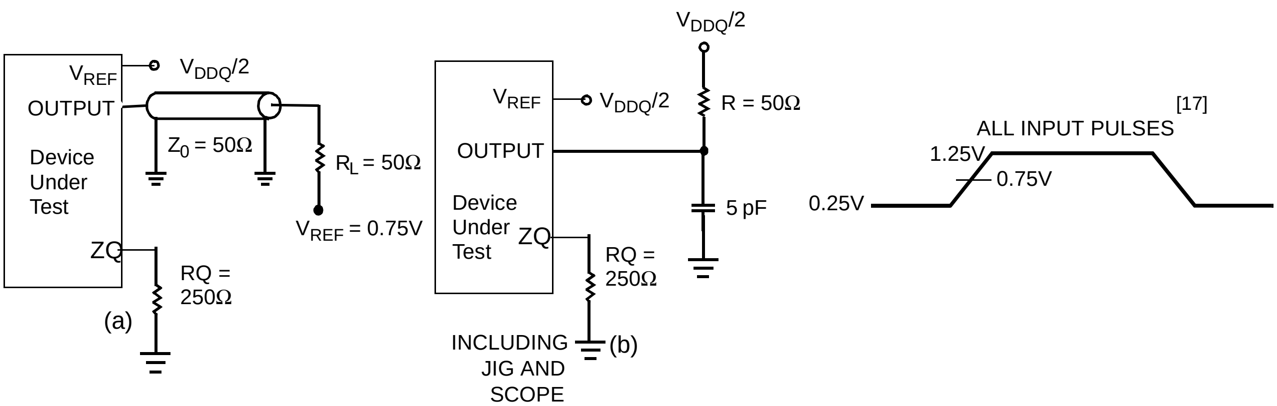
Capacitance[20]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 2.5V V_{DDQ} = 1.5V	TBD	pF
C_{CLK}	Clock Input Capacitance		TBD	pF
C_O	Output Capacitance		TBD	pF

Note:

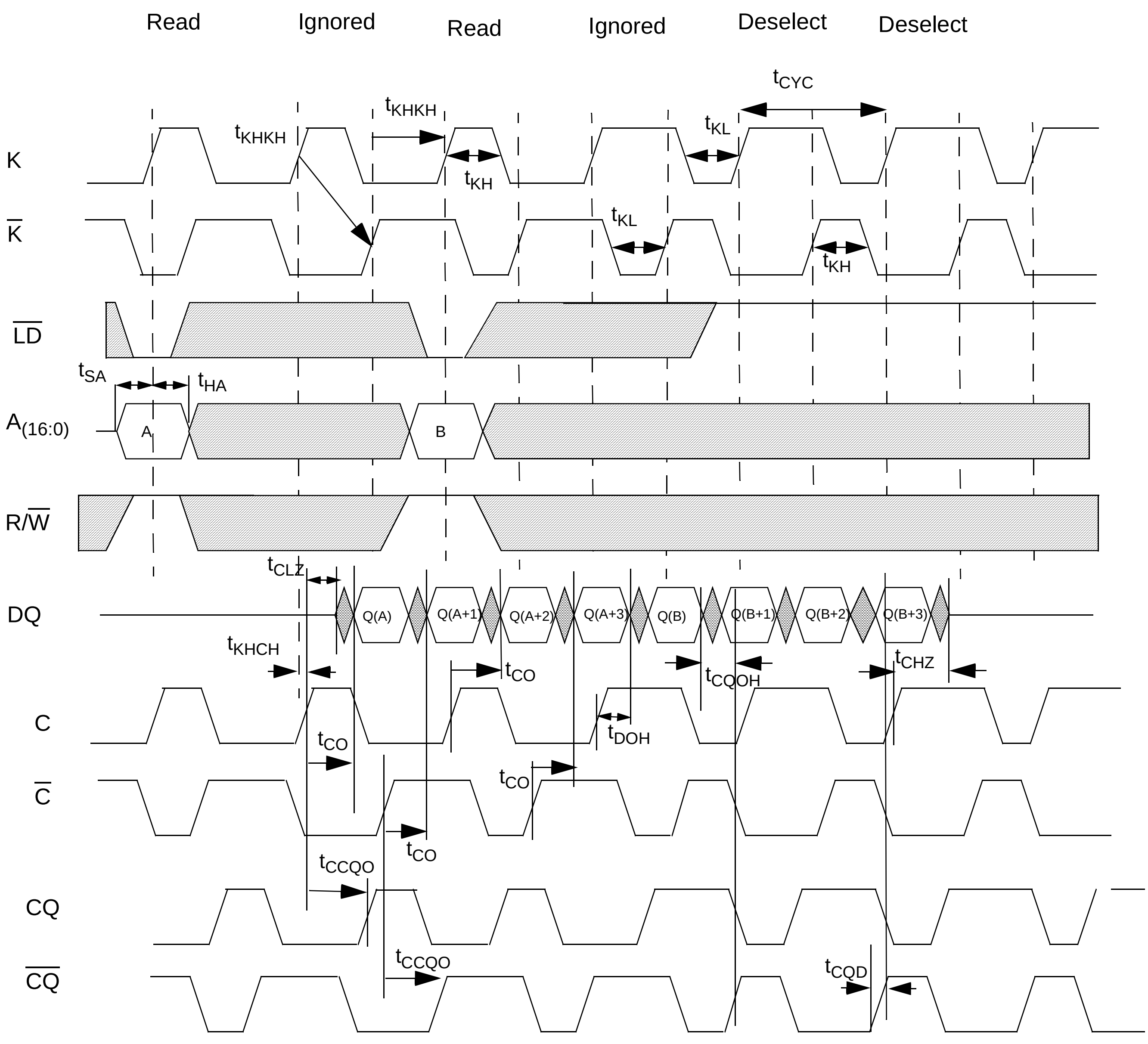
20. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms



Switching Waveforms

Read/Deselect Sequence

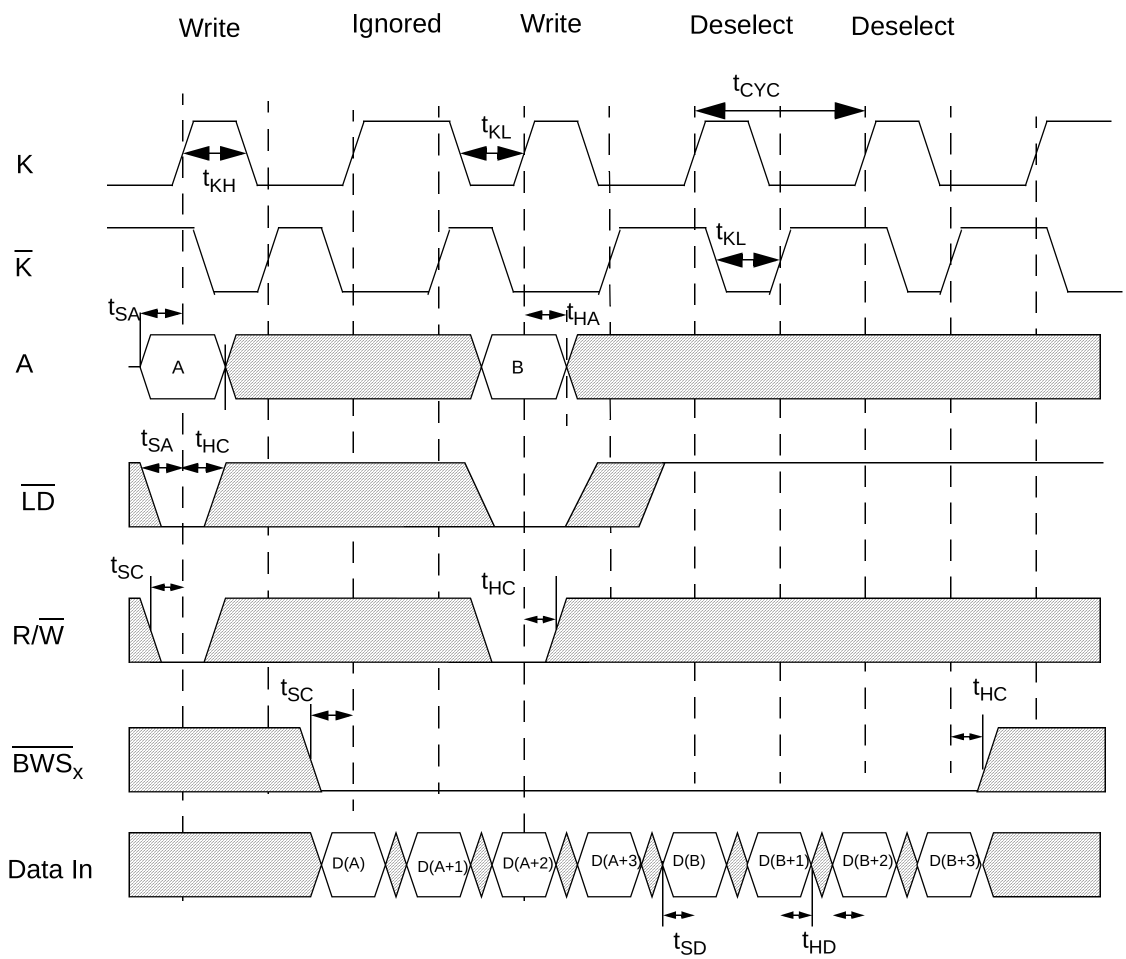


Device originally deselected. Activity on the Write Port is unknown.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

Write/Deselect Sequence

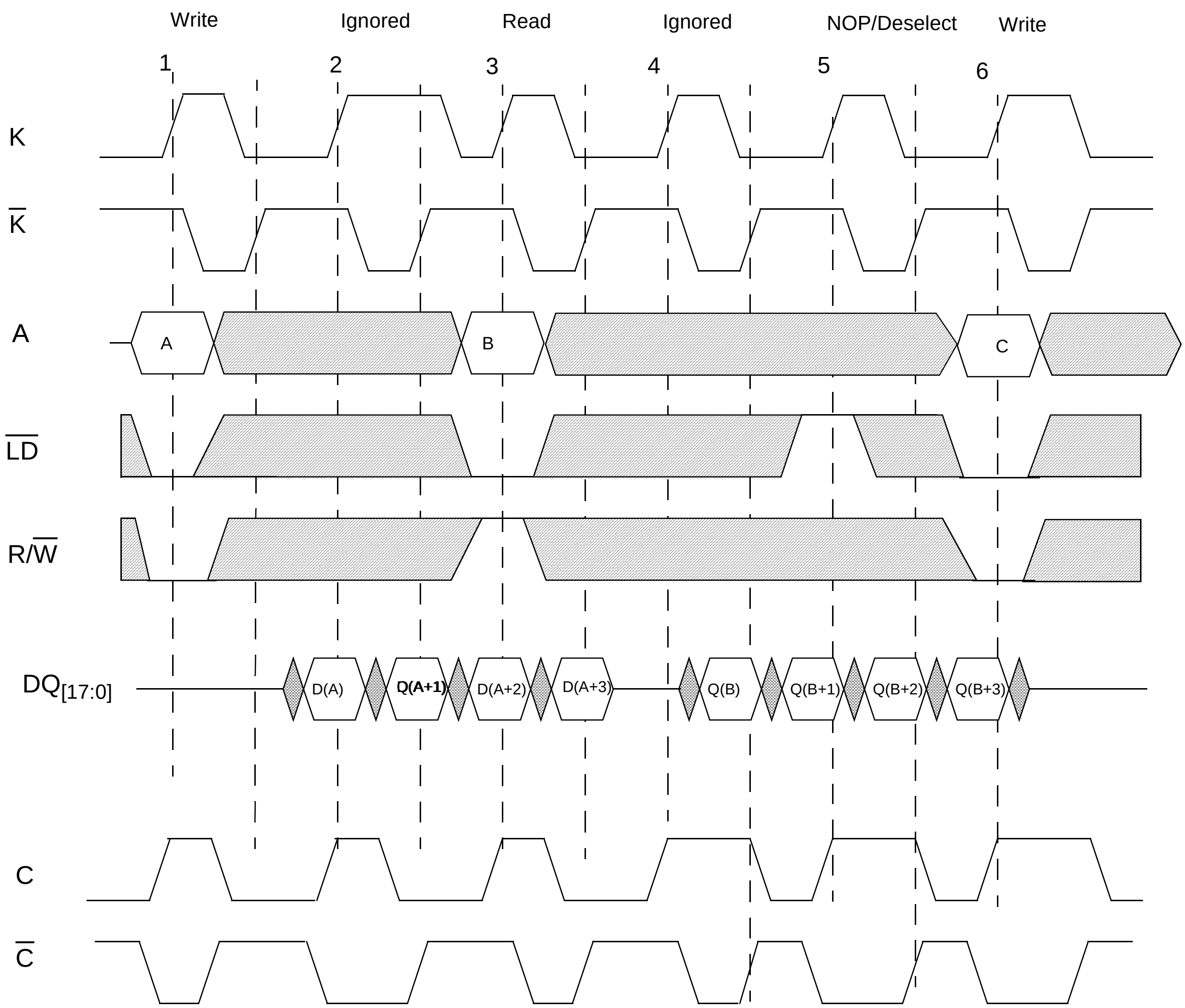


C and $\overline{C}$ reference to Data Outputs and do not affect Write operations.
Activity on the Read Port is unknown.
$\overline{BWS_x}$ LOW=Valid, Byte writes allowed, see Byte write table for details.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

Read/Write/Deselect Sequence



Read Port previously deselected.
$\overline{BWS_x}$ assumed active.

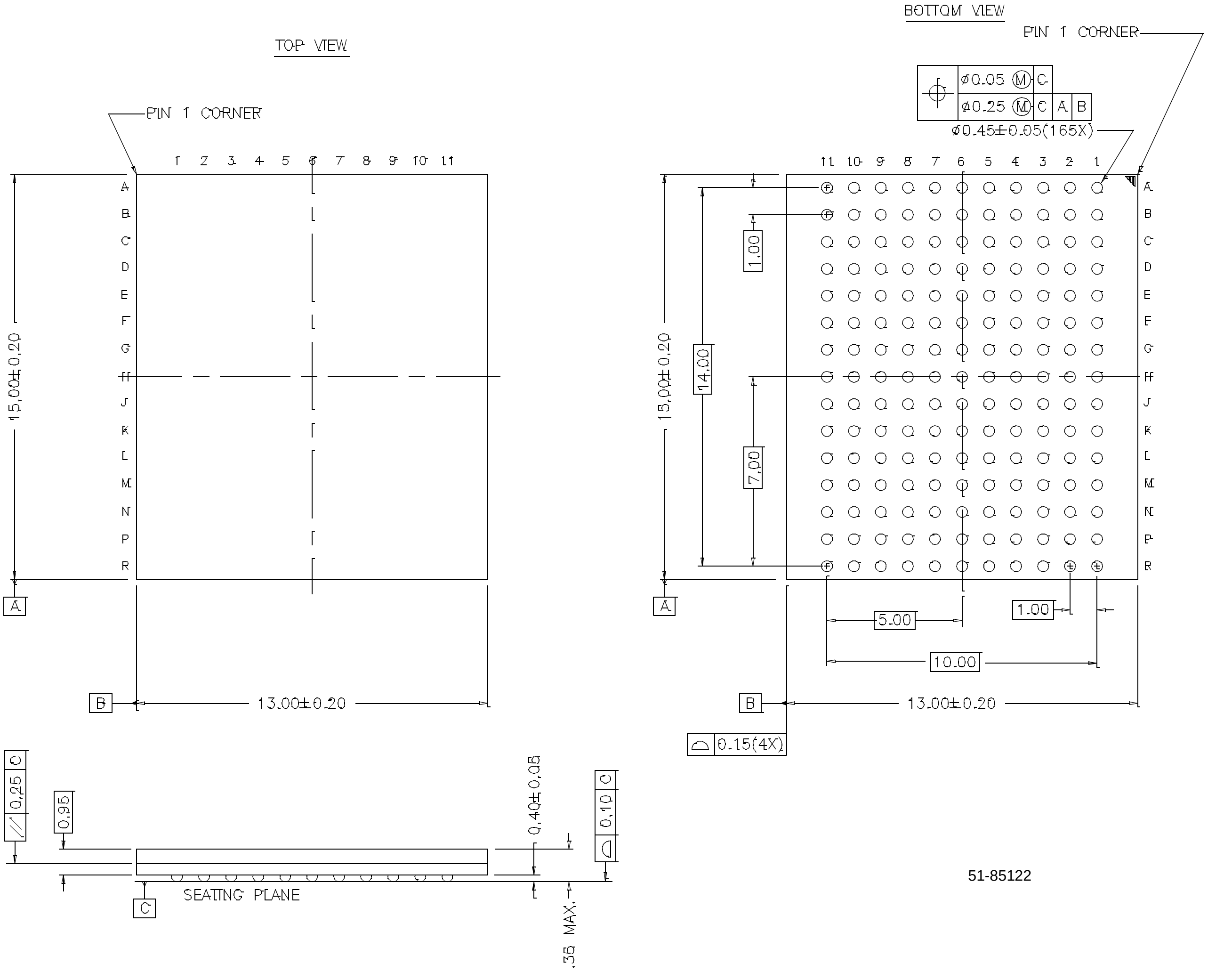
= DON'T CARE = UNDEFINED

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
300	CY7C1317V18-300BZC	BB165	13 x 15 mm FBGA	Commercial
250	CY7C1317V18-250BZC			
200	CY7C1317V18-200BZC			
167	CY7C1317V18-167BZC			
300	CY7C1319V18-300BZC	BB165	13 x 15 mm FBGA	Commercial
250	CY7C1319V18-250BZC			
200	CY7C1319V18-200BZC			
167	CY7C1319V18-167BZC			
300	CY7C1321V18-300BZC	BB165	13 x 15 mm FBGA	Commercial
250	CY7C1321V18-250BZC			
200	CY7C1321V18-200BZC			
167	CY7C1321V18-166BZC			

Package Diagram

165-Ball FBGA (13 x 15 x 1.35 mm) BB165



51-85122

Revision History

Document Title: CY7C1398V25/CY7C1323V25 18-Mb 4-Word Burst SRAM with DDR-I Architecture Document Number: 38-05176				
REV.	ECN NO.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
**	110855	11/09/01	SKX	New Data Sheet