256K x 24 Static RAM Module

Features

- **High-density 6-Megabit SRAM Module**
- **High-speed CMOS SRAMs**
  - **t_{AA} = 10 ns**
- **Single 3.3V power supply**
- **Low active power(648 W at 10 ns)**
- **TTL-compatible Inputs and Outputs**
- **Available in standard 119-ball BGA**

Functional Description

The CYM26KAH24AV33 is a 3.3V high-performance 6-Megabit static RAM organized as a 256K words by 24 bits. This module is constructed from two SRAM dies mounted on a multilayer laminate substrate combined to form a 24-bit SRAM.

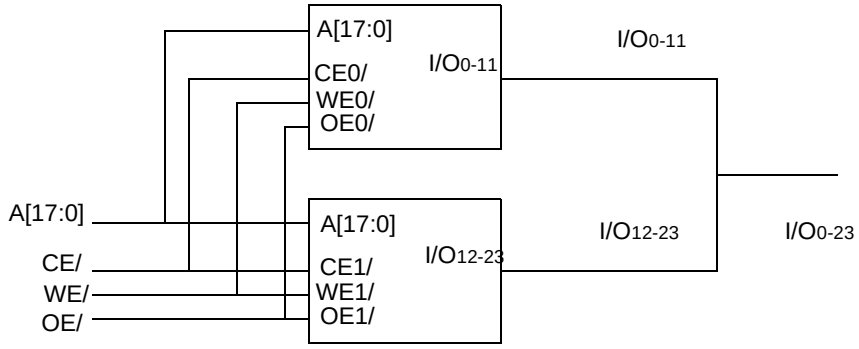
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data from I/O pins (I/O_0 through I/O_{23}), is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Then data from the memory location specified by the address pins will appear on I/O_0 to I/O_{23}. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_{23}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$HIGH), and the outputs are disabled ($\overline{OE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CYM26KAH24AV33 is available in a standard 119 BGA.

Functional Block Diagram



Selection Guide

		-10	-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Commercial	180	170	mA
	Industrial	200	190	mA
Maximum Standby Current	Commercial Industrial	20	20	mA

Pin Configurations

119 BGA
Top View

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	$\overline{CE}$	A	A	NC
C	I/O12	NC	NC[1]	A	NC[1]	NC	I/011
D	I/O13	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O10
E	I/O14	NC	V_{CC}	V_{SS}	V_{CC}	NC	I/O9
F	I/O15	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O8
G	I/O16	NC	V_{CC}	V_{SS}	V_{CC}	NC	I/O7
H	I/O17	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O6
J	V_{CC}	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	V_{DD}
K	I/O18	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O5
L	I/O19	NC	V_{CC}	V_{SS}	V_{CC}	NC	I/O4
M	I/O20	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O3
N	I/O21	NC	V_{CC}	V_{SS}	V_{CC}	NC	I/O2
P	I/O22	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O1
R	I/O23	NC	NC	NC	NC	NC	I/O0
T	NC	A	A	$\overline{WE}$	A	A	NC
U	NC	A	A	$\overline{OE}$	A	A	NC

Note:
1. Bumps 3C and 5C are actually NC's but they should be wired 3C to V_{CC} and 5C to Vss to assure compatibility with future versions.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied .. –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] ..... –0.5V to 4.6V

DC Voltage Applied to Outputs in High-Z State[2] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±5%
Industrial	–40°C to +85°C	3.3V ±5%

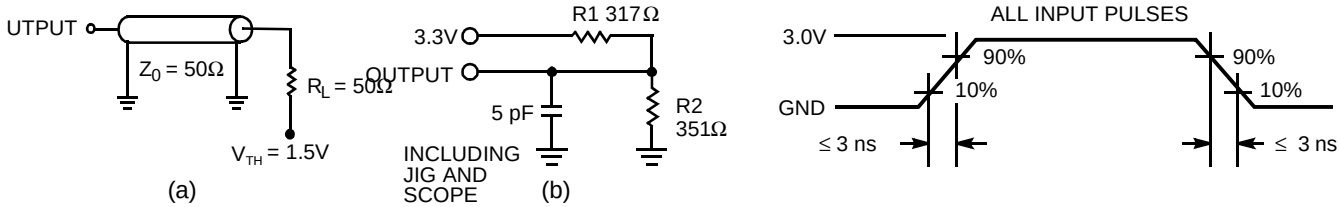
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–2	+2	-2	+2	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–2	+2	-2	+2	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. f = f_{MAX} = $1/t_{RC}$	Commercial		180		170	mA
			Industrial		200		190	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			80		80	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Commercial/ Industrial		20		20	mA

Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	10	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms



Note:

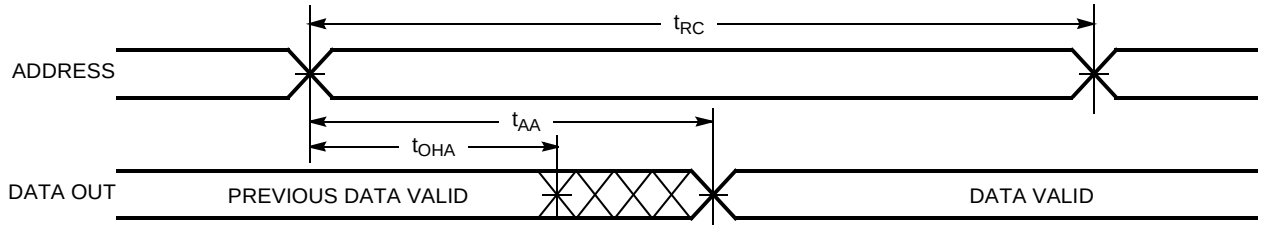
2. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.

AC Switching Characteristics[3] Over the Operating Range

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ active to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[4, 5]		5		6	ns
t_{LZCE}	$\overline{CE}$ active to Low Z[5]	3		3		ns
t_{HZCE}	$\overline{CE}$ inactive to High Z[4, 5]		5		6	ns
t_{PU}	$\overline{CE}$ active to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ inactive to Power-Down		10		12	ns
Write Cycle[6, 7]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ active to Write End	7		8		ns
t_{AW}	Address Set-Up to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Set-Up to Write End	5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4, 5]		4		5	ns

Switching Waveforms

Read Cycle No. 1[8, 9]

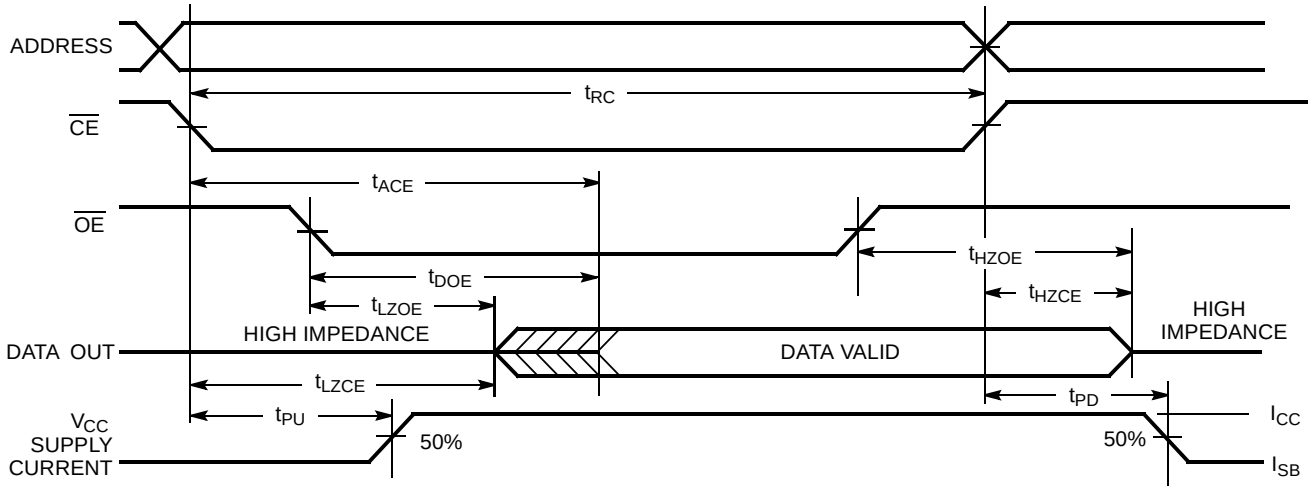


Notes:

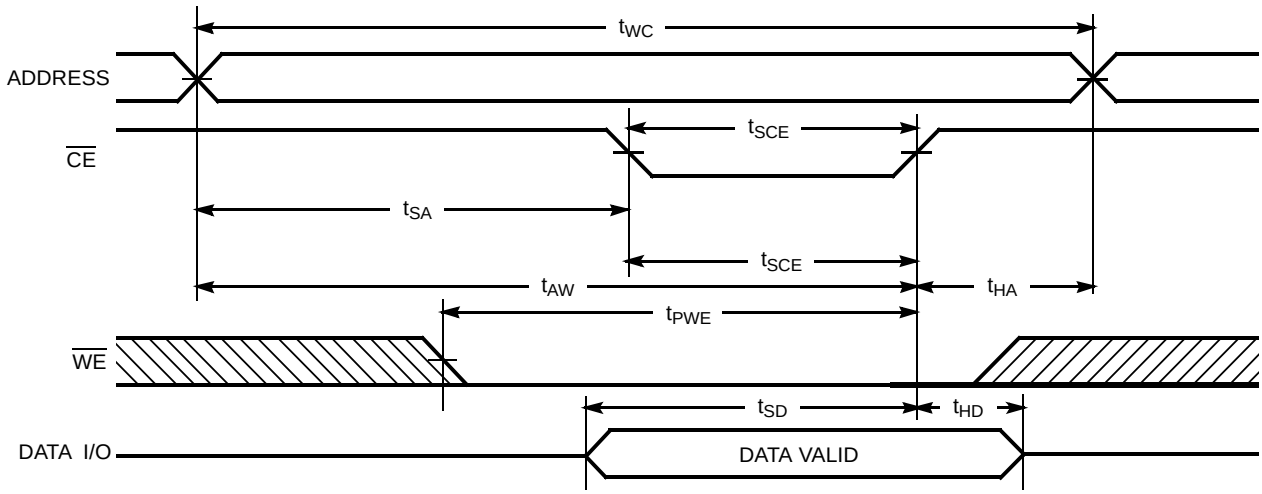
3. Tested initially and after any design or process changes that may affect these parameters.
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}.
5. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
9. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]



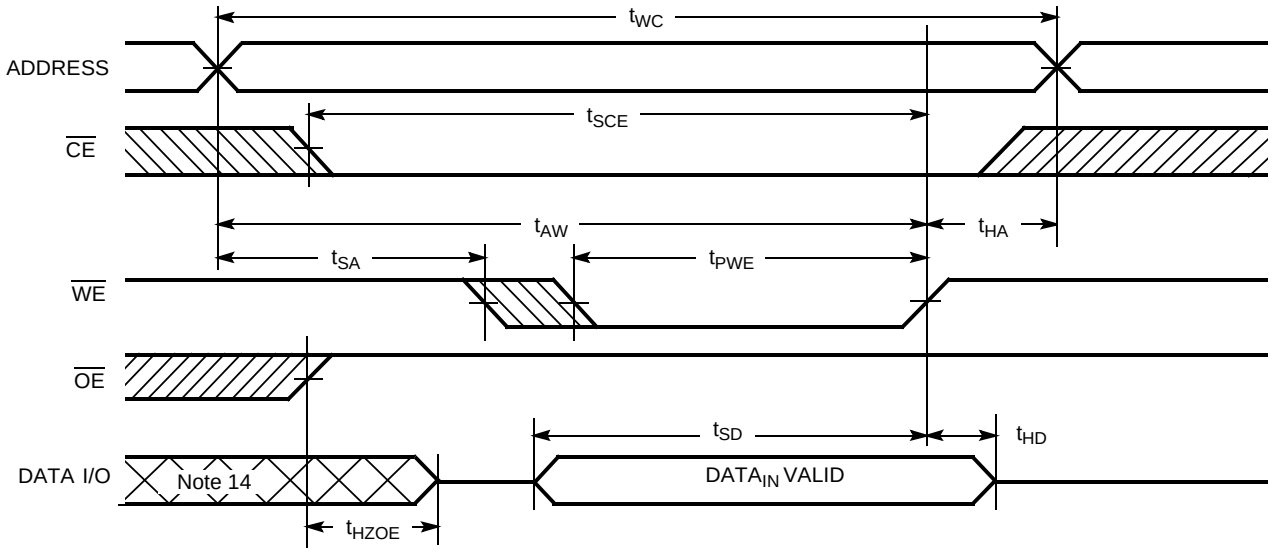
Write Cycle No. 1 ($\overline{CE}$ Controlled)[12, 13]



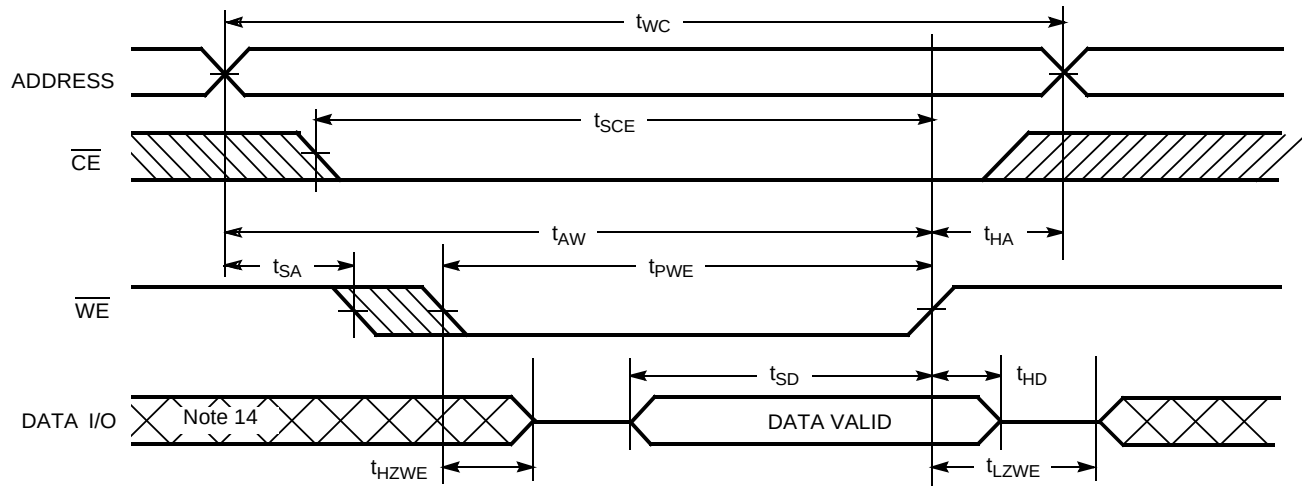
Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



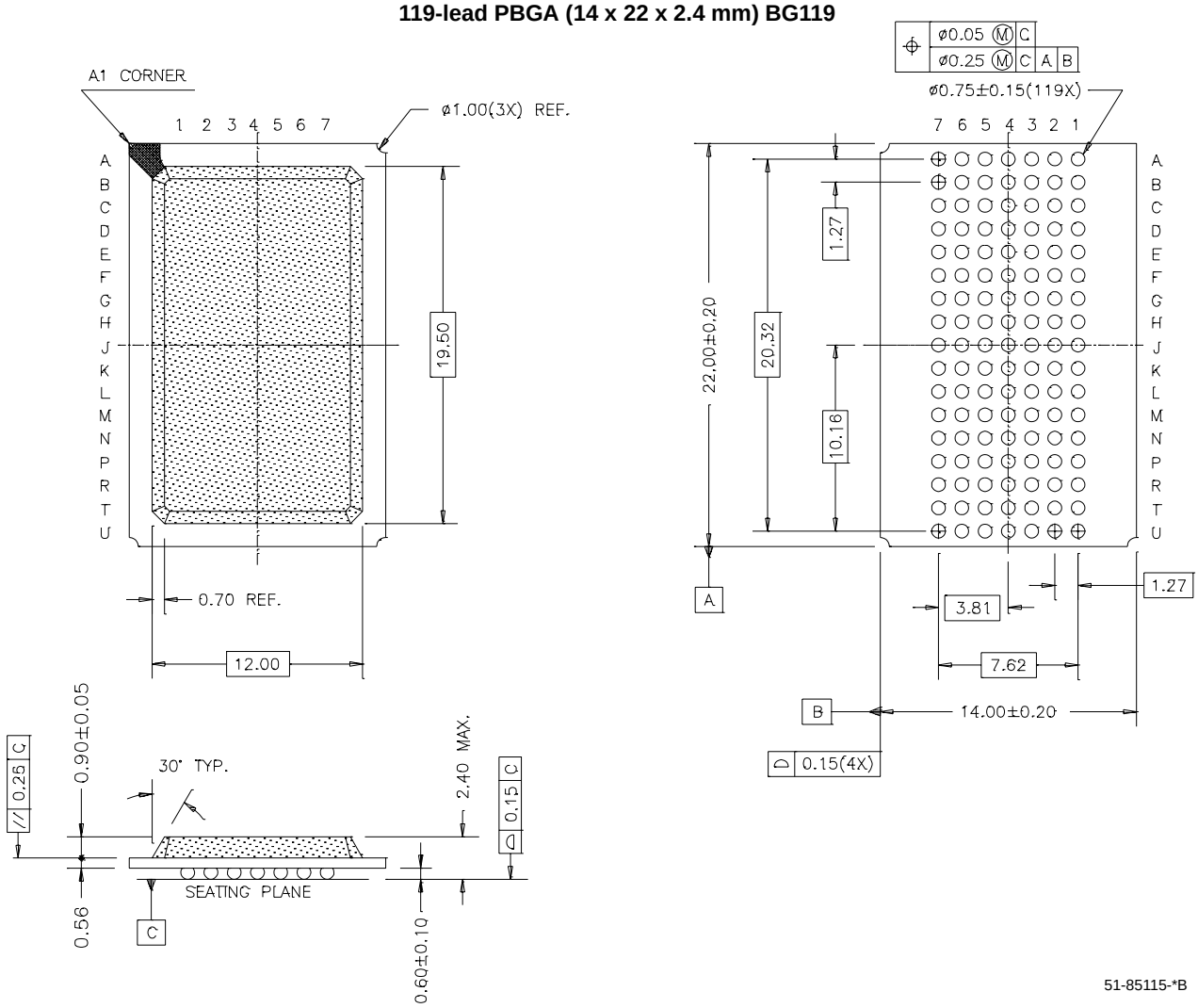
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CYM26KAH24AV33-10BGC	BG119	119-Ball BGA	Commercial
10	CYM26KAH24AV33-10BGI	BG119	119-Ball BGA	Industrial
12	CYM26KAH24AV33-12BGC	BG119	119-Ball BGA	Commercial
12	CYM26KAH24AV33-12BGI	BG119	119-Ball BGA	Industrial

Note:
14. During this period the I/Os are in the output state and input signals should not be applied.

Package Diagram

119-lead PBGA (14 x 22 x 2.4 mm) BG119



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Document History Page

Document Title: CYM26KAH24AV33 256K x 24 Static RAM Module Document Number: 38-05324				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	123014	01/22/03	CS	New Data Sheet