DAC0890

DAC0890 Dual 8-bit MuP-Compatible Digital-to-Analog Converter

Literature Number: SNAS065A

National Semiconductor

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DAC0890
Dual 8-bit μP-Compatible Digital-to-Analog Converter

General Description

The DAC0890 is a complete dual 8-bit voltage output digital-to-analog converter that can operate on a single 5V supply. It includes on-chip output amplifiers, precision bandgap voltage reference, and full microprocessor interface.

Each DAC0890 output amplifier has two externally selectable output ranges, 0V to 2.55V and 0V to 10.2V. The amplifiers are internally trimmed for offset and full-scale accuracy and therefore require no external user trims.

The DAC0890 is supplied in 20-pin ceramic DIP package.

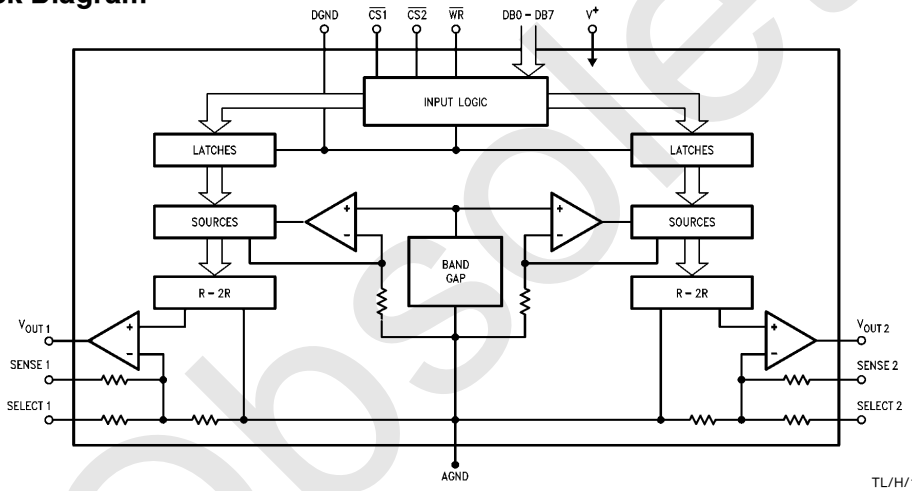
Features

- Two 8-bit voltage output DACs
- 4.75V to 16.5V single operation
- Guaranteed monotonic over temperature
- Internal precision bandgap reference
- Two calibrated output ranges; 2.55V and 10.2V
- 2 μs settling time for full-scale output change
- No external trims
- Microprocessor interface

Applications

- Industrial processing controls
- Automotive controls
- Disk drive motor controls
- Automatic test equipment

Block Diagram



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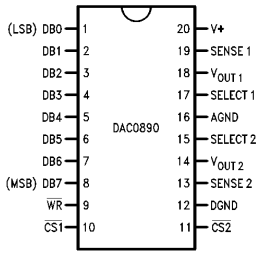
Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
DAC0890CIJ	J20A Cerdip

Connection Diagram

Dual-In-Line Package



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Top View

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage (V^+)	20V
Voltage at Any Pin (Note 3)	GND -0.3 to $V^+ +0.3$V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 4)	20 mA
Power Dissipation (Note 5)	1.0W
ESD Susceptability (Note 6)	2000V
Output Short-Circuit Protection Duration	Indefinite
Soldering Information	
J package (10 sec.)	300°C
Storage Temperature	-65°C to 150°C
Junction Temperature	(Note 5)

Operating Ratings (Notes 1 & 2)

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	
DAC0890CIJ	-40°C $\le T_A \le +85$°C
Positive Supply Voltage, V^+	4.75 to 16.5V

Electrical Characteristics

The following specifications apply for $V^+ = +5$V and $V^+ = +15$V and AGND = DGND = 0V, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25$°C.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units
	Resolution			**8**	Bits(min)
	Monotonicity			**8**	Bit(min)
	Integral Linearity Error		± 0.16	$\pm$**0.5**	LSB(min)
	Fullscale Error			$\pm 1.5/\pm$**2.5**	LSB(max)
	Zero Error			$\pm 1.0/\pm$**2.0**	LSB(max)
	Full Scale DAC-to-DAC Tracking (Note 9)		$\pm$**0.25**		LSB
	Analog Crosstalk (Note 10)	$V^+ = 15$V, 10.2V range $V^+ = 5$V, 2.55V range	-74 -66		dB dB
	Glitch Energy (Note 11)		45		V-ns
	Digital Feedthrough (Note 12)		60		V-ns
t_S	Positive Output Settling Time (Note 13)	$C_{LOAD} \le 500$ pF $C_{LOAD} \le 1000$ pF	2 3		μs μs
I_O	Output Current Drive Capability	(Note 14)	8	5/**3.5**	mA(min)
I_{SC}	Output Short Circuit Current (Note 15)	$V^+ = 15$V	20		mA
PSRR	Power Supply Rejection Ratio (Note 16)	f < 30 Hz 10.2V range $13.5\text{V} \le V^+ \le 16.5$V	7	**15**	ppm/% (max)
		2.55V range $13.5\text{V} \le V^+ \le 16.5$V $4.75\text{V} \le V^+ \le 5.25$V $4.75\text{V} \le V^+ \le 16.5$V	 4 4 4	 **59** **20** 	 ppm/% (max) ppm/% (max) ppm/%
I_S	Supply Current	All Inputs Low $V^+ = 16.5$ $V^+ = 4.75$	 25 23	 30/**35**	 mA (max) mA
V_{ILD}	Data Logic Low Threshold			**0.8**	V (max)
V_{IHD}	Data Logic High Threshold			**2.0**	V (min)
V_{ILC}	Control Logic Low Threshold			**0.8**	V (max)

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$ and $V^+ = +15V$ and AGND = DGND = 0V, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units
V_{IHC}	Control Logic High Threshold			**2.2**	V (min)
	Digital Input Current	(Note 17)	2.2	**25**	μA (max)
t_{WR}	Write Time		18	40	ns (min)
t_{DS}	Data Setup Time		18	35	ns (min)
t_{DH}	Data Hold Time		3		ns (max)
t_{CS}	Control Setup Time		18	40	ns (min)
t_{CH}	Control Hold Time			**0**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to AGND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < AGND$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less.

Note 4: The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The T_{JMAX}(°C) and θ_{JA}(°C/W) for the DAC0890ClJ are 125°C and 53°C/W, respectively.

Part Number	T_{JMAX}(°C)	θ_{JA}(°C/W)
DAC0890ClJ	125	53

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at 25°C, unless otherwise specified, and represent the most likely parametric norm.

Note 8: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Full Scale DAC-to-DAC Tracking is defined as the change in the voltage difference between the full scale output levels of DAC1 and DAC2. The result is expressed in LSBs and it referred to the full-scale voltage difference at 25°C.

Note 10: Analog Crosstalk is a measure of the change in one DAC's full scale output voltage as the second DAC's output voltage changes value. It is measured as the voltage change in one DAC's full scale output voltage divided by the voltage range through which the second DAC's output has changed (zero to full scale). This ratio is then expressed in dB.

Note 11: Glitch Energy is a worst case measurement, over the entire input code range, of transients that occur when changing code. The positive and negative areas of the transient waveforms are summed together to obtain the value listed.

Note 12: Digital Feedthrough is measured with both DAC outputs latched at full scale and a 2 ns, 5V step applied to all 8 data inputs. This gives the worst case digital feedthrough for the DAC0890.

Note 13: Settling Time is specified for a positive full scale step to ±½ LSB. Settling time for negative steps will be slower but may be improved with an external pull-down resistor. Negative settling time to ±½ LSB can be calculated for each range where $t_S = 6.23\ (C_{LOAD})\ (R_{LOAD}/10\ k\Omega)$ for the high range and $t_S = 6.23\ (C_{LOAD})\ (R_{LOAD}/2.5\ k\Omega)$ for the low range.

Note 14: Output Current Drive Capability is the minimum current that can be sourced by the output amplifiers with less than ½ LSB reduction in full scale. Current sinking capability is provided by a passive internal resistance of 10 kΩ in the high range and 2.5 kΩ in the low range.

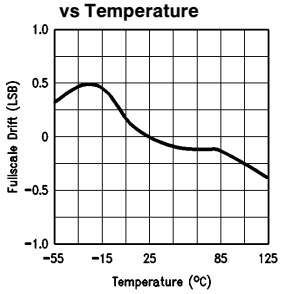
Note 15: Output Short Circuit Current is measured with the output at full-scale and shorted to AGND.

Note 16: Power Supply Rejection Ratio is a measure of how much the output voltage changes (in parts-per-million) per change (in percent) in the power supply voltage.

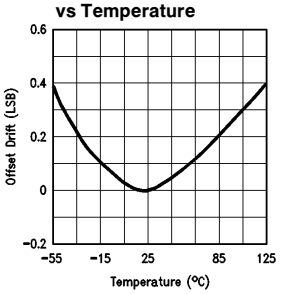
Note 17: Digital Input Current is measured with 0V and V^+ input levels. The limit specified is the higher of these two measurements.

Typical Performance Characteristics

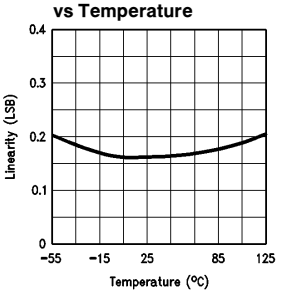
Fullscale Drift vs Temperature



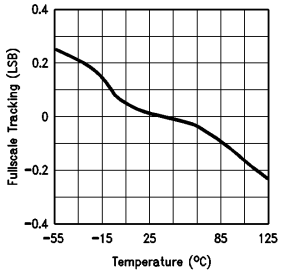
Offset Drift vs Temperature



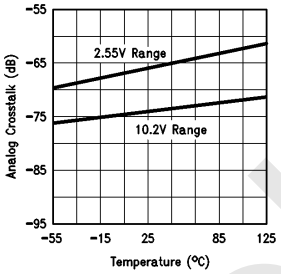
Integral Linearity vs Temperature



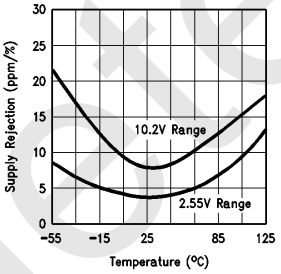
Fullscale Dac to Dac Tracking vs Temperature



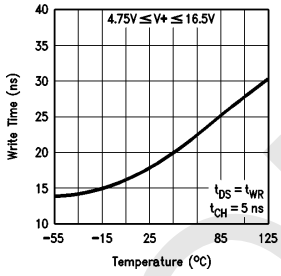
Analog Crosstalk vs Temperature



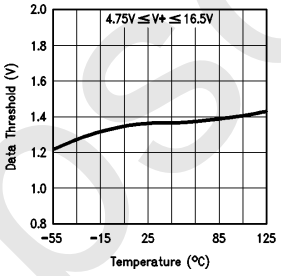
Power Supply Rejection vs Temperature



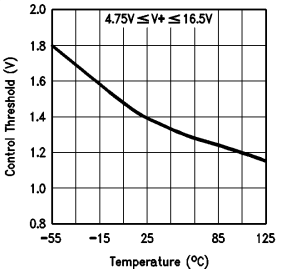
Write Time vs Temperature



Data Threshold vs Temperature



Control Threshold vs Temperature



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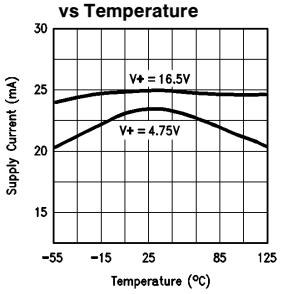
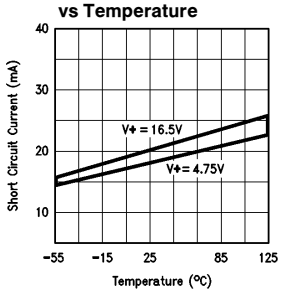
Typical Performance Characteristics

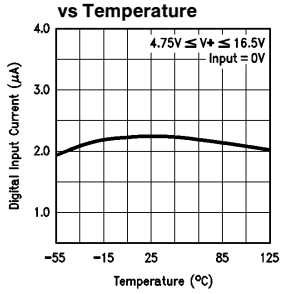
Supply Current vs Temperature



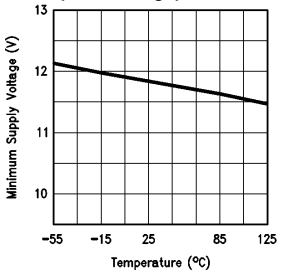
Short Circuit Current vs Temperature



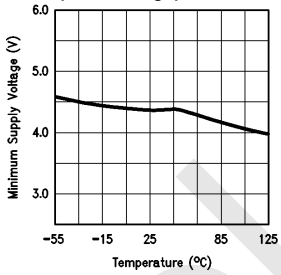
Digital Input Current vs Temperature



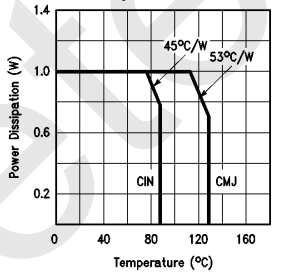
Minimum Supply Voltage vs Temperature (10.2V Range)



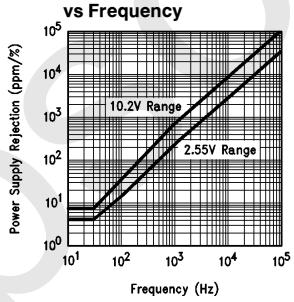
Minimum Supply Voltage vs Temperature (2.55V Range)



Max Power Dissipation vs Temperature



Power Supply Rejection vs Frequency



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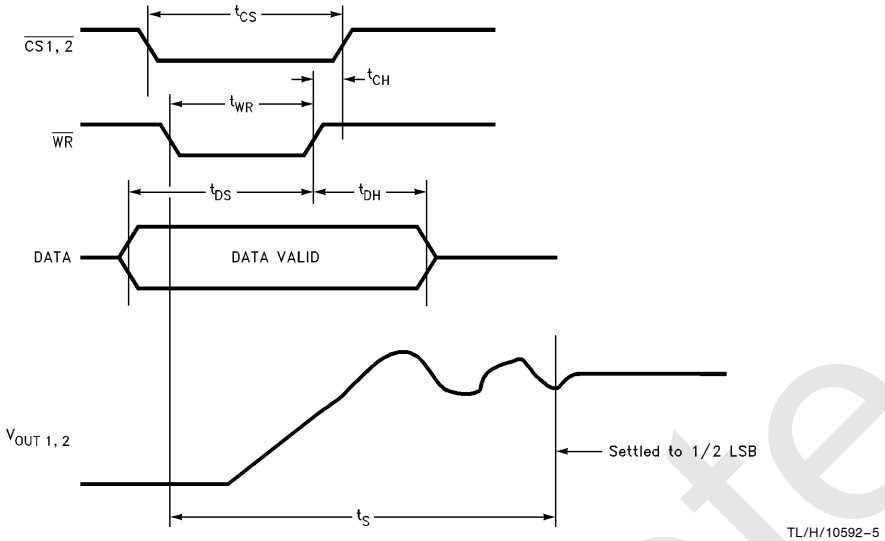
Timing Waveforms



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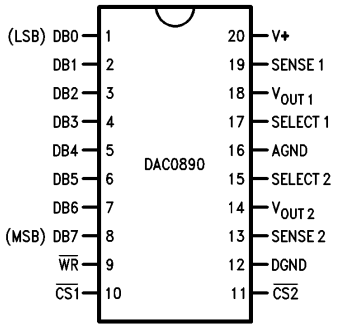
Connection Diagram

Dual-In-Line Package



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Pin Description

DB0–DB7 (1–8) These pins are data inputs for each of the internal 8-bit DACs. DB0 is the least-significant-bit.

$\overline{WR}$ (9) This is the WRITE command input pin. This input is used in conjunction with $\overline{CS1}$ and $\overline{CS2}$ to write data into either of the internal DACs. The data is latched into a selected DAC with the rising edge of either $\overline{WR}$ or $\overline{CS1}$ for DAC1 or $\overline{CS2}$ for DAC2, whichever occurs first.

$\overline{CS1}$ (10) This is the input pin used to select DAC1. This input is used in conjunction with the $\overline{WR}$ input to write data into either of the internal DACs. The data is latched into DAC1 with the rising edge of either $\overline{CS1}$ or $\overline{WR}$, whichever occurs first.

$\overline{CS2}$ (11) This is the input pin used to select DAC2. This input is used in conjunction with the $\overline{WR}$ input to write data into either of the internal DACs. The data is latched into DAC2 with the rising edge of either $\overline{CS2}$ or $\overline{WR}$, whichever occurs first.

DGND (12) The system digital ground is connected to this pin. For proper operation, this and AGND must be connected together.

SENSE 2 (13) DAC2's output sense connection. When this pin is connected to the VOUT2's load impedance, the feedback loop will compensate for any voltage drops between the VOUT2 pin and the load.

V_{OUT2} (14) DAC2's voltage output connection. It provides two full-scale output voltage ranges, 2.55V and 10.2V.

SELECT 2 (15) The two output voltage ranges available from DAC2 are selected by connecting this pin to SENSE2 for the 2.55V full-scale range and leaving it unconnected for the 10.2V full-scale range.

AGND (16) The system digital ground is connected to this pin. For proper operation, this and DGND must be connected together.

SELECT 1 (17) The two output voltage ranges available from DAC1 are selected by connecting this pin to SENSE1 for he 2.55V full-scale range and leaving it unconnected for the 10.2V full-scale range.

V_{OUT1} (18) DAC1's voltage output connection. It provides two full-scale output voltage ranges, 2.55V and 10.2V.

SENSE 1 (19) DAC1's output sense connection. When this pin is connected to the VOUT1's load impedance, the feedback loop will compensate for any voltage drops between the VOUT1 pin and the load.

V^+ (20) The power supply voltage, ranging from 4.75V to 16.5V, is applied to this pin. It should be bypassed, to AGND, with a 0.01 $\sim$ 0.1 μF ceramic capacitor in parallel with a 2.2 $\sim$ 22 μF electrolytic capacitor.

Functional Description

The DAC0890 is a monolithic dual 8-bit bipolar Digital-to-Analog converter comprising six major functional blocks designed to operate on a single supply as low as 5V (±5%). These include two latch/DAC combinations, two high-speed output amplifiers, band-gap reference, and control/interface logic.

The two internal 8-bit DACs use equal valued current sources. Controlled by a corresponding bit in the input data, each current source's output is switched into either an R/2R ladder or AGND. Each internal DAC has an 8-bit latch to store a digital input. See *Figure 1*.

The high-speed output amplifiers operate in the non-inverting mode. The R-2R's output current is applied to the output amplifier and converted to a voltage. The amplifier's gain is externally set through the range select pin. The two ranges are 0V to 2.55V and 0V to 10.2V. The internal resistors that set the gain are matched to the unit resistor of the R/2R ladder. This ensures that these resistors match over process variations and temperature. This greatly reduces gain variations that would exist if external gain setting resistors were used.

An internal band-gap reference and its control amplifier generate a full scale reference voltage for the DACs. It produces a 1.2V output from a single supply.

The DAC0890 provides a TTL and CMOS-compatible control interface and allows writing and latching digital values to each of the internal DACs.

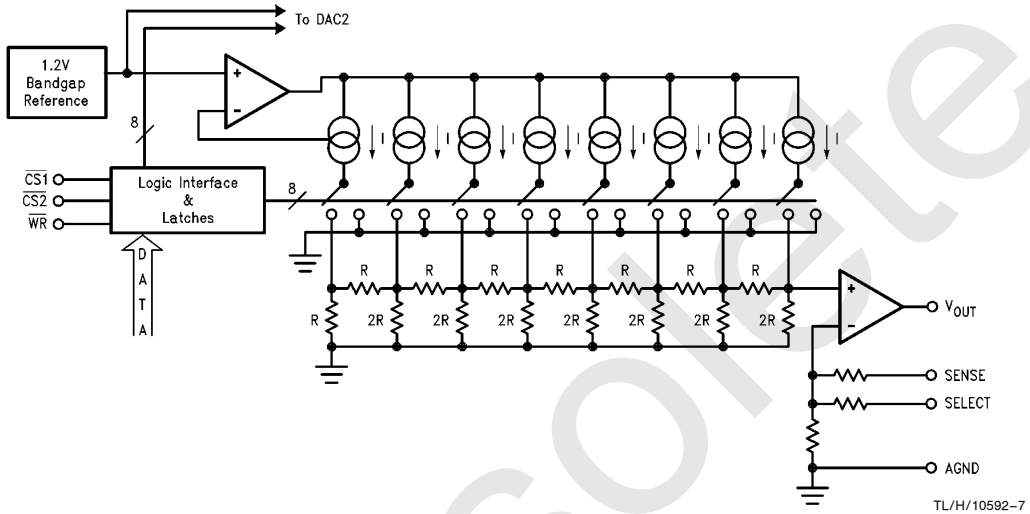

FIGURE 1. Simplified Internal Schematic (One DAC Shown)

Applications Information

Full-Scale Output Voltage Range Selection

The DAC0890 has been designed for ease of use. All reference voltage and output amplifier connections are internal. All trims such as full-scale (gain) and zero (offset) are performed during manufacturing. Therefore, no external trimming is required to achieve the specified accuracy. The only external connections required select the desired full-scale output voltage range.

The two full-scale output voltage ranges are selected by connecting SENSE, SELECT and VOUT as shown in *Figure 2a*, *b*. The 2.55V range can be used with supply voltages as low as 4.75V. The 10.2V range can be selected with supplies as low as 12.0V.

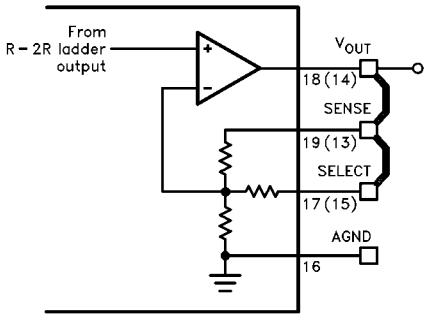

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FIGURE 2a. 0V to 2.55V Output Voltage Range

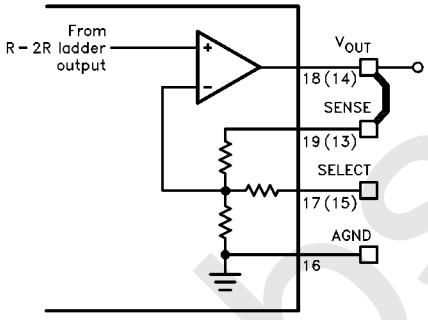

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FIGURE 2b. 0V to 10.2V Output Voltage Range

Power Supply Voltage

The DAC0890 is designed to operate on a single power supply voltages +4.75V and +16.5V. For 2.55V full-scale operation the power supply voltage can be as low as +4.75V. When the 10.2V full-scale is used the supply voltage needs to be between +12V to +16.5V.

Grounding and Power Supply Bypassing

Proper grounding is essential to extract all the precision and full rated performance that the DAC0890 is capable of delivering. Typical applications for the DAC0890 include operation with a microprocessor. In this environment digital noise is prevalent and anticipated. Therefore, special care must be taken to ensure that proper operation will be achieved.

The DAC0890 uses two ground pins, AGND and DGND, to minimize ground drops and noise in the analog signal paths. *Figure 3* details the proper bypassing and ground connections.

The DAC0890's best performance can be ensured by connecting 0.01 μF to 0.1 μF ceramic capacitor in parallel with an electrolytic of 2.2 μF to 22 μF between the V^+ pin and AGND.

Sense Inputs

The SENSE inputs (pins 13 and 19) allow compensation for voltage drops in long output lines to remote loads. This places the drops in the internal amplifier's feedback loop. An example of this is shown in *Figure 3*. The I-R drop, which might be caused by printed circuit board traces or long cables, between the VOUT2 and the load impedance R_L is placed inside the feedback loop if SENSE1 is connected directly to the load. This forces the voltage at the load to be the correct value. It is important to remember that the voltage at the DAC0890's VOUT pins may become higher than the full-scale output voltage selected using the SELECT pins. Therefore, the power supply voltage applied to V^+ must be ≥2.2V above the resulting output voltage (at pins 14 and 18) when the SENSE inputs are used.

The SENSE inputs have a finite input impedance. The range-setting resistors load the output with 2.5 kΩ when the 0V to 2.55V range is selected and 10 kΩ when the 0V to 10.2V range is selected.

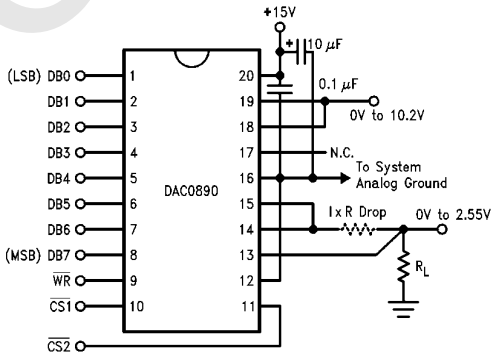

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FIGURE 3. Typical Connection Showing Power Supply Bypassing, and the Use of SENSE Inputs

Minimizing Settling Time

The DAC0890's output stage uses a passive pull-down resistor to achieve single supply operation and an output voltage range that includes ground. This results in a negative-going settling time that is longer than the settling time or positive-going signals. The actual settling time is dependant on the load resistance and capacitance. If available, a negative power supply can be used to improve the negative settling time by connecting a pull down resistor between the output and the negative supply. The resistor's value is chosen so that the current through the pull down resistor is not greater than 0.5 mA when the output voltage is 0V. See *Figure 4*.

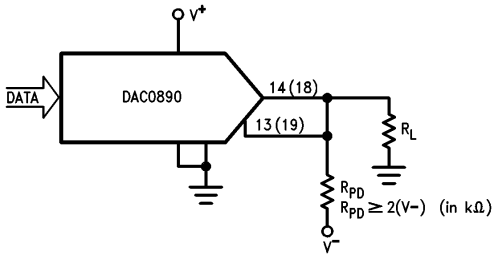

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FIGURE 4. Improving Negative Slew Rate

Bipolar Operation

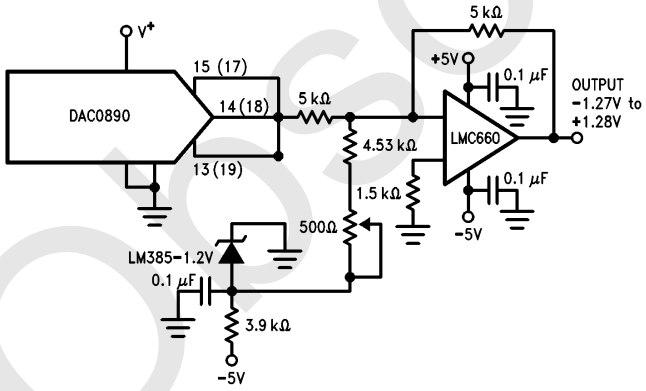
While the DAC0890 was designed to operate on a single positive supply voltage and generate a unipolar output voltage, bipolar operation is still possible if a negative supply is available or added. As shown in *Figure 5*, the output voltage is offset and scaled to achieve a −1.27V to +1.28V output range with the addition of a −5V supply. The required offset is generated with an LM385–1.2V reference. The external output amplification is provided by the LMC660. The output voltage is generated with a complementary binary offset input code.

Microprocessor Interface

When interfacing with a microprocessor, the DAC0890 appears as a two byte write-only memory location for memory mapped and I/O mapped input-output. Each of the internal DACs is chosen through one of the two chips selects, CS1 or CS2. The action of the control signals is detailed in Table I. The data is latched on the rising edge of either Chip Select or $\overline{WR}$, whichever occurs first for a given selected DAC. For interfacing ease, $\overline{WR}$ can be tied low and $\overline{CS1}$ or $\overline{CS2}$ can be used to latch the data. Both DACs can be updated simultaneously by pulling both $\overline{CS1}$ and $\overline{CS2}$ low. Further versatility is provided by the ability of $\overline{WR}$ and $\overline{CS1}$ and/or $\overline{CS2}$ to be tied together.

TABLE I. DAC0890 Control Logic Truth Table

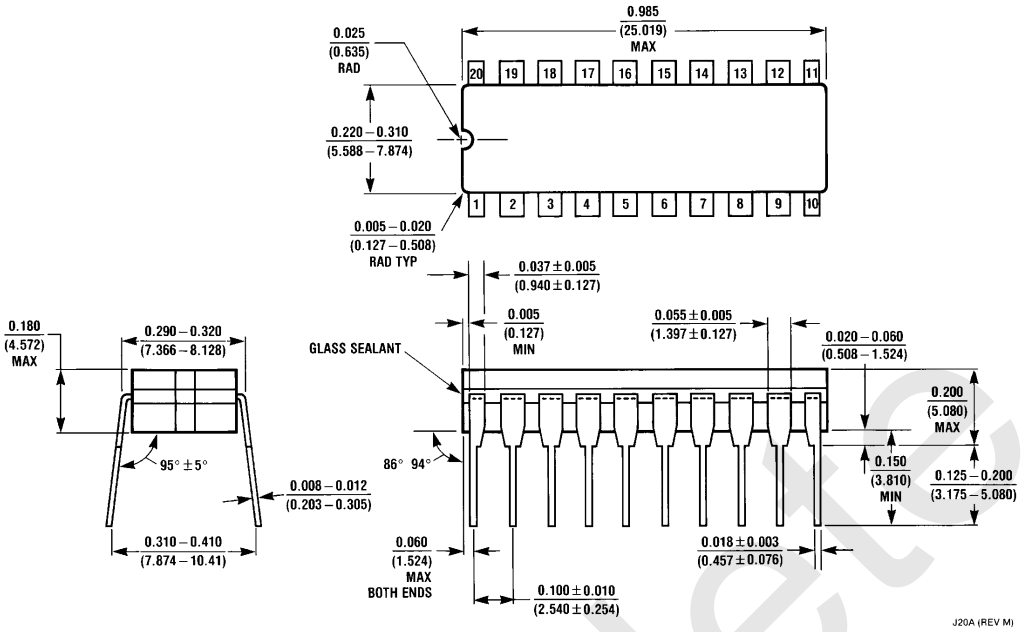
Input Data	$\overline{WR}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	↑	0	0	latching
1	↑	0	1	latching
0	0	↑	0	latching
1	0	↑	1	latching
X	1	X	previous data	latching
X	X	1	previous data	latching
X	1	1	previous data	latching



TL/H/10592–12

FIGURE 5. Bipolar Operation

Physical Dimensions inches (millimeters)



Cerdip Dual-In-Line Package (J)
Order Number DAC0890CIJ
NS Package Number J20A

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