

DAC1600

FOR COMMERCIAL APPLICATIONS

Monolithic 16-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
INTERNAL REFERENCE
 $\pm 10V$ OUTPUT OPERATIONAL AMPLIFIER
- 14-BIT ACCURACY (K GRADE):
 $\pm 0.003\%$ FSR LINEARITY ERROR
14-BIT MONOTONICITY GUARANTEED $0^\circ C$ to $+70^\circ C$
- SETTLING TIME $10\mu s$, MAX
- $\pm 15V$ POWER SUPPLY OPERATION
- 24-PIN MOLDED PLASTIC DIP

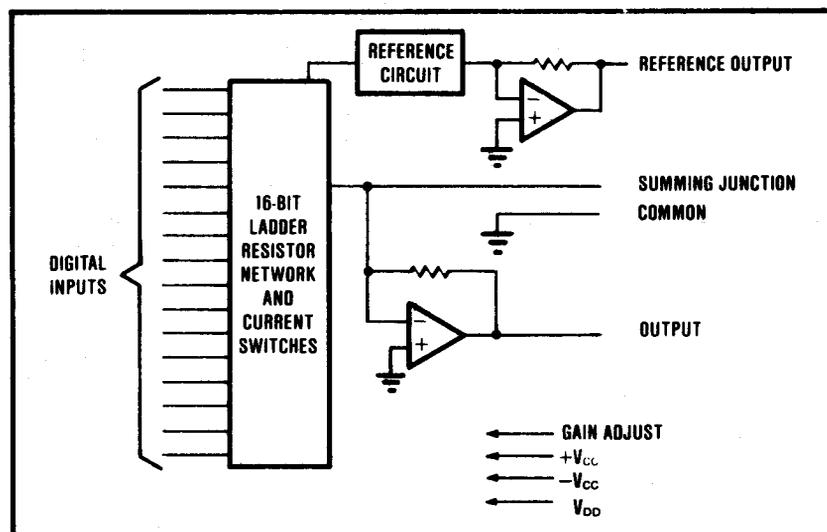
DESCRIPTION

The low prices of DAC1600JP and DAC1600KP make these very-high resolution D/A converters the best value available.

The DAC1600 family offers TTL input compatibility, guaranteed monotonicity (13-bit, J grade; 14-bit, K grade) over $0^\circ C$ to $+70^\circ C$ and settling time of $10\mu s$ maximum.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

The DAC1600 is priced and specified for applications where high resolution and monotonicity are the key application parameters and where tightly-specified performance over temperature is not required. Because of the low price, it is feasible to use a 16-bit D/A converter for new applications in communications systems, electronic controllers, electronic games, and personal computer peripherals.



SPECIFICATIONS

ELECTRICAL

Typical at +25°C. $\pm V_{CC} = 15V$, $V_{DD} = +5V$ unless otherwise noted.

MODEL	DAC1600JP-V	DAC1600KP-V	UNITS
INPUTS			
DIGITAL INPUTS			
Input Code ⁽¹⁾	COB	*	Bits
Resolution, max	16	*	Bits
Digital Logic Inputs ⁽²⁾ :			
V_{IH} , min to max	+2.4 to $+V_{DD}$	*	V
V_{IL} , min to max	-1.0 to +0.8	*	V
I_{IH} , $V_i = +2.7V$, max	+40	*	μA
I_{IL} , $V_i = +0.4V$, max	-0.5	*	mA
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error, max ⁽³⁾	± 0.006	± 0.003	% of FSR ⁽⁴⁾
Differential Linearity Error, max	± 0.012	± 0.006	% of FSR
Gain Error, max ⁽⁵⁾⁽⁶⁾	± 0.3	*	%
Bipolar Zero Error, max ⁽⁵⁾	40	*	mW
Monotonicity Over 0°C to +70°C ⁽⁷⁾	13	14	Bits
Sensitivity of Gain to Power Supply Variations:			
$\pm V_{CC}$	± 0.002	*	% of FSR/% V_{CC}
V_{DD}	± 0.0002	*	% of FSR/% V_{DD}
TEMPERATURE COEFFICIENTS			
Gain	± 10	*	ppm/°C
Bipolar Zero	± 5	*	ppm of FSR/°C
SETTLING TIME (to $\pm 0.003\%$ of FSR) ⁽⁸⁾ , 10V step and 2k Ω load, max			
	10	*	μsec
OUTPUT			
ANALOG OUTPUT			
Voltage Range, min	± 10	*	V
Current, min ⁽⁹⁾	± 5	*	mA
Impedance	0.15	*	Ω
REFERENCE OUTPUT			
Voltage ⁽¹⁰⁾	+6.3	*	V
Source Current Available for External Loads, max	+1.5	*	mA
Temperature Coefficient	± 10	*	ppm/°C
POWER SUPPLY REQUIREMENTS			
RATED VOLTAGE			
$\pm V_{CC}$ ⁽¹¹⁾	15	*	V
V_{DD} ⁽¹²⁾	+5	*	V
CURRENT, max⁽¹³⁾			
$\pm V_{CC}$	35	*	mA
V_{DD}	8	*	mA
TEMPERATURE RANGE			
For parameters specified over temp, min/max			
Storage, min/max	0 to +70	*	°C
	-60 to +100	*	°C

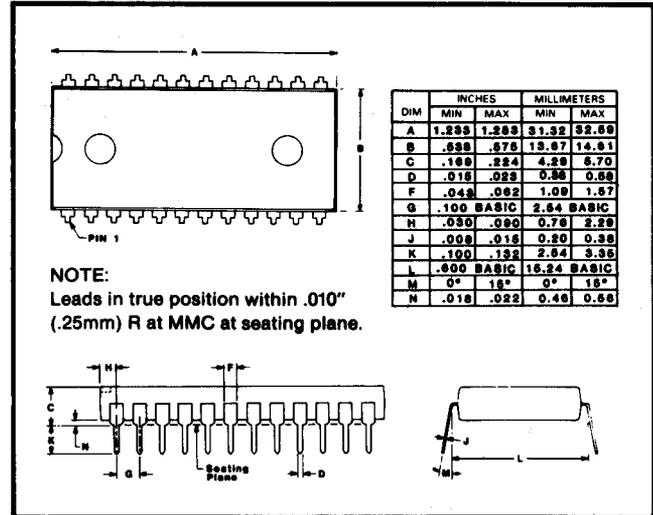
NOTES: (1) COB = Complementary Offset Binary. (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4.5V to $+V_{CC}$. Digital input specs are guaranteed over 0°C to +70°C. These specs are tested at 25°C only. (3) $\pm 0.003\%$ of FSR is 1/2LSB at 14 bits. (4) FSR means Full Scale Range and is 20V for a $\pm 10V$ range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the gain potentiometer rotates the transfer function around Bipolar Zero, 0V (Input Code 7FFF_H). (7) Guaranteed. Tested at 25°C only. (8) Guaranteed. Not tested. (9) Output may be indefinitely shorted to Common without damage. (10) Tolerance is $\pm 5\%$. (11) Range of operation is $\pm 13.5V$ to $\pm 16.5V$. (12) V_{DD} may be operated up to $+V_{CC}$. Digital input logic threshold remains at +1.4V over the V_{DD} range. (13) Typical power supply currents are about 50% of the maximum.

ABSOLUTE MAXIMUM RATINGS

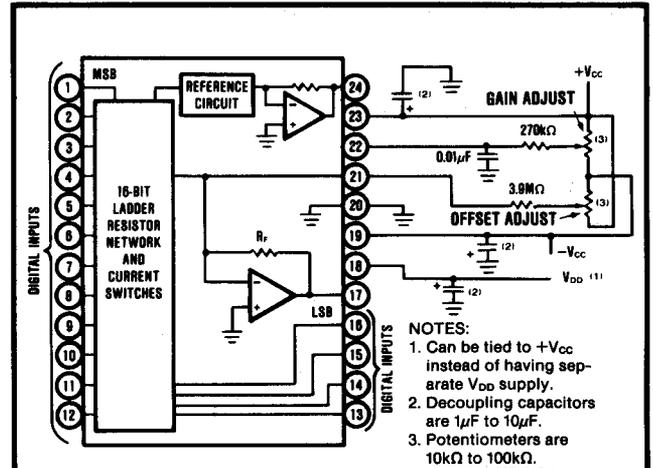
$+V_{CC}$ to Common	0V, +18V
$-V_{CC}$ to Common	0V, -18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	-1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to D/A Output	-5V to +5V
V_{OUT}	Indefinite Short to Common
Power Dissipation	1000mW
Storage Temperature	-60°C to +100°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

MECHANICAL



CONNECTION DIAGRAM



ORDERING INFORMATION

Model	Linearity Error & Monotonicity for	1-99	100-999	1000+
DAC1600JP-V	13 bits	\$14.35	\$8.95	\$8.05
DAC1600KP-V	14 bits	15.95	9.95	8.95

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PIN ASSIGNMENTS

Pin	Description	Pin	Description
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16 (LSB)
5	Bit 5	17	V_{OUT}
6	Bit 6	18	V_{DD}
7	Bit 7	19	$-V_{CC}$
8	Bit 8	20	Common
9	Bit 9	21	Summing Junction (Zero Adjust)
10	Bit 10	22	Gain Adjust
11	Bit 11	23	$+V_{CC}$
12	Bit 12	24	+6.3V Reference Output

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. $1\mu\text{F}$ to $10\mu\text{F}$ tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be $100\text{ppm}/^\circ\text{C}$ or less. The $3.9\text{M}\Omega$ and $270\text{k}\Omega$ resistors ($\pm 20\%$ carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in place of the $3.9\text{M}\Omega$ part. A $0.001\mu\text{F}$ to $0.01\mu\text{F}$ ceramic capacitor should be connected from Gain Adjust to Common to prevent noise pickup. See Figure 2 for relationship of zero and gain adjustment.

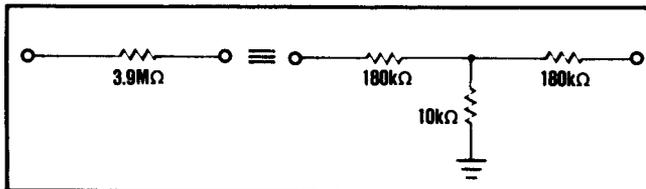


FIGURE 1. Equivalent Resistances.

Zero Adjustment

Apply the digital input code that produces zero output voltage or current. See Table I for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

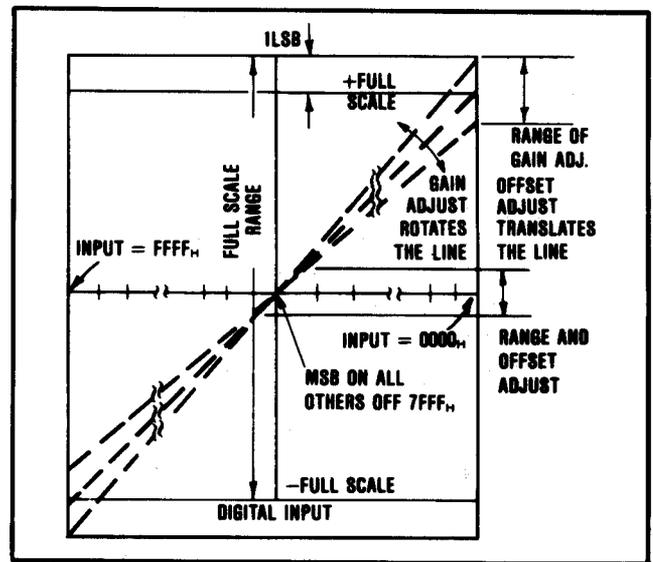


FIGURE 2. Relationship of Zero and Gain Adjustment.

TABLE I. Calibration Table.

Digital Input	Description	Analog Output		
		16-bit	15-bit	15-bit
One LSB	One LSB	$305\mu\text{V}$	$610\mu\text{V}$	$1224\mu\text{V}$
0000 _H	+ Full Scale	$+9.99960\text{V}$	9.99939V	$+9.99878\text{V}$
7FFF _H	Bipolar Zero	0V	0V	0V
FFFF _H	- Full Scale	-10.00000V	-10.00000V	-10.00000V

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single $1\text{k}\Omega$ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a 20V full-scale range, 1LSB is $305\mu\text{V}$. With a load current of 5mA , series wiring and connector resistances of only $60\text{m}\Omega$ will cause the output to be in error by 1LSB . To understand what this means in terms of a system layout, the resistance of #23 wire is about $0.021\Omega/\text{ft}$. Neglecting contact resistance, less than 18 inches of wire will produce a $1/2\text{LSB}$ error in the analog output voltage!

In Figure 3 lead and contact resistances are represented by R_1 through R_3 . As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed during initial calibration. R_2 is part of R_L , if the output voltage is sensed at Common, and therefore introduces no error. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_3 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC1600 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under $20\mu\text{A}$ (with changing input codes), therefore R_3 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_3 ($R_3 \times 2\text{mA}$) appears as zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figure 3.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

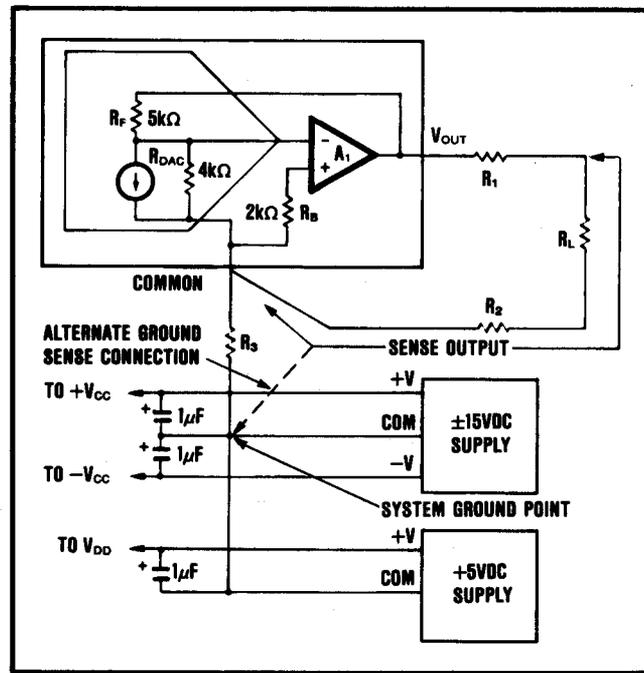


FIGURE 3. Output Circuit.

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