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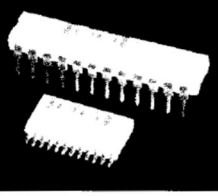


DAC713

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

16-Bit DIGITAL-TO-ANALOG CONVERTER With 8-Bit Double-Buffered Bus Interface

FEATURES

- HIGH-SPEED 8-BIT PARALLEL DOUBLE-BUFFERED INTERFACE
- VOLTAGE OUTPUT: ±10V, ±5V, 0 to +10V
- 13-, 14-BIT LINEARITY GRADES
- 14-BIT MONOTONIC OVER TEMPERATURE (B GRADE)
- GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters
- SPECIFIED OVER –40°C TO +85°C
- 24-LEAD SKINNY DIP AND SOIC PACKAGES

DESCRIPTION

DAC713 is a complete 16-bit resolution monolithic digital-to-analog converter.

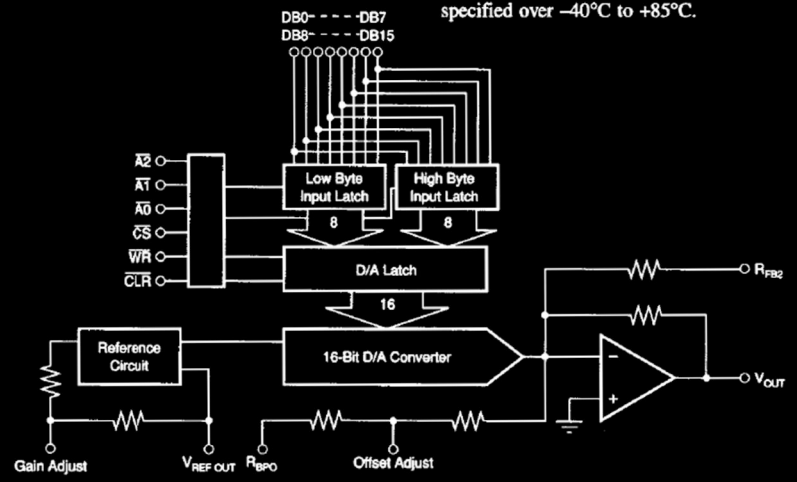
DAC713 has precision temperature compensated voltage reference, voltage output amplifier and 8-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a RESET function.

GAIN and BIPOLAR OFFSET adjustment are arranged so that they can be set by external digital-to-analog converters as well as by potentiometers.

DAC713 is available in two linearity error grades: ±4LSB DAC713P and U, ±2LSB DAC713PB and UB, and are specified at power supply voltages of ±12V and ±15V.

DAC713 is packaged in a 24-pin plastic skinny-DIP and in a wide-body 24-lead plastic SOIC. DAC713 is specified over –40°C to +85°C.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = −12V and −15V unless otherwise noted.

PARAMETER	DAC713P, U			DAC713PB, UB			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
RESOLUTION	16			*			Bits
DIGITAL INPUTS							
Input Code		Binary Two's Complement			*		
Logic Levels[1]							
V_{IH}	+2.0		$+V_{CC}$	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	µA
I_{IL} (V_I = +0.4V)			±10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Differential Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Monotonicity Over							
T_{MIN} to T_{MAX}	13			14			Bits
Gain Error[3]			±0.1			*	%
T_{MIN} to T_{MAX}			±0.25			±0.02	%
Unipolar/Bipolar Zero Error[3]			±0.1			*	% of FSR[2]
T_{MIN} to T_{MAX}			±0.2			±0.15	% of FSR
Power Supply Sensitivity of Gain			±0.003			*	%FSR/%+V_{CC}
			±30			*	ppm FSR/%V_{CC}
DYNAMIC PERFORMANCE							
Settling Time (to ±0.003%FSR, 5kΩ || 500pF Load)[4]							
20V Output Step		6			*	10	µs
1LSB Output Step[5]		4			*		µs
Output Slew Rate		10			*		V/µs
Total Harmonic Distortion							
0dB, 1001Hz, f_S = 100kHz		0.005			*		%
−20dB, 1001Hz, f_S = 100kHz		0.03			*		%
−60dB, 1001Hz, f_S = 100kHz		3.0			*		%
SINAD: 1001Hz, f_S = 100kHz		87			*		dB
Digital Feedthrough[5]		2			*		nV–s
Digital-to-Analog Glitch Impulse[5]		15			*		
Output Noise Voltage (includes reference)		120			*		nV/√Hz
ANALOG OUTPUT							
Output Voltage Range							
+V_{CC}, −V_{CC} = ±11.4V	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.1			*		Ω
Short Circuit to ACOM Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+9.975	+10.000	+10.025	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	V
Output Resistance		1			*		Ω
Source Current	2			*			mA
Short Circuit to ACOM Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage							
+V_{CC}	+11.4	+15	+16.5	*	*	*	V
−V_{CC}	−11.4	−15	−16.5	*	*	*	V
Current (No Load, ±15V Supplies)							
+V_{CC}		15	TBD		*	*	mA
−V_{CC}		24	TBD		*	*	mA
Power Dissipation[6]			TBD			*	W
TEMPERATURE RANGES							
Specification	−40		+85	*		*	°C
Storage	−60		+150	*		*	°C
Thermal Coefficient, θ_{JA}							
Plastic DIP		75			*		°C/W
Plastic SOIC		75			*		°C/W

*Same specification as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst-case code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. (6) Typical supply voltages times maximum currents.

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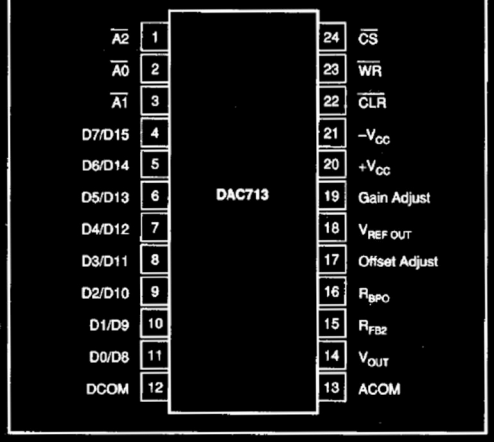
PIN CONFIGURATION

Top View — DIP AND SOIC



ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to COMMON	0V to +17V
$-V_{CC}$ to COMMON	0V to −17V
$+V_{CC}$ to $-V_{CC}$	34V
Digital Inputs to COMMON	−1V to $+V_{CC}$
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
Power Dissipation	750mW
Storage Temperature	−60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	LINEARITY ERROR max at +25°C	TEMPERATURE RANGE
DAC713P	Plastic DIP	±4	−40°C to +85°C
DAC713U	Plastic SOIC	±4	−40°C to +85°C
DAC713PB	Plastic DIP	±2	−40°C to +85°C
DAC713UB	Plastic SOIC	±2	−40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC713P	Plastic DIP	243
DAC713U	Plastic SOIC	239
DAC713PB	Plastic DIP	243
DAC713UB	Plastic SOIC	239

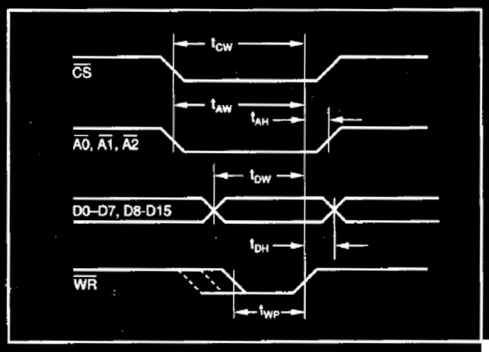
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TIMING SPECIFICATIONS

T_A = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{DW}	Data Valid to End of $\overline{WR}$	80		ns
t_{CS}	$\overline{CS}$ Valid to End of $\overline{WR}$	80		ns
t_{AW}	$\overline{A0}$, $\overline{A1}$, $\overline{A2}$: Valid to End of $\overline{WR}$	80		ns
t_{DH}	Data Hold After End of $\overline{WR}$	10		ns
t_{AH}	$\overline{A0}$, $\overline{A1}$, $\overline{A2}$ HOLD after End of $\overline{WR}$	10		ns
t_{WP}	Write Pulse Width	80		ns
t_{CP}	CLEAR Pulse Width	150		ns

TIMING DIAGRAM



TIMING DIAGRAM

$\overline{A0}$	$\overline{A1}$	$\overline{A2}$	$\overline{WR}$	$\overline{CS}$	$\overline{CLR}$	DESCRIPTION
0	1	1	1→0→1	0	1	Load LOW Byte
1	0	1	1→0→1	0	1	Load HIGH Byte
1	1	0	1→0→1	0	1	Load D/A Latch
X	X	X	X	1	1	No Change
X	X	X	1	X	1	No Change
X	X	X	X	X	0	RESET D/A Latch

NOTE: X = Don't Care.