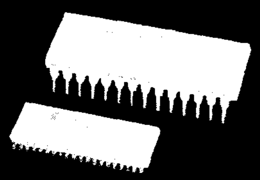
BURR - BROWN®



DF1750

Dual Channel DIGITAL DECIMATION FILTER

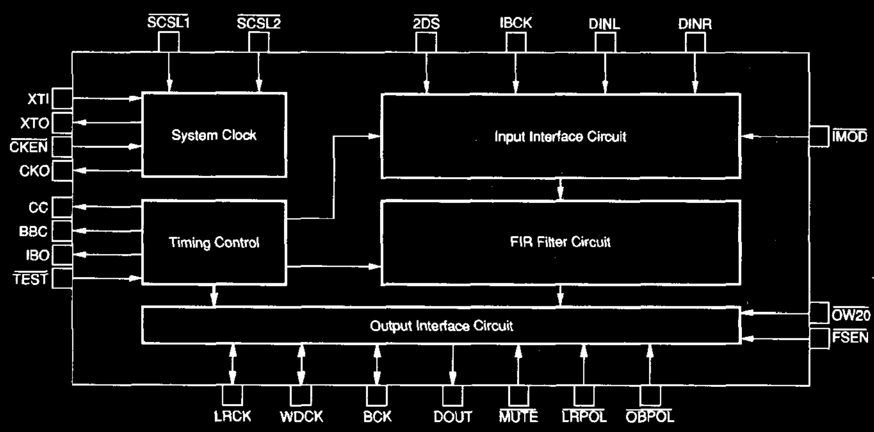
FEATURES

- USER SELECTABLE FOR 1/4 OR 1/2 DECIMATING RATIOS
- USER SELECTABLE FOR 16- OR 18-BIT INPUT DATA
- SERIAL DATA INPUT IS COMPATIBLE WITH THE BURR-BROWN PCM1750 ADC
- FILTERS OUT-OF-BAND NOISE WITH STOPBAND ATTENUATION > 95dB
- PASSBAND RIPPLE < 0.0005dB
- SINGLE +5V SUPPLY OPERATION WITH LOW POWER DISSIPATION OF ONLY 250mW

DESCRIPTION

The DF1750 is a high performance 1/4 or 1/2 decimating digital filter that is designed for digital audio applications. This device decimates and filters 2x or 4x (2fs or 4fs) oversampled data from the output of an ADC to a data frequency of fs. The technique of oversampling and decimating allows the input to an oversampling ADC to be processed by a much lower order, linear phase, analog low-pass filter. This simultaneously improves system performance while reducing circuit complexity and cost.

The DF1750 provides output data word rates (fs) up to 50.5kHz and it is compatible with the Burr-Brown PCM1750, dual 18-bit analog-to-digital converter.



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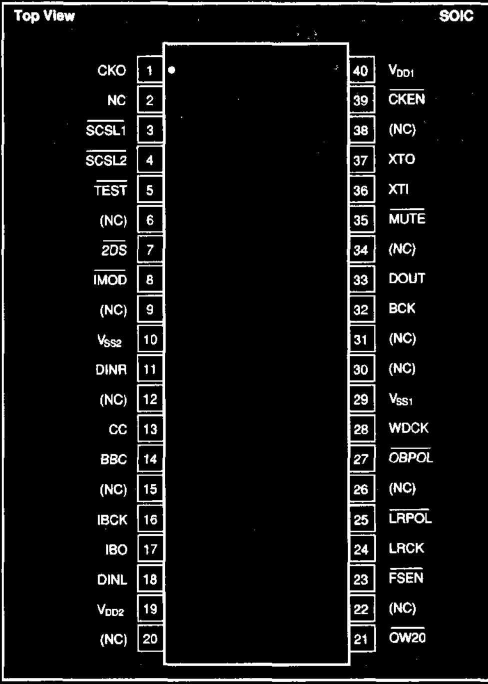
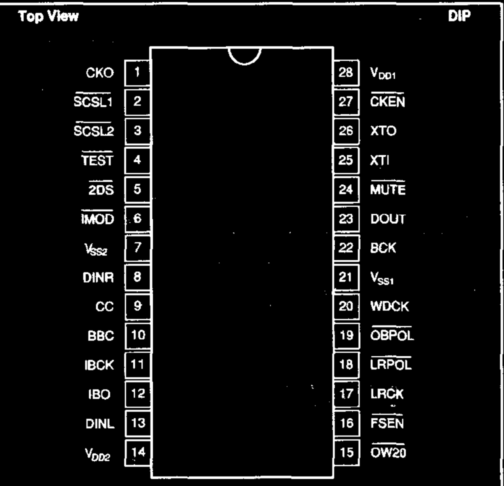
PIN CONFIGURATION





PIN DESCRIPTION

PIN NO. DIP	PIN NO. SOIC	NAME	I/O*	DESCRIPTION
1	1	CKO	o	Clock output (the same as XTI frequency), CKO = L when $\overline{CKEN}$ = H
–	2	(NC)		
2	3	$\overline{SCSL1}$	ip	XTI Frequency select
3	4	$\overline{SCSL2}$	ip	(Refer to XTI pin description)
4	5	$\overline{TEST}$	ip	Test, (Test = L; test mode)
–	6	(NC)		
5	7	$\overline{2DS}$	ip ip	1/4 or 1/2 decimating select $\overline{2DS}$ = H: 1/4 decimating, $\overline{2DS}$ = L: 1/2 decimating
6	8	$\overline{IMOD}$	ip	A/D converter interface mode select
–	9	(NC)		
7	10	V_{SS2}	–	GND 2
8	11	DINR	ip	Rch input data
–	12	(NC)		
9	13	CC	o	A/D converter control signal
10	14	BBC	o	A/D converter control signal
–	15	(NC)		
11	16	IBCK	ip	Input data bit clock input
12	17	IBO	o	Input data bit clock output
13	18	DINL	ip	Lch input data
14	19	V_{DD2}	–	+5V
–	20	(NC)		
15	21	$\overline{OW20}$	ip	Output data bit select (16bit: $\overline{OW20}$ = H, 20 bit: $\overline{OW20}$ = L)
–	22	(NC)		
16	23	$\overline{FSEN}$	ip	I/O pin select (FSEN = H: BCK, WDCK, LRCK pin=Input (FSEN = L: BCK, WDCK, LRCK *pin=Output*)
17	24	LRCK	ip	fs clock
18	25	$\overline{LRPOL}$	ip	LRCK polarity select ($\overline{LRPOL}$ = H: Lch/Rch=Low/High) (LRPOL = L: Lch/Rch=High/Low)
–	26	(NC)		
19	27	$\overline{OBPOL}$	ip	BCK polarity select
20	28	WDCK	ip/o	2fs clock
21	29	V_{SS1}	–	GND 1
–	30	(NC)		
–	31	(NC)		
22	32	BCK	ip/o	Output data bit clock
23	33	DOUT	o	Data output (Lch or Rch serial data output).
–	34	(NC)		
24	35	$\overline{MUTE}$	ip	Data output mute, ($\overline{MUTE}$ = L: DOUT = L)
25	36	XTI	i	Oscillator Input (512fs: $\overline{SCSL1}$ = H, $\overline{SCSL2}$ = H) (256fs: SCSL1 = H, SCSL2 = L) (768fs: $\overline{SCSL1}$ = L, $\overline{SCSL2}$ = H) (384fs: SCSL1 = L, $\overline{SCSL2}$ = L)
26	37	XTO	o	Oscillator Output
–	38	(NC)		
27	39	$\overline{CKEN}$	ip	*CKO output select, ($\overline{CKEN}$ = H, CKO = L)*
28	40	V_{DD1}	–	+5V

*i = Input pin ip = input with pull-up resistor o = Output pin ip/o = Input with pull-up resistor when $\overline{FSEN}$ = H, output with $\overline{FSEN}$ = L.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD})	–0.3V to +7.0V
Input Voltage (V_{IN})	–0.3V to V_{DD} + 0.3V
Soldering Temperature	+255°C
Soldering Time	10s
Storage Temperature	–40°C to +125°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DF1750P	28-Pin Plastic DIP	215
DF1750U	40-Pin Plastic SOIC	252

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

DC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = –20°C to +80°C unless otherwise specified.

				DF1750P/U			
PARAMETER	PIN	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
INPUTS							
Logic Family					CMOS		
Logic Voltages	XTI	V_{IL1}	For Clock Input			0.3V_{DD}	V
	XTI	V_{IH1}	For Clock Input	0.7V_{DD}			V
	XTI	V_{CLK}	For AC Coupling	1.8			V_{P-P}
	(1),(2)	V_{IL2}	$\overline{FSEN}$ = H			0.5	V
	(1),(2)	V_{IH2}	$\overline{FSEN}$ = H	2.4			V
Logic Currents	XTI	I_{IL1}	V_{IN} = 0V		5	10	µA
	XTI	I_{IH1}	V_{IN} = V_{DD}		5	10	µA
	(1),(2)	I_{IL2}	V_{IN} = 0V, $\overline{FSEN}$ = H		10	20	µA
Input Leakage Current	(1),(2)	I_{LH1}	V_{IN} = V_{DD}, $\overline{FSEN}$ = H			1.0	µA
OUTPUTS							
Logic Family					CMOS		
Logic Voltages	(2),(3)	V_{OL}	I_{OL} = 1.6mA, $\overline{FSEN}$ = L			0.4	V
	(2),(3)	V_{OH}	I_{OH} = –0.4mA, $\overline{FSEN}$ = L	2.5			
POWER SUPPLY REQUIREMENTS							
Supply Voltage		V_{DD1}, V_{DD2}			+5		V
Supply Current		I_{DD}	V_{DD} = 5V[4], $\overline{FSEN}$ = H			30	mA
Power Dissipation		P_D	Nominal V_{DD}			250	mW
TEMPERATURE RANGE (AMBIENT, T_A)							
Specification				–20		+80	°C
Operating				–20		+80	°C

NOTES: (1) Refers to pins $\overline{SCSL1}$, $\overline{SCSL2}$, $\overline{TEST}$, $\overline{2DS}$, $\overline{IMOD}$, DINR, IBCK, DINL, $\overline{OW20}$, $\overline{MUTE}$, $\overline{OBPOL}$, $\overline{LRPOL}$, $\overline{FSEN}$, $\overline{CKEN}$. (2) Refers to pins BCK, WDCK, LRCK. (3) Refers to pins CKO, CC, BBC, IBO, DOUT. (4) Test Condition; $\overline{SCSL1}$ = H, $\overline{SCSL2}$ = H, $\overline{TEST}$ = H, $\overline{2DS}$ = H, $\overline{IMOD}$ = H, $\overline{OW20}$ = H, $\overline{MUTE}$ = H, $\overline{OBPOL}$ = H, $\overline{LRPOL}$ = H, $\overline{FSEN}$ = L, $\overline{CKEN}$ = L. T_{CY} = 38ns (XTI Clock Period), C_L = 0pF (Capacitive Load), DINL, DINR (Applicable Input Data).

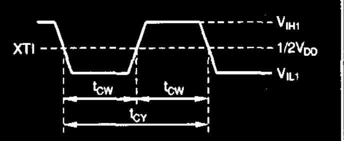
AC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = –20°C to +80°C unless otherwise specified.

XTI Clock

PARAMETER	SYMBOL	CONDITION $\overline{SCSL1}$	CONDITION $\overline{SCSL2}$	SYS FREQ	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
Crystal Oscillator Frequency	F_{OSC}	H	H	512fs(1)	8		26	MHz
		H	L	256fs	4		13	MHz
		L	H	768fs	12		26	MHz
		L	L	384fs	6		20	MHz
External Clock Pulse Width	t_{CW}	H	H	512fs	15		70	ns
		H	L	256fs	38		140	ns
		L	H	768fs	15		50	ns
		L	L	384fs	25		100	ns
External Clock Pulse Period	t_{CY}	H	H	512fs	38		125	ns
		H	L	256fs	77		250	ns
		L	H	768fs	38		84	ns
		L	L	384fs	50		167	ns

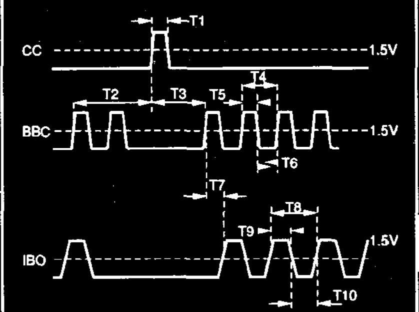


AC Coupling is required with an external clock.

NOTE: (1) fs = Sampling frequency.

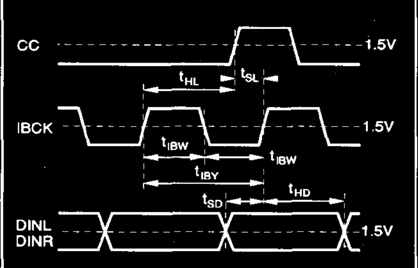
ADC CONTROL SIGNAL TIMING (CC, BBC, AND IBO) WITH $\overline{IMOD}$ = H

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
$\overline{2DS}$ = H					
CC Pulse Width (H)	T1	65	1/256fs		ns
S/H Acquisition Time	T2	670	9/256fs		ns
CC-BBC Time	T3	285	4/256fs		ns
BBC Pulse Period	T4	228	3/256fs		ns
BBC Pulse Width (H)	T5	65	1/256fs		ns
BBC Pulse Width (L)	T6	140	2/256fs		ns
BBC-IBO Time	T7	140	2/256fs		ns
IBO Pulse Period	T8	228	3/256fs		ns
IBO Pulse Width (H)	T9	140	2/256fs		ns
IBO Pulse Width (L)	T10	65	1/256fs		ns
$\overline{2DS}$ = L					
CC Pulse Width (H)	T1	130	1/256fs		ns
S/H Acquisition Time	T2	1350	9/256fs		ns
CC-BBC Time	T3	570	4/256fs		ns
BBC Pulse Period	T4	456	3/256fs		ns
BBC Pulse Width (H)	T5	130	1/256fs		ns
BBC Pulse Width (L)	T6	280	2/256fs		ns
BBC-IBO Time	T7	280	2/256fs		ns
IBO Pulse Period	T8	456	3/256fs		ns
IBO Pulse Width (H)	T9	280	2/256fs		ns
IBO Pulse Width (L)	T10	130	1/256fs		ns



SERIAL INPUT TIMING (IBCK, DINL, DINR) WITH $\overline{IMOD}$=H

PARAMETER	SYMBOL	DF1750P/U MIN	TYP	MAX	UNIT
$\overline{2DS}$ = H					
IBCK Pulse Width	t_{IBW}	50	1/256fs		ns
IBCK Pulse Period	t_{IBY}	3/12.928MHz(1)	3/256fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns
$\overline{2DS}$ = L					
IBCK Pulse Width	t_{IBW}	50	1/128fs		ns
IBCK Pulse Period	t_{IBY}	3/12.928MHz(1)	3/128fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns

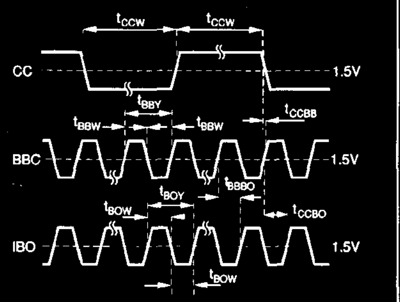


Normally, IBO output is connected to IBCK (Refer to the applications diagram).

NOTE: (1) 12.928MHz = 256 x 50.5kHz (max sampling frequency).

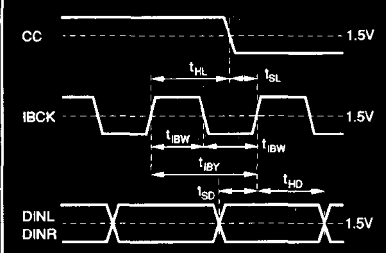
ADC CONTROL SIGNAL TIMING (CC, BBC, AND IBO) WITH $\overline{IMOD}$ = L

PARAMETER	SYMBOL	DF1750P/U MIN	TYP	MAX	UNIT
$\overline{2DS}$ = H					
CC Pulse Width (H)	t_{CCW}		1/8fs		ns
BBC Pulse Width	t_{BBW}	130	1/128fs		ns
BBC Pulse Period	t_{BBY}		1/64fs		ns
IBO Pulse Width	t_{BOW}	130	1/128fs		ns
IBO Pulse Period	t_{BOY}		1/64fs		ns
CC-BBC Time	t_{CCBB}	-5	0	20	ns
CC-IBO Time	t_{CCBO}	130	1/128fs		ns
BBC-IBO Time	t_{BBBO}	130	1/128fs		ns
$\overline{2DS}$ = L					
CC Pulse Width (H)	t_{CCW}		1/4fs		ns
BBC Pulse Width	t_{BBW}	280	1/64fs		ns
BBC Pulse Period	t_{BBY}		1/32fs		ns
IBO Pulse Width	t_{BOW}	280	1/64fs		ns
IBO Pulse Period	t_{BOY}		1/32fs		ns
CC-BBC Time	t_{CCBB}	–5	0	20	ns
CC-IBO Time	t_{CCBO}	280	1/64fs		ns
BBC-IBOTime	t_{BBBO}	280	1/64fs		ns



SERIAL INPUT TIMING (IBCK, DINL, DINR) WITH $\overline{\text{IMOD}}$ = L

PARAMETER	SYMBOL	DF1750P/U			UNIT
		MIN	TYP	MAX	
$\overline{\text{2DS}}$ = H					
IBCK Pulse Width	t_{IBW}	100	1/128fs		ns
IBCK Pulse Period	t_{IBY}	1/3.232MHz(1)	1/64fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns
$\overline{\text{2DS}}$ = L					
IBCK Pulse Width	t_{IBW}	100	1/64fs		ns
IBCK Pulse Period	t_{IBY}	1/3.232MHz(1)	1/32fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns

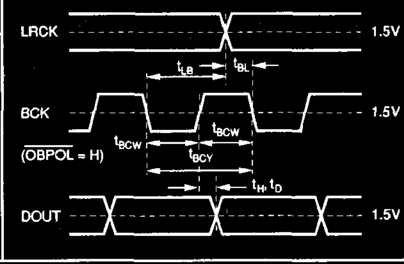


Normally, IBO output is connected to IBCK. (Refer to the application diagram).

NOTE: (1) 3.232MHz = 64 x 50.5kHz (max sampling frequency).

SERIAL OUTPUT TIMING WITH $\overline{\text{FSEN}}$ = H

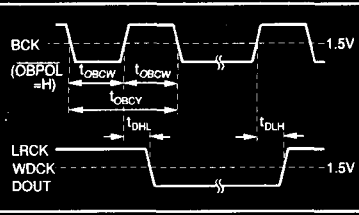
PARAMETER	SYMBOL	DF1750P/U			UNIT	REMARKS
		MIN	TYP	MAX		
BCK Pulse Width	t_{BCW}	100	1/128fs		ns	
BCK Pulse Period	t_{BCY}	1/3.232MHz(1)	1/64fs		ns	
LRCK Pulse Width	t_{LCW}		1/2fs		µs	Duty = 50%
LRCK Pulse Period	t_{LCY}	1/50.5kHz	1/fs		µs	
LRCK Set-up Time	t_{BL}	50			ns	
LRCK Hold Time	t_{LB}	50			ns	
Output Data Hold Time	t_H	0			ns	C_L = 0pF
Output Data Delay Time	t_D			100	ns	C_L = 15pF



NOTE: (1) 3.232MHz = 64 x 50.5kHz (max sampling frequency).

SERIAL OUTPUT TIMING WITH $\overline{\text{FSEN}}$ = L

PARAMETER	SYMBOL	DF1750P/U			UNIT
		MIN	TYP	MAX	
BCK Pulse Width	t_{OBCW}	140	1/128fs		ns
BCK Pulse Period	t_{OBCY}		1/64fs		ns
WDCK Pulse Width	t_{WDCW}		1/4fs		µs
WDCK Pulse Period	t_{WDCY}		1/2fs		µs
LRCK Pulse Width	t_{LRCW}		1/2fs		µs
LRCK Pulse Period	t_{LRCY}		1/fs		µs
Output Data Delay Time	t_{DHL}	–10		30	ns
	t_{DLH}	–10		30	ns



THEORY

According to the Nyquist Theorem, digital audio recordings sampled at a rate of 44.1kHz (CD) or 48kHz (DAT) should accurately reproduce the full 20kHz audio bandwidth. Unfortunately, if frequencies higher than 1/2 the sample rate are seen at the input of an analog-to-digital converter, aliasing back into the baseband will occur. At these sample frequencies, the way to assure that aliasing does not occur is to use complicated high order filters at the input of the ADC. These filters can be expensive and they can also have undesirable phase characteristics. These problems can be avoided by using an oversampling ADC (such as the PCM1750) with a decimating filter, where a high order filter can be replaced with a low order filter which has very little phase distortion (Figure 1).

With the oversampling-decimating technique, the input signal (Figure 2a) is band limited by a low order analog low-pass filter as shown in Figure 2b. This signal is 4-times oversampled, with its spectra and foldover noise shown in Figure 2c. The DF1750 first rejects the high frequency components of the 4fs ADC output (Figure 2d). A 1/2 decimating filter then processes this data into a 2fs data stream. This output spectra is shown in Figure 2e. The high frequency components of the 2fs data are then removed, producing the output spectra shown in Figure 2f. A second 1/2 decimating filter processes the 2fs data to a final fs data stream and the original signal is restored without distortion (Figure 2g). Note, when operating in the 1/2 decimating mode the DF1750 processes data through the first LPF and a single 1/2 decimating filter only.

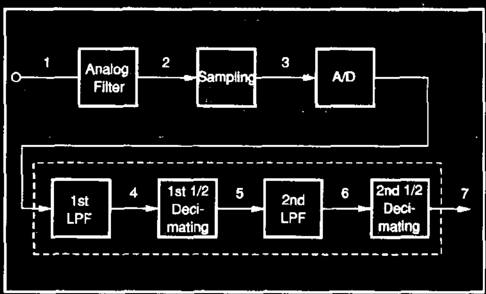


FIGURE 1. A Block Diagram of an Oversampling ADC Followed by Digital Decimation.

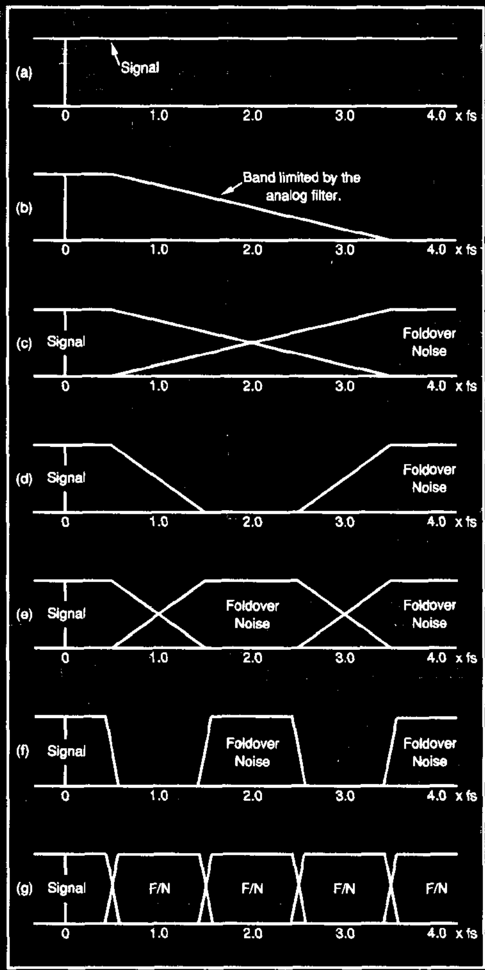


FIGURE 2. The Associated Spectra of the Oversampling-Decimating Technique.

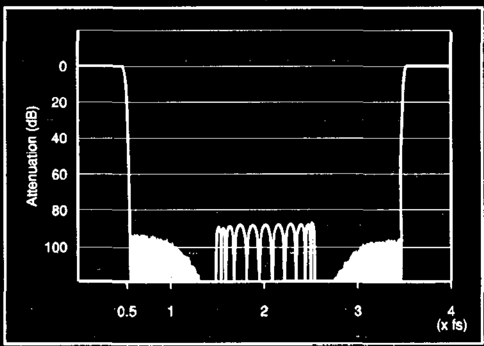
THEORETICAL FILTER CHARACTERISTICS

1/4 DECIMATING, INPUT DATA FREQUENCY = 4fs

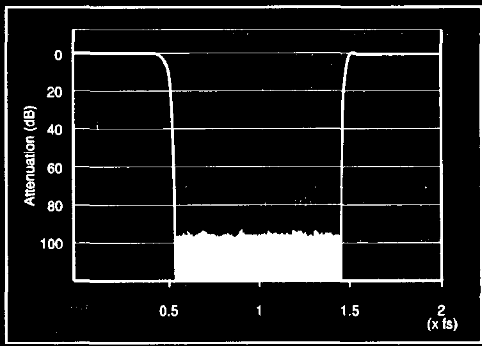
PARAMETER	CHARACTERISTICS
Passband	DC to 0.4583fs
Stopband	0.5417fs and Above
Passband Ripple	±0.0005 dB
Stopband Attenuation	95dB min, 0.5417fs to 1.4583fs 88dB min, 1.4583fs to 2.5417fs 95dB min, 2.5417fs to 3.4583fs
Group Delay Time	Constant, Linear Phase

1/2 DECIMATING, INPUT DATA FREQUENCY = 2fs

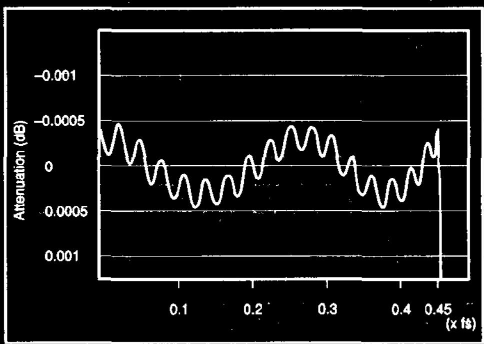
PARAMETER	CHARACTERISTICS
Passband	DC to 0.4583fs
Stopband	0.5417fs and above
Passband Ripple	±0.0002dB
Stopband Attenuation	95dB min, 0.5417fs to 1.4583fs
Group Delay Time	Constant, Linear Phase



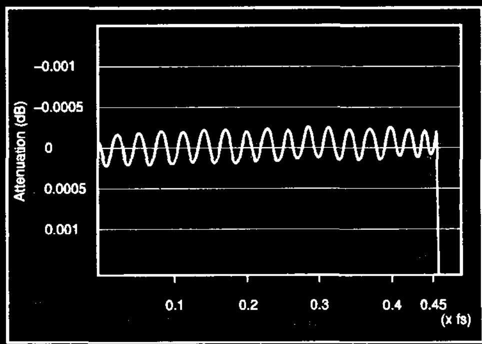
DF1750 1/4 Decimating Filter Tranfer Characteristics.



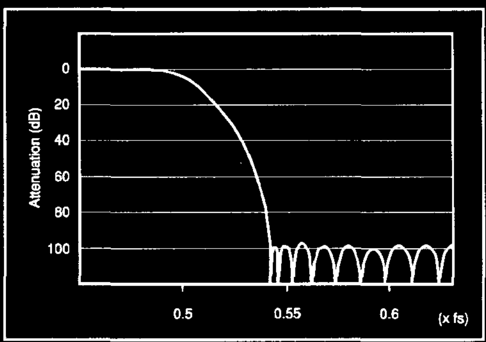
DF1750 1/2 Decimating Filter Transfer Characteristics.



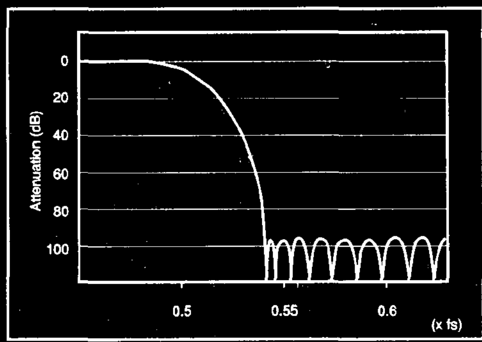
DF1750 1/4 Decimating Passband Frequency Response.



DF1750 1/2 Decimating Passband Frequency Response.



DF1750 1/4 Decimating Transitionband Frequency Response.



DF1750 1/2 Decimating Transitionband Frequency Response.

FUNCTIONAL DESCRIPTION

1/4 AND 1/2 DECIMATING FUNCTIONS

1/4 or 1/2 decimating filtering converts 4fs or 2fs oversampled data back to a sampling rate of fs data by a digital filtering algorithm. $\overline{2DS}$ is used to select 1/4 or 1/2 decimating.

$\overline{2DS}$ = H; 1/4 decimating (0.5417fs ~ 3.4583fs)
$\overline{2DS}$ = L; 1/2 decimating (0.5417fs ~ 1.4583fs)

The filter arithmetic block consists of two 1/2 decimating finite impulse response (FIR) filters as shown in Figure 3.

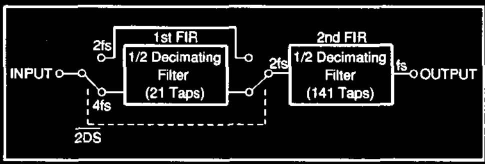


FIGURE 3. Filter Arithmetic Structure

SYSTEM CLOCK

The system clock frequency can be 256fs, 364fs, 512fs, or 768fs selectable with $\overline{SCSL1}$ and $\overline{SCSL2}$ as indicated in Table I. An external clock (applied to Pin XTI) or crystal oscillator (Pins XTI and XTO) can be employed. AC coupling is required for an external clock.

The XTI input clock is available as an output at pin CKO, when $\overline{CKEN}$ = L. CKO stays low when $\overline{CKEN}$ = H.

$\overline{SCSL1}$		H		L	
$\overline{SCSL2}$		H	L	H	L
XTI Clock Frequency	F_{XI}	512fs	256fs	768fs	384fs
Clock Input		External Clock or Crystal Oscillator			
Internal System Clock Frequency	F_{SYS}	256fs			

TABLE I. System Clock and Internal Clock Frequency Selection.

SERIAL DATA INPUT

The DF1750 is programmed for accepting the correct number of input data bits per word by the $\overline{IMOD}$ pin. A 16-bit input word is selected with $\overline{IMOD}$ = L and an 18-bit input word is selected with $\overline{IMOD}$ = H. Set $\overline{IMOD}$ = H for use with the PCM1750. The serial input data format is two's complement and MSB first. Both the left and right channel data are loaded into the DF1750 simutaneously.

Each bit of the data is loaded to each channel's SIPO (Serial/parallel conversion register) by the rising edge of the Input Bit Clock, IBCK (Figure 4). After the serial input data is loaded, the data is latched into a parallel register by the rising edge of CC for $\overline{IMOD}$ = H and the falling edge of CC for $\overline{IMOD}$ = L (Figure 5).

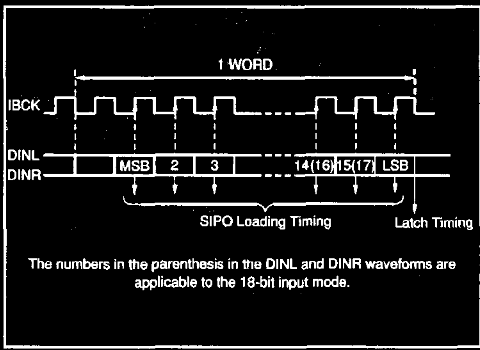


FIGURE 4. SIPO Input Data Loading Timing.

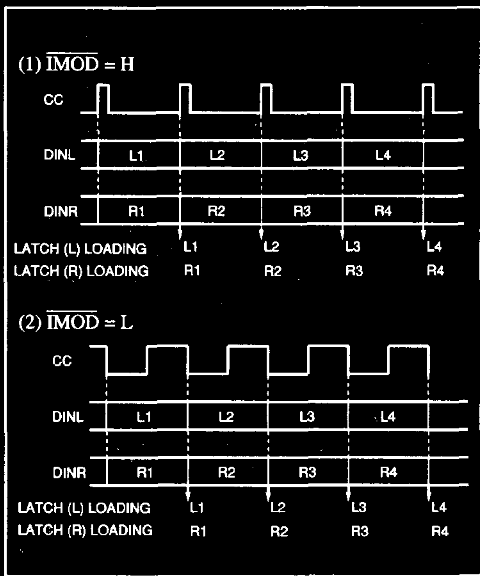


FIGURE 5. Input Data Latch/Loading Timing.

ADC CONTROL SIGNALS (CC, BBC, AND IBO) WITH $\overline{\text{IMOD}}$ = H

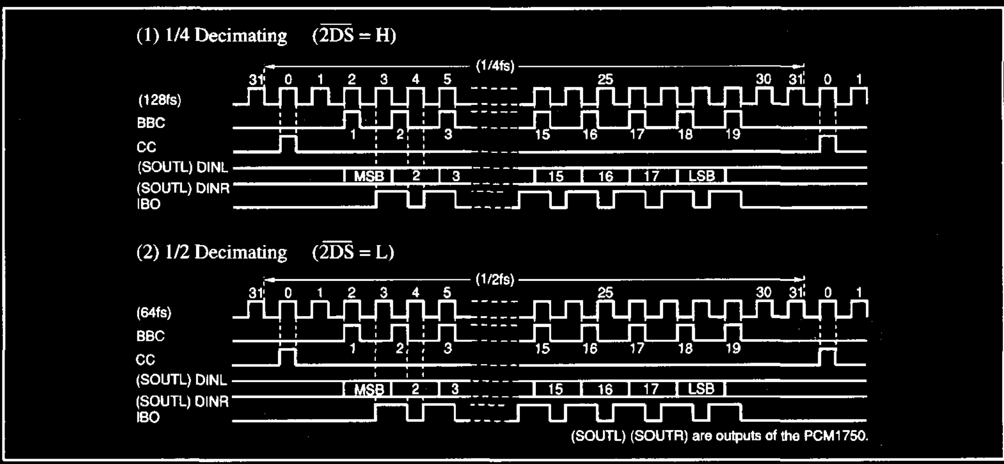


FIGURE 6. ADC Control Signals With $\overline{\text{IMOD}}$ = H. (Applicable for use with the Burr-Brown PCM1750 ADC).

ADC CONTROL SIGNALS (CC, BBC AND IBO) WITH $\overline{\text{IMOD}}$ = L

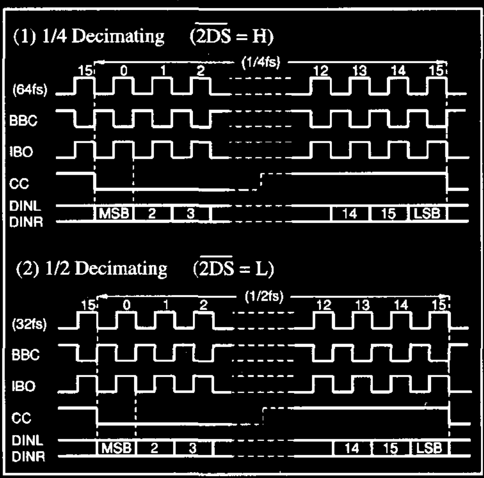


FIGURE 7. ADC Control Signals with $\overline{\text{IMOD}}$ = L.

OUTPUT INTERFACE (BCK, WDCK, LRCK, $\overline{\text{OBPOL}}$, $\overline{\text{LRPOL}}$, $\overline{\text{FSEN}}$)

The output of the DF1750 can be interfaced to many different devices by programming the output interface pins. These pins provide the following functions:

a. Output control clocks, BCK, WDCK, LRCK I/O selection ($\overline{\text{FSEN}}$).

$\overline{\text{FSEN}}$ = H; BCK WDCK, LRCK = Input
$\overline{\text{FSEN}}$ = L; BCK WDCK, LRCK = Output

b. Sampling rate clock (LRCK)
When $\overline{\text{FSEN}}$ = H, apply a 50% duty cycle sampling frequency (fs) to pin LRCK.
When $\overline{\text{FSEN}}$ = L, a fs clock generated from the system clock is available at pin LRCK.

c. Word Clock (WDCK)
When $\overline{\text{FSEN}}$ = L, WDCK provides a 2fs clock that is derived from the system clock.

d. Output bit clock
When $\overline{\text{FSEN}}$ = H, apply a 64fs clock to pin BCK.
When $\overline{\text{FSEN}}$ = L, a 64fs clock generated from the system clock is available at pin BCK.

e. LRCK polarity selection ($\overline{\text{LRPDL}}$)
$\overline{\text{LRPOL}}$ = H; Lch/Rch = Low/High
$\overline{\text{LRPOL}}$ = L; Lch/Rch = High/Low
(Regardless of LRCK's I/O mode).

f. BCK polarity selection ($\overline{\text{OBPOL}}$)
$\overline{\text{OBPOL}}$ = H; DOUT changes state at rising edge of BCK.
$\overline{\text{OBPOL}}$ = L; DOUT changes state at falling edge of BCK.
(Regardless of BCK's I/O mode).

g. Timing relation between XTI and BCK, WDCK, LRCK clocks.
When $\overline{\text{FSEN}}$ = H, clocks to BCK and LRCK must be synchronized to XTI. However, there is no limit on their phase differences (between XTI and BCK, LRCK clocks).

SERIAL DATA OUTPUT

The number of bits per output data word is selected with the OW20 pin. With OW20 = H a 16-bit output is selected and with OW20 = L a 20-bit output is selected.

The serial output data format is two's complement and MSB first. The left and right channel outputs are alternated, with the left channel preceeding the right channel. Each data word is allocated in each pulse of LRCK and the LSB is located at the end of the LRCK pulse as shown in Figure 8.

The output of the DF1750 can be muted by the use of the MUTE pin. When MUTE = L, the output stays low (muted). Under normal operation MUTE = H.

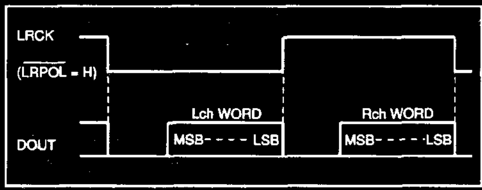
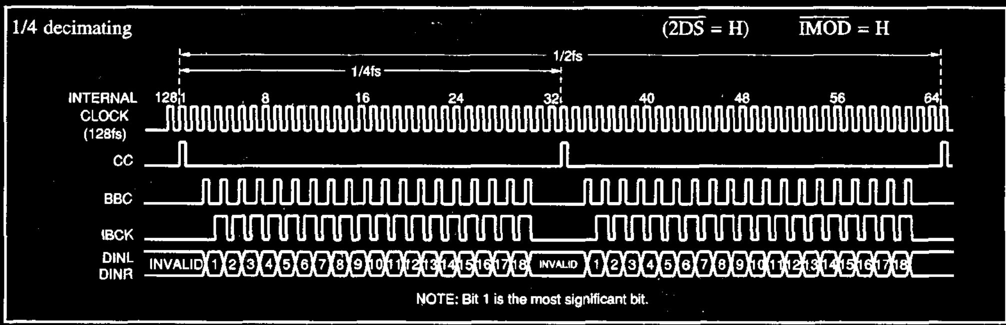
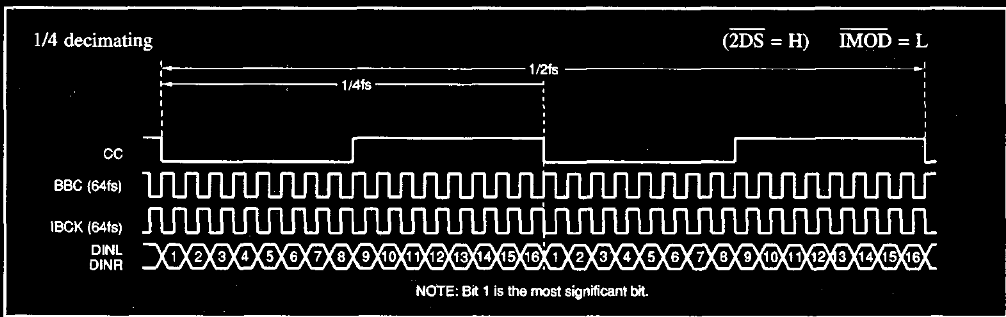


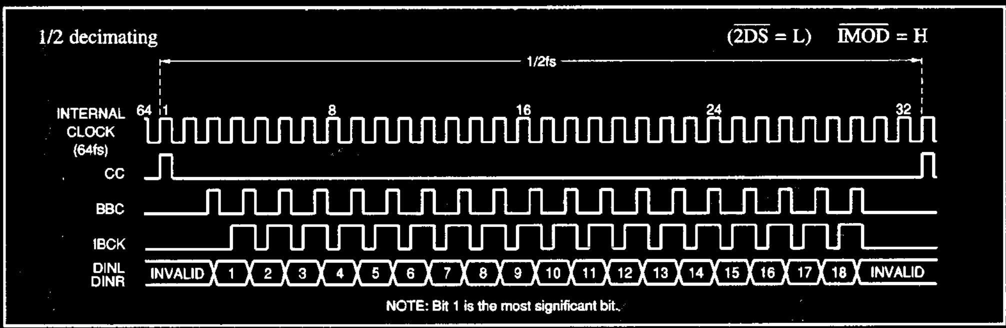
FIGURE 8. Output Timing.

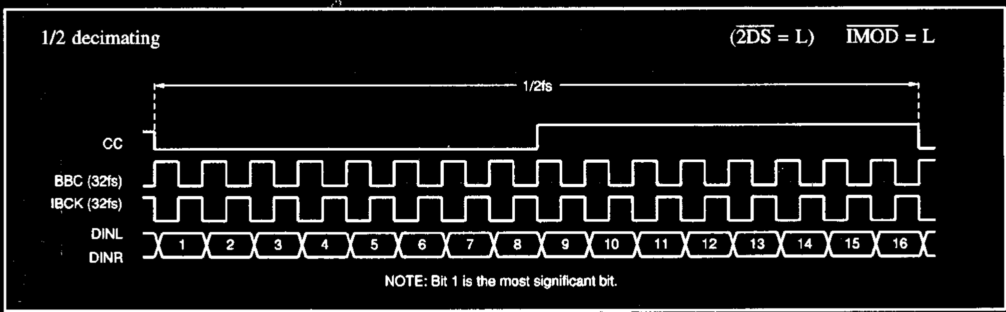
TIMING DIAGRAMS

INPUT

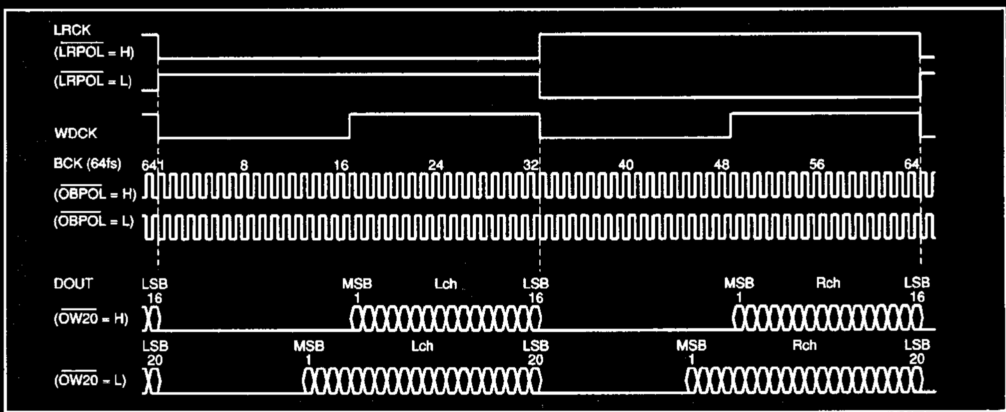








OUTPUT



APPLICATIONS

A typical circuit configuration for digital audio recording is shown in Figure 9. Each of the stereo input channels passes through a six pole Generalized Immitance Converter (GIC) low pass analog filter. This filter features extremely low distortion and negligible phase shift. The band limited signals are 4X oversampled by the dual-channel PCM1750 A/D converter. Clock and convert signals are provided to the PCM1750 by the DF1750. The 4fs oversampled data of the PCM1750 is filtered by the DF1750 to provide a data stream of fs. A PCM1750/DF1750 evaluation board, DEM1133, is available from Burr-Brown. This board incorporates the features mentioned above as well as an AES/EBU interface, test points for monitoring both the serial and parallel data outputs, and a breadboard area for user experimentation.

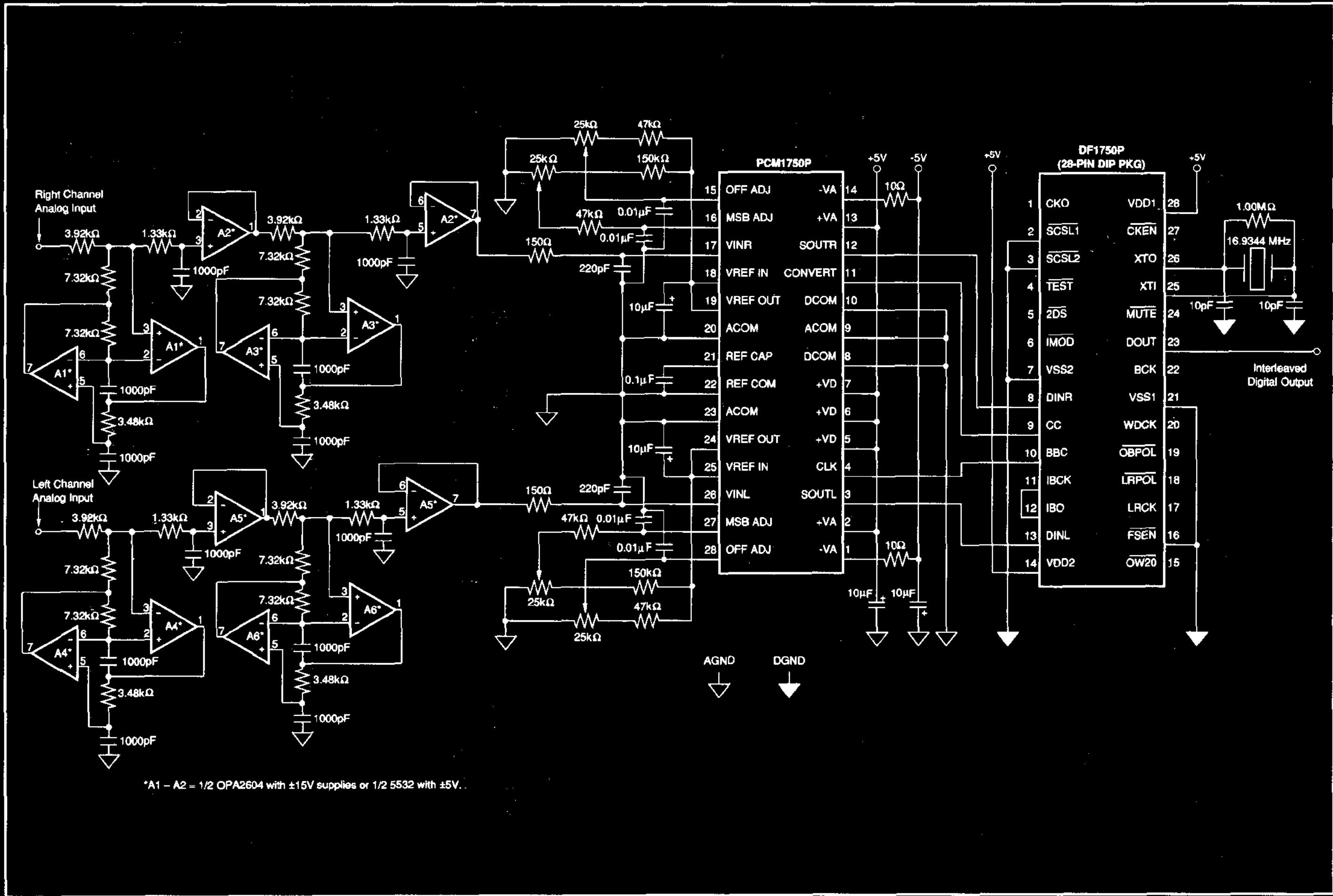


FIGURE 9. Circuit diagram for a typical digital audio application using the DF1750 for decimating oversampled data from the output of the PCM1750 dual channel ADC. The OPA2604s are configured in a generalized immittence converter (GIC) filter arrangement to avoid aliasing in the PCM1750.