National Semiconductor

5475/DM5475/DM7475
Quad Latches

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.
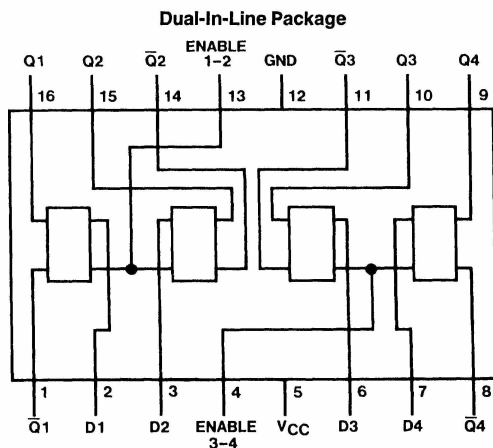
These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch and are available in 16-pin packages.

Features

■ Alternate Military/Aerospace device (5475) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

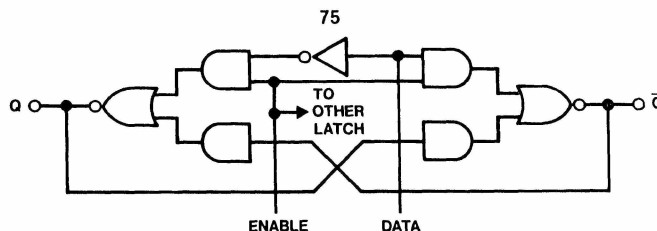**Dual-In-Line Package**

TL/F/6527–1

Order Number 5475DMQB, 5475FMQB, DM5475J, DM5475W or DM7475N
See NS Package Number J16A, N16E or W16A

Function Table (Each Latch)

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care, Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagram (Each Latch)

TL/F/6527–2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	$-55°C$ to $+125°C$
DM74	$0°C$ to $+70°C$
Storage Temperature Range	$-65°C$ to $+150°C$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM5475			DM7475			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			-0.4			-0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
t_W	Enable Pulse Width (Note 4)	20			20			ns
t_{SU}	Setup Time (Note 4)	20			20			ns
t_H	Hold Time (Note 4)	5			5			ns
T_A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = $ Min, $I_I = -12$ mA				-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = $ Min, $I_{OH} = $ Max $V_{IL} = $ Max, $V_{IH} = $ Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = $ Min, $I_{OL} = $ Max $V_{IH} = $ Min, $V_{IL} = $ Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = $ Max, $V_I = 5.5$V				1	mA
I_{IH}	High Level Input Current	$V_{CC} = $ Max, $V_I = 2.4$V				80	μA
I_{IL}	Low Level Input Current	$V_{CC} = $ Max, $V_I = 0.4$V				-3.2	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = $ Max (Note 2)	DM54	-20		-55	mA
			DM74	-18		-55	
I_{CC}	Supply Current	$V_{CC} = $ Max (Note 3)	DM54		32	46	mA
			DM74		32	50	

Note 1: All typicals are at $V_{CC} = 5$V, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: $T_A = 25°C$ and $V_{CC} = 5$V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15\,pF$		Units
			Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Q		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	G to Q		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	G to Q		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	G to $\overline{Q}$		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	G to $\overline{Q}$		30	ns