National Semiconductor

DM54L93
Decade, Divide-by-12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

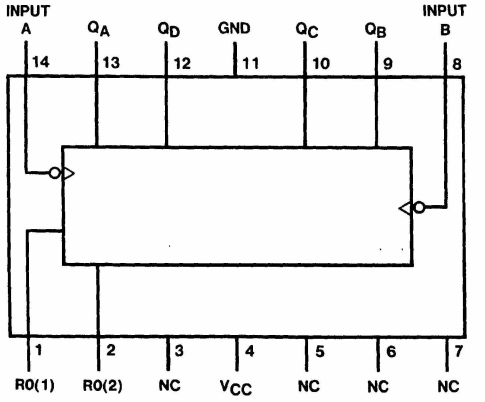
To use their maximum count length (decade, divide-by-twelve, or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table.

Features

- Typical power dissipation 16 mW
- Count frequency 15 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6637–1

Order Number DM54L93J or DM54L93W
See NS Package Number J14A or W14B

Function Tables

COUNT SEQUENCE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

RESET/COUNT TRUTH TABLE (Note B)

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B

Note B: H = High Level, L = Low Level, X = Don't Care.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L93			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 5)		0		6	MHz
t_W	Pulse Width (Note 5)	A	90			ns
		B	90			
		Reset	200			
t_{REL}	Reset Release time (Note 5)		200			ns
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 4)			0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	Reset			0.1	mA
			A			0.2	
			B			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			10	μA
			A			20	
			B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Reset			−0.18	mA
			A			−0.36	
			B			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				5.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

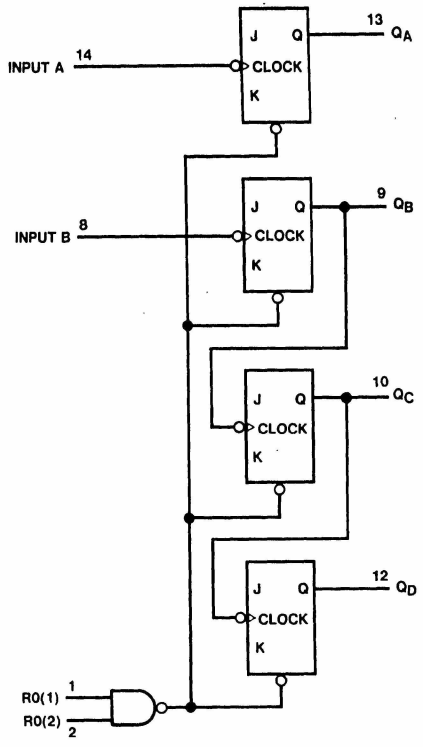
Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		400	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		400	ns

Logic Diagram



TL/F/6637–2

The J and K inputs shown without connection are for reference only and are functionally at a high level.