

# DM54LS502,DM74LS502

*DM54LS502 DM74LS502 8-Bit Successive Approximation Register*



Literature Number: SNOS311A

## DM54LS502/DM74LS502 8-Bit Successive Approximation Register

### General Description

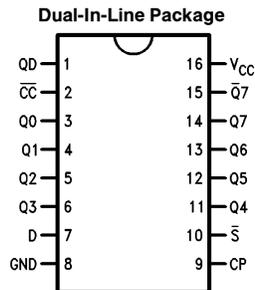
The LS502 is an 8-bit register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete ( $\overline{CC}$ ) signal coincident with storage of the eighth bit. An active LOW Start (S) input performs synchronous initialization which forces Q7 LOW and all other outputs HIGH. Subsequent clocks shift this Q7 LOW signal downstream which simultaneously backfills the register such that the first serial data (D input) bit is stored in Q7, the second bit in Q6, the third in Q5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on Q<sub>D</sub>.

Designed primarily for use in the successive approximation technique for analog-to-digital conversion, the LS502 can also be used as a serial-to-parallel converter ring counter and as the storage and control element in recursive digital routines.

### Features

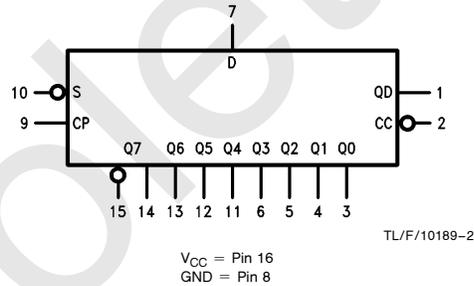
- Low power Schottky version of 2502
- Storage and control for successive approximation A to D conversion
- Performs serial-to-parallel conversion

### Connection Diagram



Order Number DM54LS502J, DM54LS502W,  
DM74LS502WM or DM74LS502N  
See NS Package Number J16A, M16B, N16E or W16A

### Logic Symbol



Pin Names	Description
D	Serial Data Input
$\overline{S}$	Start Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q <sub>D</sub>	Synchronized Serial Data Output
$\overline{CC}$	Conversion Complete Output (Active LOW)
Q0–Q7	Parallel Register Outputs
$\overline{Q7}$	Complement of Q7 Output

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	-55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	DM54LS502			DM74LS502			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.8	V
I <sub>OH</sub>	High Level Output Current			-0.4			-0.4	mA
I <sub>OL</sub>	Low Level Output Current			4			8	mA
T <sub>A</sub>	Free Air Operating Temperature	-55		125	0		70	°C
t <sub>s</sub> (H)	Setup Time HIGH or LOW	5			16			ns
t <sub>s</sub> (L)	$\bar{S}$ to CP	5			16			ns
t <sub>h</sub> (H)	Hold Time HIGH or LOW	5			0			ns
t <sub>h</sub> (L)	$\bar{S}$ to CP	5			0			ns
t <sub>s</sub> (H)	Setup Time HIGH or LOW	5			8			ns
t <sub>s</sub> (L)	D to CP	5			8			ns
t <sub>h</sub> (H)	Hold Time HIGH or LOW	5			10			ns
t <sub>h</sub> (L)	D to CP	5			10			ns
t <sub>w</sub> (H)	CP Pulse Width HIGH or LOW	20			46			ns
t <sub>w</sub> (L)		20			46			ns

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max	DM54	2.5		V
			DM74	2.7		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min	DM54		0.4	V
			DM74		0.5	
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min	DM74		0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V V <sub>I</sub> = 10V	DM74 DM54		0.1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			20	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			-0.8	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	DM54	-20	-100	mA
			DM74	-20	-100	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max			65	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics $V_{CC} = +5.0V, T_A = +25^\circ C$

Symbol	Parameter	DM54LS502		DM74LS502		Units
		$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$				
		Min	Max	Min	Max	
$f_{max}$	Maximum Clock Frequency	25		15		MHz
$t_{PLH}$	Propagation Delay		35		35	ns
$t_{PHL}$	CP to $Q_n$ or $\overline{CC}$		25		25	

## Functional Description

The register stages are composed of transparent RS latches arranged in master/slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals  $\phi_1$  and  $\phi_2$  derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.

Initializing the register requires a LOW signal on  $\overline{S}$  while exercising CP. With  $\overline{S}$  and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with  $\overline{S}$  remaining LOW, then forces the slave latches to the condition wherein Q7 is LOW and all other register outputs, including  $\overline{CC}$ , are HIGH. This condition will prevail as long as  $\overline{S}$  remains LOW, regardless of subsequent CP rising edge. To start the conversion process,  $\overline{S}$  must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to  $Q_D$  and Q7, while Q6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches  $\overline{CC}$ , the register is locked up and no further changes can occur until the register is initialized for the next conversion process.

Figure a shows a simplified hook-up of a LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8-bit binary number by the successive approximation technique. Figure b is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time  $t_1$ , Q7 is LOW and Q6–Q0 are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the LS502) will be LOW, and at times  $t_2$  the D/A output will rise to three-fourths of full scale because Q7 will remain LOW and contribute 50% while Q6 is forced LOW and contributes another 25%. On the other hand, if the analog input voltage is less than one-half of full scale, the comparator output will be HIGH and Q7 will go HIGH at  $t_2$ . Q6 will still be forced LOW at  $t_2$ , and the D/A output will decrease to 25% of full scale. Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at  $t_9$ , the binary number represented by the register outputs will be the numerator of the fraction  $n/256$ , representing the analog input voltage as a fraction of the full scale output D/A converter.

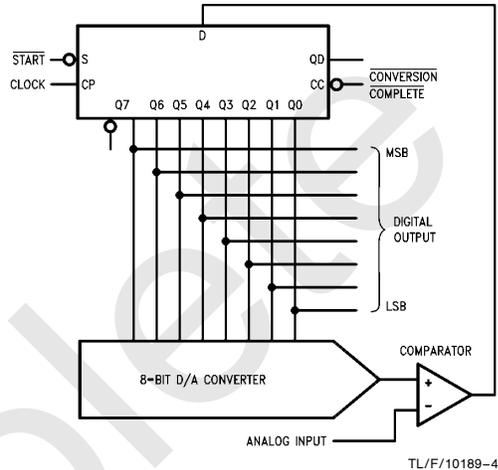


FIGURE a.

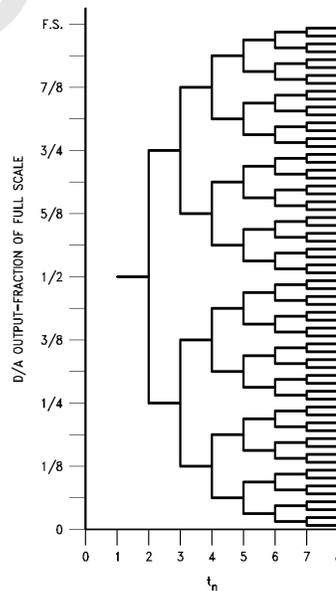


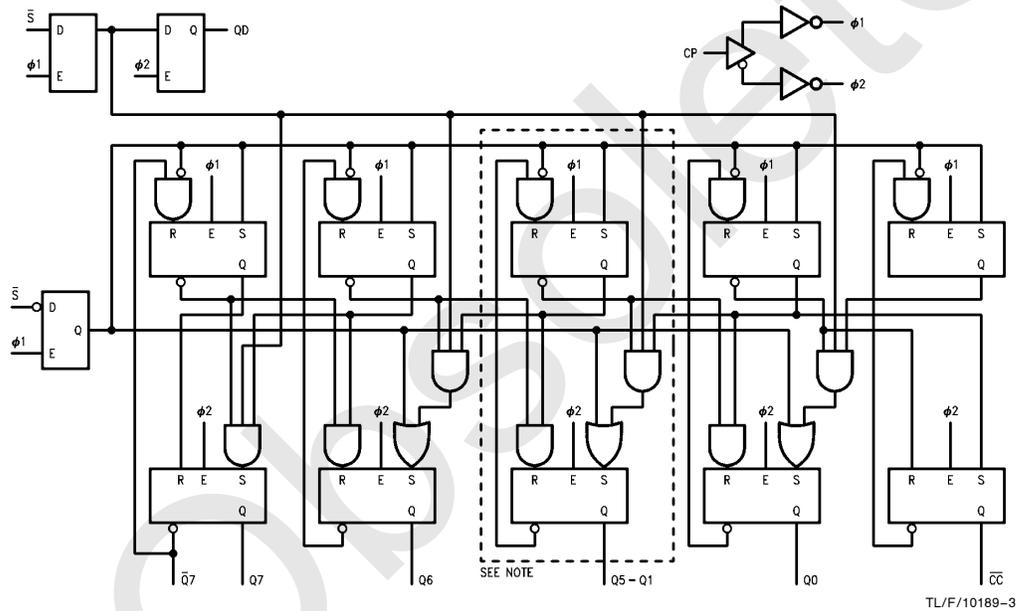
FIGURE b.

## Truth Table

Time $t_n$	Inputs		Outputs									
	D	$\bar{S}$	$Q_D$	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	X	L	H	H	H	H	H	H	H	H
2	D6	H	D7	D7	L	H	H	H	H	H	H	H
3	D6	H	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	H	X	D7	D6	D5	D4	D3	D2	D1	D0	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

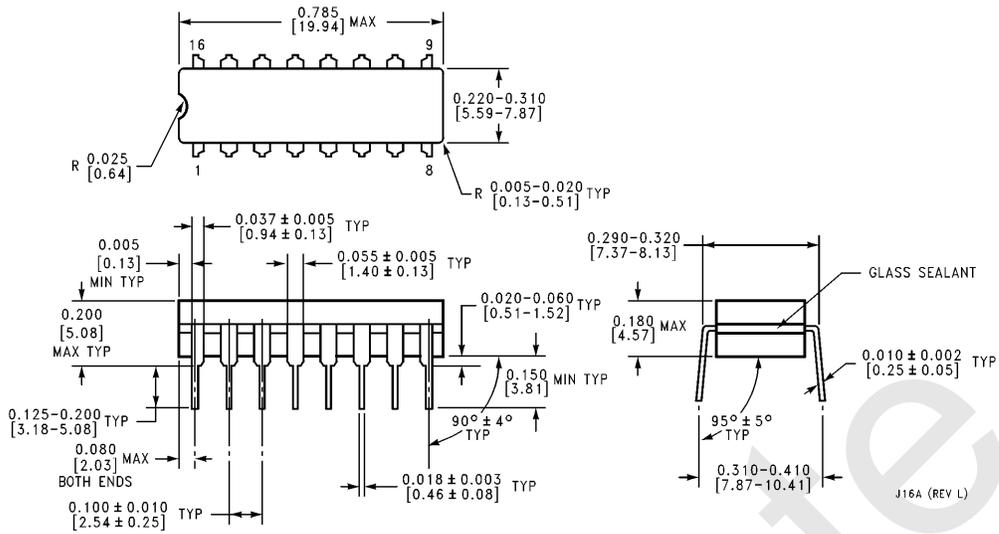
## Logic Diagram



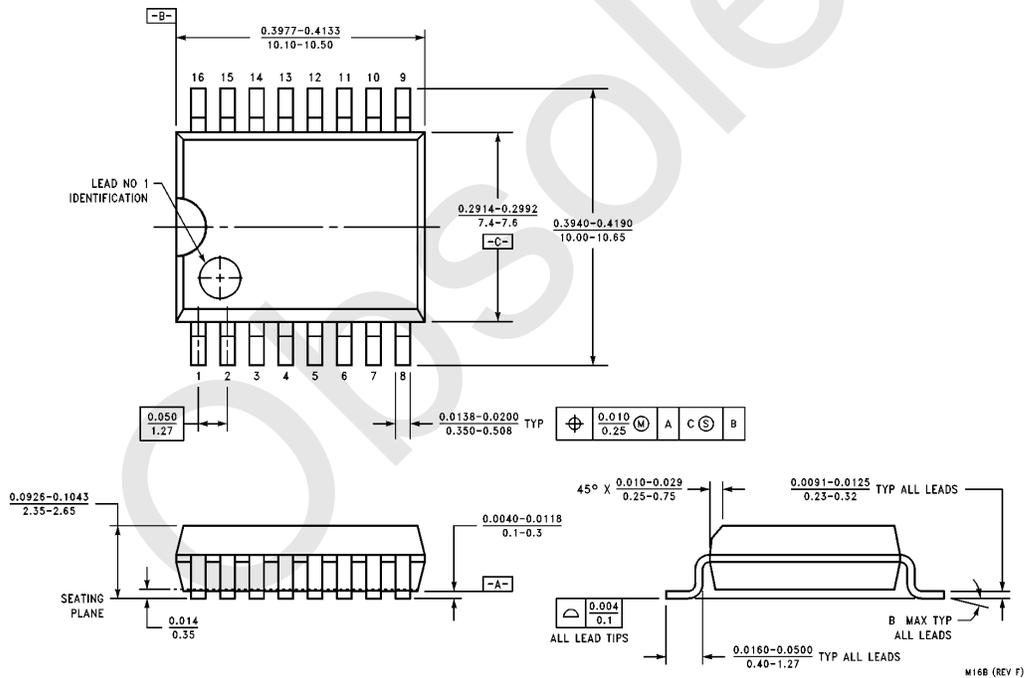
**Note:** Cell logic is repeated for register stages Q5 to Q1.

TL/F/10189-3

**Physical Dimensions** inches (millimeters)

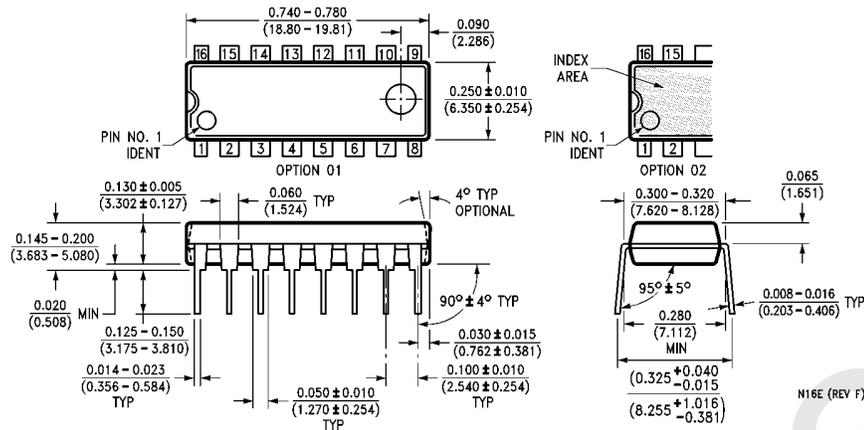


**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number DM54LS502J**  
**NS Package Number J16A**

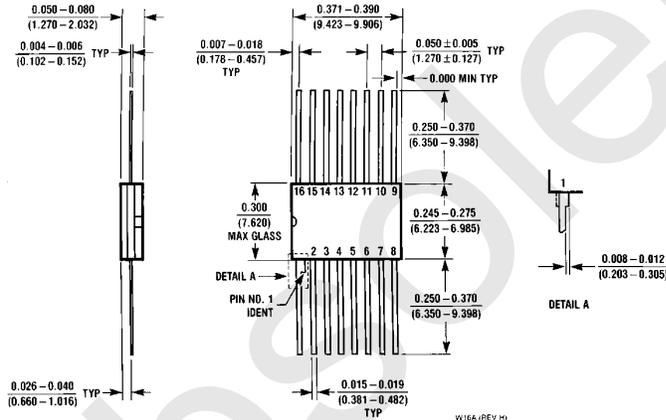


**16-Lead Wide Small Outline Molded Package (M)**  
**Order Number DM74LS502WM**  
**NS Package Number M16B**

**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74LS502N**  
**NS Package Number N16E**



**16-Lead Ceramic Flat Package (W)**  
**Order Number DM54LS502W**  
**NS Package Number W16A**

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