National Semiconductor

DM54S161/DM74S161, DM54S163/DM74S163 Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. They are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input.

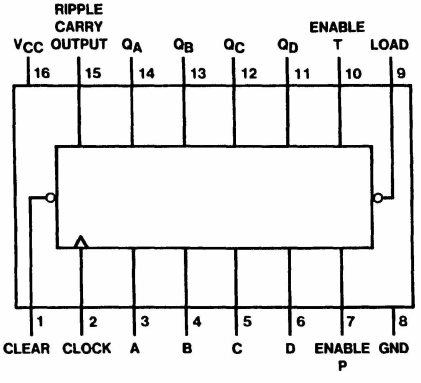
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

Connection Diagram

Dual-In-Line Package



TL/F/6471–1

Order Number DM54S161J, DM54S163J, DM54S161W, DM74S161N, or DM74S163N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions See Section 1 for Test Waveforms and Output Load

Symbol	Parameter		DM54S161/163			DM74S161/163			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0		40	0		40	MHz
	Clock Frequency (Note 2)		0		35	0		35	
t_w	Pulse Width (Note 1)	Clock	10			10			ns
		Clear (Note 4)	10			10			
	Pulse Width (Note 2)	Clock	12			12			
		Clear (Note 4)	12			12			
t_{SU}	Setup Time (Note 1)	Data	4			4			ns
		Enable P or T	12			12			
		Load	14			14			
		Clear (Note 3)	14			14			
	Setup Time (Note 2)	Data	5			5			
		Enable P or T	14			14			
		Load	16			16			
		Clear (Note 3)	16			16			
t_H	Hold Time (Note 1)	Data	3			3			ns
		Others	0			0			
	Hold Time (Note 2)	Data	5			5			
		Others	2			2			
t_{REL}	Load or Clear Release Time (Note 1)		12			12			ns
	Load or Clear Release Time (Note 2)		14			14			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: Applies only to the 'S163 which has synchronous clear inputs.

Note 4: Applies only to the 'S161 which has asynchronous clear inputs.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	Low Level Input Current	V_{CC} = Max, V_I = 2.7V	CLK, Data			50	µA
			Others	−10		−200	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Enable T			−4	mA
			Others			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			95	160	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		40		35		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		25		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		25		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		15		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		15		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 3)	Clear to Any Q		20		24	ns

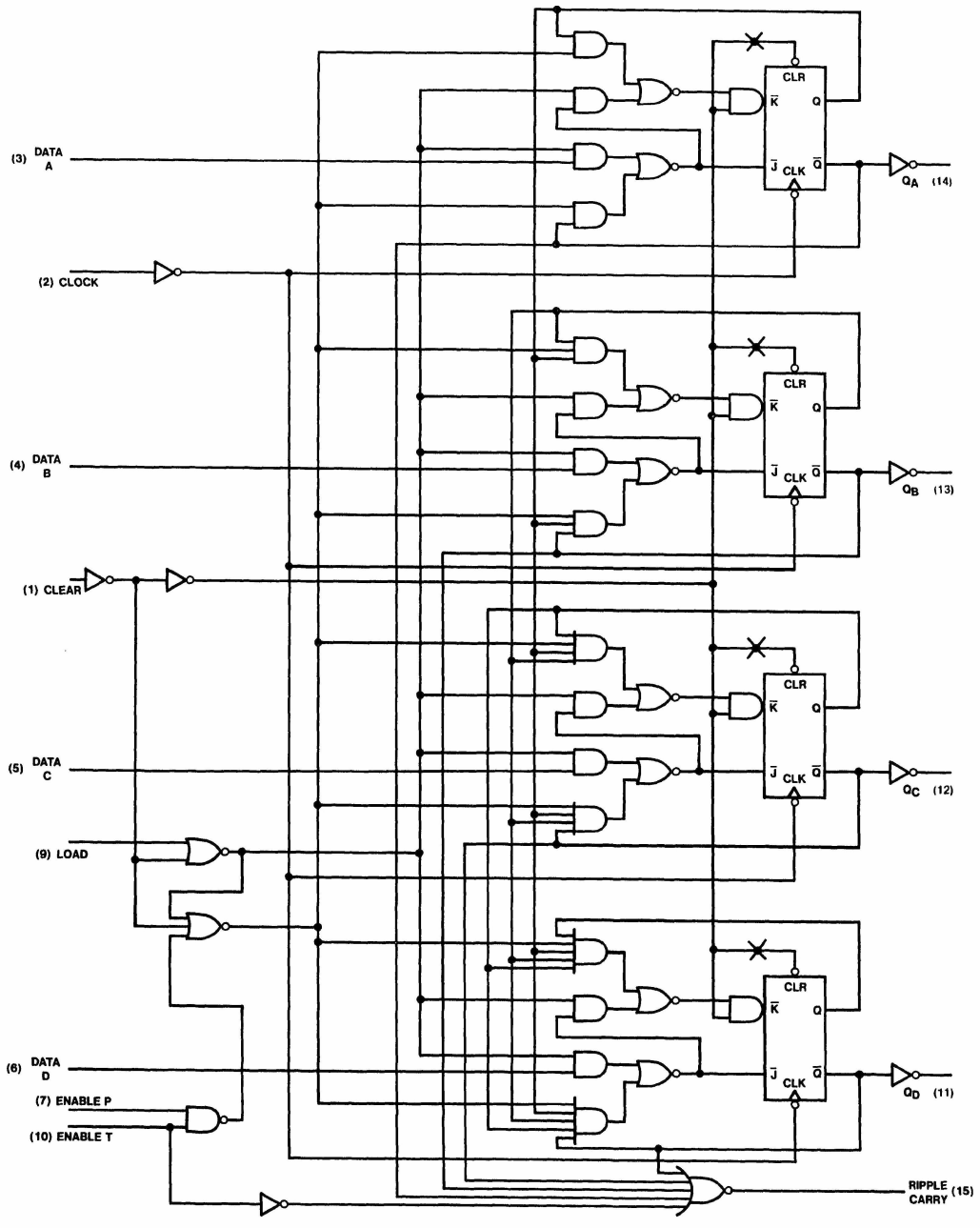
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Propagation delay for clearing is measured from clear input for the 'S161 and from the clock input transition for the 'S163.

Logic Diagram

S161, S163

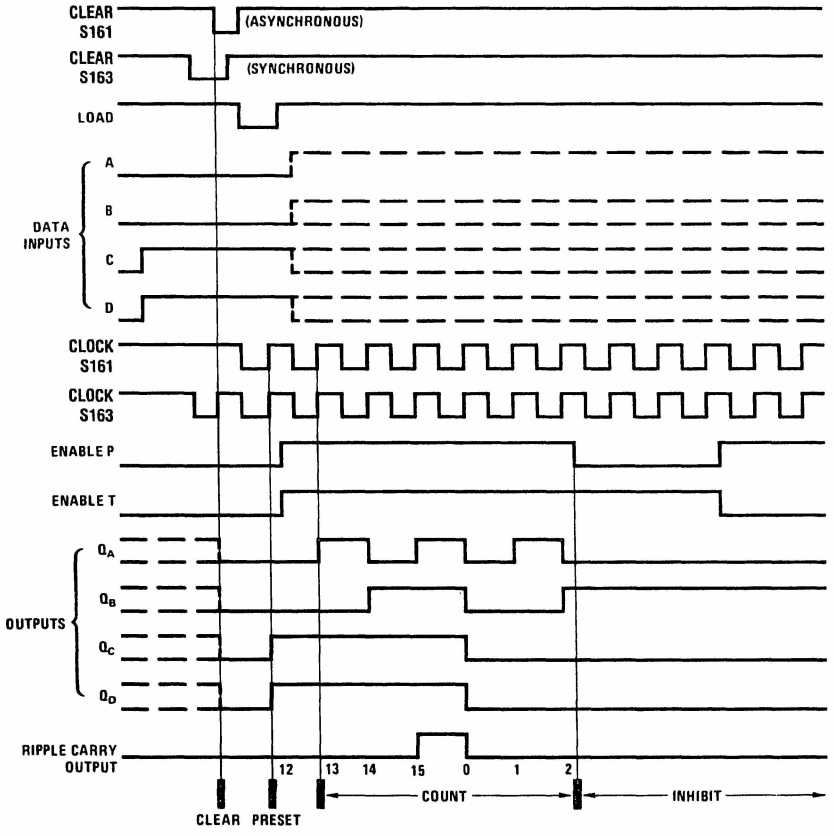


✕ S161 option

TL/F/6471–2

Timing Diagram

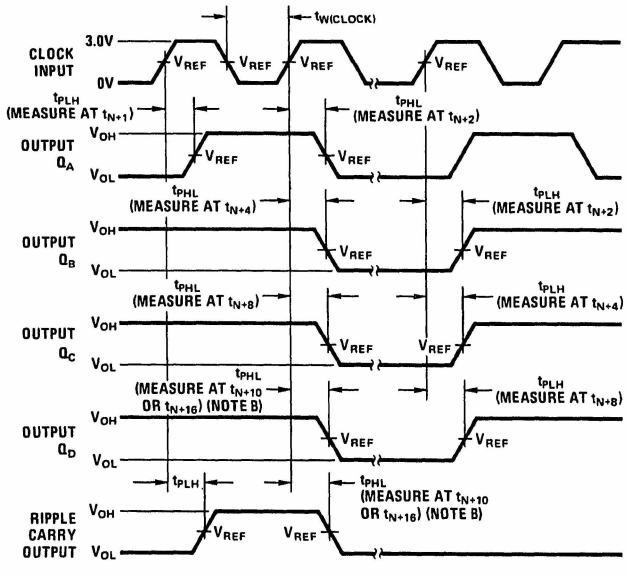
S161, S163 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



TL/F/6471–3

Parameter Measurement Information

Switching Time Waveforms



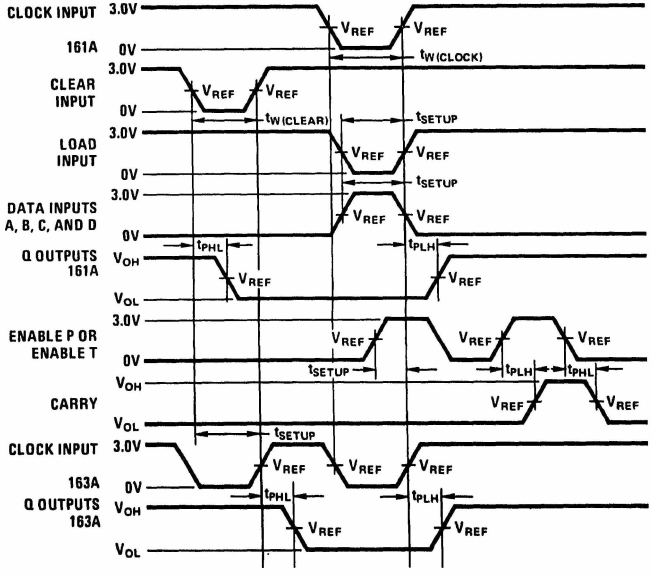
TL/F/6471–4

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For S161/163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at $t_n + 16$ for S161, S163 where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Switching Time Waveforms



TL/F/6471–5

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at $t_n + 0$.

Note C: $V_{REF} = 1.5V$.