National Semiconductor

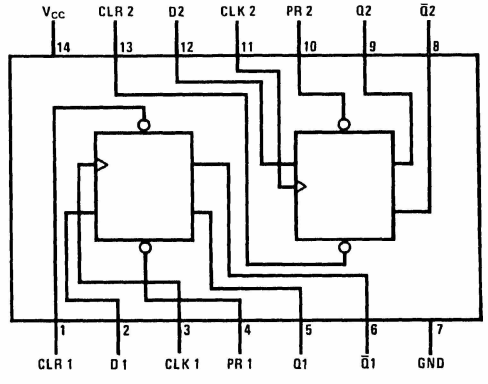
DM54S74/DM74S74
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6457–1

Order Number DM54S74J, DM54S74W, DM74S74M or DM74S74N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↑ = Positive-going Transition
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.
Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S74			DM74S74			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	110	75	0	110	75	MHz
f_{CLK}	Clock Frequency (Note 3)		0	95	65	0	95	65	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	7.3			7.3			
		Clear Low	7			7			
		Preset Low	7			7			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	9			9			
		Clear Low	9			9			
		Preset Low	9			9			
t_{SU}	Setup Time (Notes 1 & 2)		3↑			3↑			ns
t_{SU}	Setup Time (Notes 1 & 3)		3↑			3↑			ns
t_H	Input Hold Time (Notes 1 & 2)		2↑			2↑			ns
t_H	Input Hold Time (Notes 1 & 3)		2↑			2↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge at the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D			50	μA
			Clear			150	
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	D			−2	mA
			Clear			−6	
			Preset			−4	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		75		65		MHz
$t_{P'H}$	Propagation Delay Time Low to High Level Output	Preset to Q		6		9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		6		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock High)	Preset to $\overline{Q}$		13.5		17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock Low)	Preset to $\overline{Q}$		8		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock High)	Clear to Q		13.5		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock Low)	Clear to Q		8		13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		9		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		9		14	ns