



Gates, Series 54/74

DM7450, DM7451, DM7453, DM7454, DM7460

DM7450 (SN7450) expandable dual 2-wide 2-input AND-OR-INVERT gate
DM7451 (SN7451) dual 2-wide 2-input AND-OR-INVERT gate
DM7453 (SN7453) expandable 4-wide 2-input AND-OR-INVERT gate
DM7454 (SN7454) 4-wide 2-input AND-OR-INVERT gate
DM7460 (SN7460) dual 4-input expander

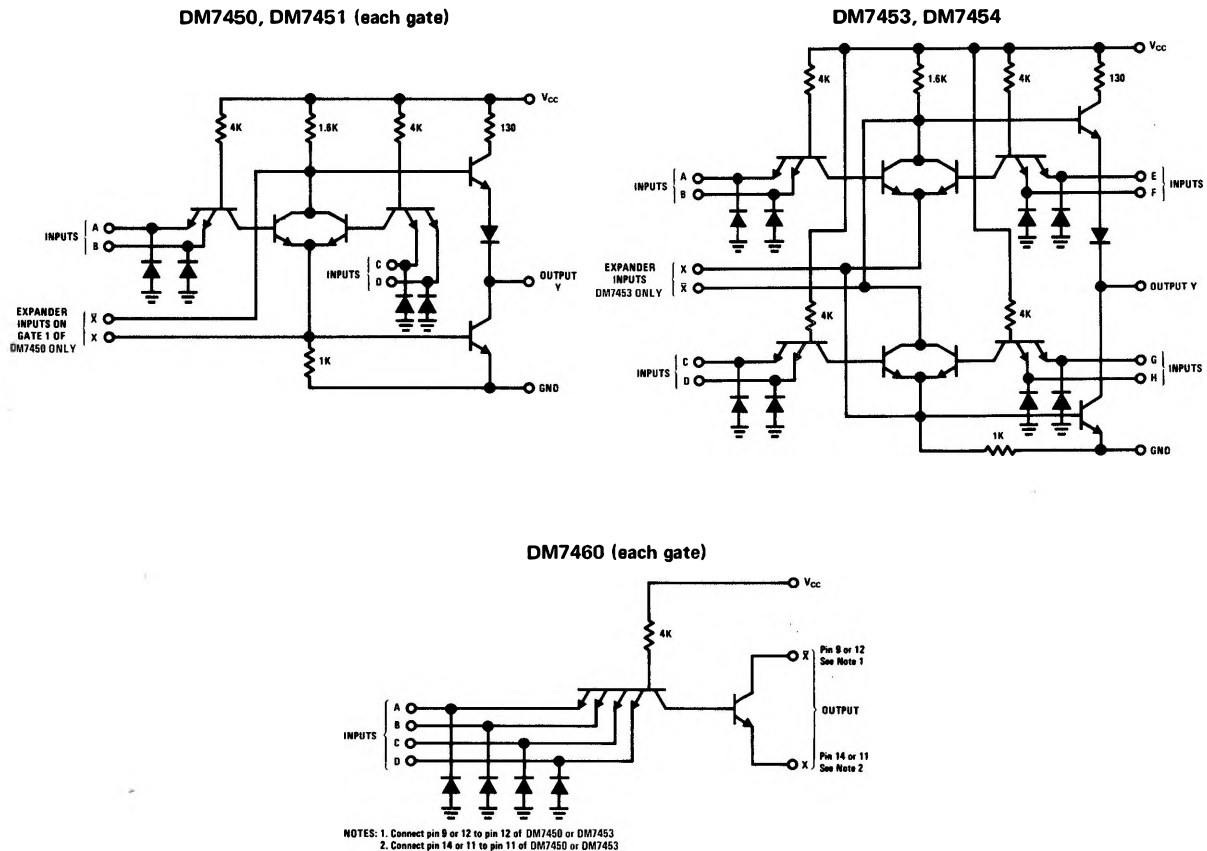
general description

The devices described in this data sheet employ TTL to achieve high speed at moderate power dissipation. They are consolidated onto one sheet since they perform the AND-OR-INVERT function with only differing numbers of AND inputs and OR terms. Characteristics include high noise immunity, low output impedance, good capacitance drive capability, and minimal variation in switching time with temperature. The gates are compatible with and interchangeable with Series 74 devices.

Key features include:

- Input Clamping Diodes
- Typical Noise Immunity 1 Volt
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Allowable Power Supply Variation 4.75V to 5.25V
- Average Propagation Delay 13 ns
- Average Power Dissipation 14 mW/ gate

schematic diagrams



absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to +150°C
Fan-Out	10
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics (Notes 1, 3) (DM7450, DM7451, DM7453, DM7454)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	$V_{CC} = 5.0V$, $T_A = 25^\circ C$ $I_{IN} = -12 \text{ mA}$			-1.5	V
Logical "1" Input Voltage	$V_{CC} = 4.75V$	2.0			V
Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $V_{IN} = 0.8V$ $I_{OUT} = -400 \mu A$	2.4			V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $V_{IN} = 2.0V$ $I_{OUT} = 16 \text{ mA}$			0.4	V
Logical "1" Input Current	$V_{CC} = 5.25V$, $V_{IN} = 2.4V$			40	μA
Logical "1" Input Current	$V_{CC} = 5.25V$, $V_{IN} = 5.5V$			1	mA
Logical "0" Input Current	$V_{CC} = 5.25V$, $V_{IN} = 0.4V$			-1.6	mA
Output Short Circuit Current (Note 2)	$V_{CC} = 5.25V$, $V_{IN} = 0V$	-18		-55	mA
Supply Current — Logical "0" (Each Gate)	$V_{CC} = 5.25V$, $V_{IN} = 5.0V$		3.7	6.5	mA
Supply Current — Logical "1" (Each Gate)	$V_{CC} = 5.25V$, $V_{IN} = 0V$		2.0	3.6	mA
Propagation Delay Time to a Logical "0", t_{pd0}	$V_{CC} = 5.0V$, $T_A = 25^\circ C$ $C = 50 \text{ pF}$, $N = 10$			15	ns
Propagation Delay Time to a Logical "1", t_{pd1}	$V_{CC} = 5.0V$, $T_A = 25^\circ C$ $C = 50 \text{ pF}$, $N = 10$			25	ns
Propagation Delay Time to Logical "0" Level (through DM7450 or DM7453)	$V_{CC} = 5.0V$, $T_A = 25^\circ C$ $C = 50 \text{ pF}$, $N = 10$			20	ns
Propagation Delay Time to Logical "1" Level (through DM7450 or DM7453)	$V_{CC} = 5.0V$, $T_A = 25^\circ C$ $C = 50 \text{ pF}$, $N = 10$			34	ns

Note 1: Min/Max units apply across the guaranteed temperature range of 0°C to 70°C unless otherwise specified. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

Note 2: Not more than 1 output should be shorted at a time.

Note 3: Measurements made with expandable inputs open.

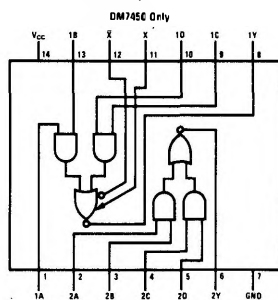
electrical characteristics (Note 1) (DM7460)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Diode Clamp Voltage	$V_{CC} = 5.0V$ $I_{IN} = -12 \text{ mA}$	$T_A = 25^\circ\text{C}$			-1.5	V
Logical "1" Input Voltage	$V_{CC} = 4.75V$, $R_{V_{CC} \text{ to COLLECTOR}} = 1.1 \text{ k}\Omega$, $V_{EMITTER} = 1V$, $T_A = 0^\circ\text{C}$		2			V
Logical "0" Input Voltage	$V_{CC} = 4.75V$, $R_{EMITTER \text{ to GND}} = 1.2 \text{ k}\Omega$, $V_{COLLECTOR} = 4.5V$, $I_{COLLECTOR} = 0.27 \text{ mA}$, $T_A = 0^\circ\text{C}$				0.8	V
Logical "0" Output Voltage (With Respect to Emitter)	$V_{CC} = 4.75V$, $V_{EMITTER} = 1V$, $T_A = 0^\circ\text{C}$	$V_{IN} = 2V$, $R_{V_{CC} \text{ to COLLECTOR}} = 1.1 \text{ k}\Omega$,			0.4	V
Logical "1" Output Current	$V_{CC} = 4.75V$, $V_{COLLECTOR} = 4.5V$, $T_A = 0^\circ\text{C}$	$V_{IN} = 0.8V$, $R_{EMITTER \text{ to GND}} = 1.2 \text{ k}\Omega$,		270		μA
Logical "0" Output Current	$V_{CC} = 4.75V$, $V_{EMITTER} = 1V$	$V_{IN} = 2V$,	-0.43			mA
Logical "0" Input Current	$V_{CC} = 5.25V$,	$V_{IN} = 0.4V$			-1.6	mA
Logical "1" Input Current	$V_{CC} = 5.25V$, $V_{CC} = 5.25V$,	$V_{IN} = 2.4V$ $V_{IN} = 5.5V$		40 1		μA mA
Logical "0" Supply Current (Each Gate)	$V_{CC} = 5V$, $V_{EMITTER} = 0.85V$	$V_{IN} = 5V$,		0.6	1.25	mA
Logical "1" Supply Current (Each Gate)	$V_{CC} = 5V$, $V_{EMITTER} = 0.85V$	$V_{IN} = 0$		1.0	1.8	mA

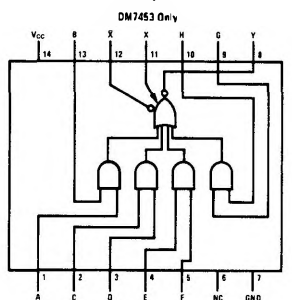
(DM7450, DM7453 only) using expander inputs, $T_A = 0^\circ\text{C}$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Expander Current	$V_{CC} = 4.75V$, $I_{SINK} = 16 \text{ mA}$	$V_{PIN 11 \text{ to PIN } 12} = 0.4V$			3.1	mA
Base-Emitter Voltage of Output Transistor (Q)	$V_{CC} = 4.75V$, $I_{PIN 11} = 0.62 \text{ mA}$,	$I_{SINK} = 16 \text{ mA}$, $R_{PIN 11 \text{ to PIN } 12} = 0$			1	V
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{PIN 11} = 0.27 \text{ mA}$,	$I_{LOAD} = -400 \mu\text{A}$, $I_{PIN 12} = -0.27 \text{ mA}$	2.4			V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{PIN 11} = 0.43 \text{ mA}$,	$I_{SINK} = 16 \text{ mA}$, $R_{PIN 11 \text{ to } 12} = 130\Omega$			0.4	V

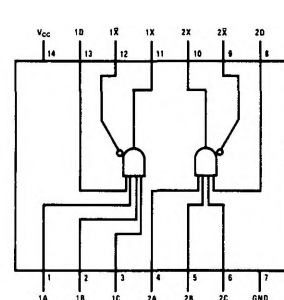
Note 1: Min/Max units apply across the guaranteed temperature range of 0°C to 70°C unless otherwise specified. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25^\circ\text{C}$.

connection diagrams**DM7450, DM7451**

$Y = (AB) + (CD) + X$ $X = ABCD$ from DM7460
 NOTES: Expander nodes X and Y are on the DM7450 only. If not used, leave open.
 Make no external connection to pins 11 and 12 of the DM7451.
 A total of four expander gates may be connected to the DM7450 expandable gate.

DM7453, DM7454

$Y = (AB) + (CD) + (EF) + (GH) + X$ $X = ABCD$ from DM7460
 NOTES: Expander nodes X and Y are on the DM7453 only. If not used, leave open.
 Make no external connection to pins 11 and 12 of the DM7454.
 A total of four expander gates may be connected to the DM7453 expandable gate.

DM7460

$X = ABCD$
 NOTE: Connect Pin 9 or 12 to pin 12 of DM7450 or DM7453.
 Connect Pin 10 or 11 to pin 11 of DM7450 or DM7453.