National Semiconductor

54LS173/DM74LS173A TRI-STATE® 4-Bit D-Type Register

General Description

This four-bit register contains D-type flip-flops with totem-pole TRI-STATE® outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

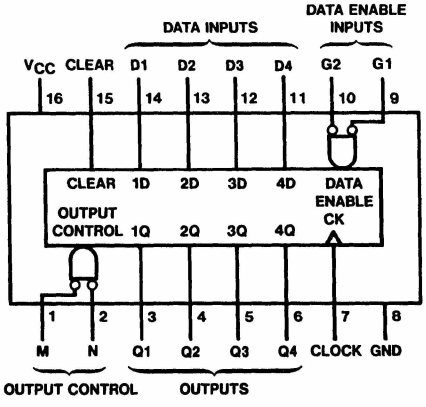
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers

Connection Diagram

Dual-In-Line Package



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Order Number 54LS173DMQB, 54LS173FMQB, 54LS173LMQB, DM74LS173AM or DM74LS173AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs					Output Q
Clear	Clock	Data Enable G1	Data Enable G2	Data D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = High Level (Steady State)

L = Low Level (Steady State)

↑ = Low-to-High Level Transition

X = Don't Care (Any Input Including Transitions)

Q_0 = The Level of Q Before the Indicated Steady State Input Conditions Were Established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS173			DM74LS173A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency (Note 1)		30			0		30	MHz
	Clock Frequency (Note 2)					0		20	MHz
t_W	Pulse Width (Note 3)	Clock	20			17			ns
		Clear	17			17			
t_{SU}	Setup Time (Note 3)	Enable	17			23			ns
		Data	15			15			
t_H	Hold Time (Note 3)	Enable	0			0			ns
		Data	5			0			
t_{REL}	Clear Release Time		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 45 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 150 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			17	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS C_L = 50 pF		DM74LS C_L = 150 pF, R_L = 667Ω		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		20		ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		28		34	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		28		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		30		40	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control (M or N) to Any Q		23		34	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control (M or N) to Any Q		28		45	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 8)	Output Control (M or N) to Any Q		17		25	ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 8)	Output Control (M or N) to Any Q		23		25	ns

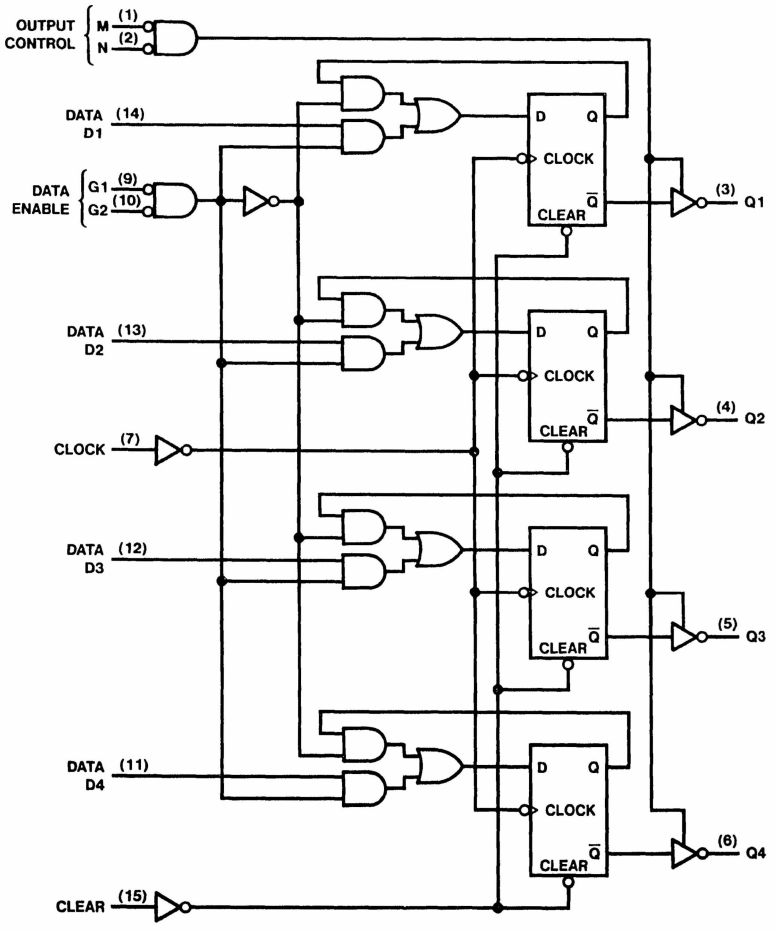
Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open: Clear grounded after a momentary 4.5V; N, G1, G2 and all data inputs grounded: and the CLOCK and M input at 4.5V.

Note 7: C_L = 5 pF.

Logic Diagram



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