National Semiconductor

54LS323/DM74LS323
8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

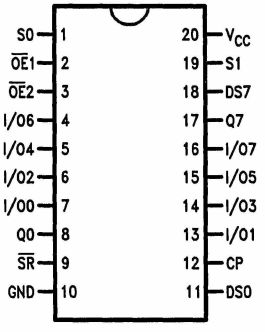
The 'LS323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Its function is similar to the 'LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

Features

- Common I/O for reduced pin count
- Four operation modes: shift left, shift right, parallel load and store
- Separate continuous inputs and outputs from Q0 and Q7 allow easy cascading
- Fully synchronous reset
- TRI-STATE outputs for bus oriented applications

Connection Diagram

Dual-In-Line Package



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Order Number 54LS323DMQB, 54LS323FMQB, DM74LS323WM or DM74LS323N
See NS Package Number J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D_S0	Serial Data Input for Right Shift
D_S7	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{SR}$	Synchronous Reset Input (Active LOW)
$\overline{OE}$1, $\overline{OE}$2	TRI-STATE Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q0, Q7	Serial Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS323			DM74LS323			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW S0 or S1 to CP	24 24			24 24			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S0 or S1 to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW I/O_n, D_S0, D_S7 to CP	15 15			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW I/O_n, D_S0, D_S7 to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SR}$ to CP	30 20			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SR}$ to CP	0 0			0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15			15 15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
			S_n Inputs			0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
			S_n Inputs			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
			S_n Inputs			−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				60	mA
I_{OZH}	TRI-STATE Output Off Current HIGH	V_{CC} = V_{CCH}, V_{OZH} = 2.7V				40	μA
I_{OZL}	TRI-STATE Output Off Current LOW	V_{CC} = V_{CCH}, V_{OZL} = 0.4V				−400	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	54LS323 C_L = 15 pF		DM74LS323 R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	Min	Max	
f_{max}	Maximum Input Frequency	35		35		MHz
t_{PLH}	Propagation Delay CP to Q0 or Q7		26		23	ns
t_{PHL}			28		25	
t_{PLH}	Propagation Delay CP to I/O_n		25		25	ns
t_{PHL}			35		29	
t_{PZH}	Output Enable Time C_L = 50 pF		18		18	ns
t_{PZL}			25		23	
t_{PHZ}	Output Disable Time C_L = 5 pF		15		15	ns
t_{PLZ}			20		15	

Functional Description

The 'LS323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S0 and S1 as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

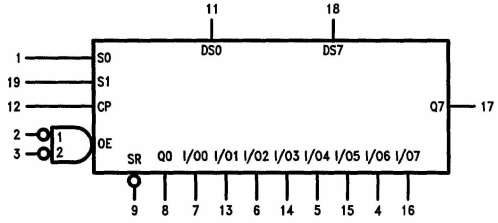
A HIGH signal on either $\overline{OE}1$ or $\overline{OE}2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{SR}$	S1	S0	CP	
L	X	X	↑	Synchronous Reset; Q0–Q7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; DS0 → Q0, Q0 → Q1, etc.
H	H	L	↑	Shift Left; DS7 → Q7, Q7 → Q6, etc.
H	H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

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Logic Diagram