National Semiconductor

DM74S299
TRI-STATE® 8-Bit Universal Shift/Storage Registers

Description

This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

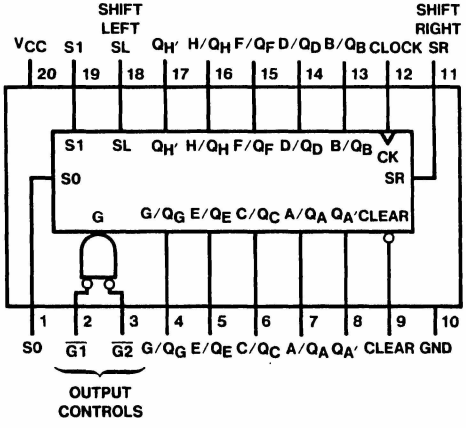
Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the TRI-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Features

- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- TRI-STATE outputs drive bus lines directly
- Can be cascaded for N-bit word lengths
- Operates with outputs enabled or at high Z
- Guaranteed shift (clock) frequency 50 MHz
- Typical power dissipation 700 mW

Connection Diagram

Dual-In-Line Package



TL/F/6485–1

Order Number DM74S299N
See NS Package Number N20A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM74S299 Min	DM74S299 Nom	DM74S299 Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current (Q_A thru Q_H)				−6.5	mA
	High Level Output Current ($Q_{A'}$, $Q_{H'}$)				−0.5	
I_{OL}	Low Level Output Current (Q_A thru Q_H)				20	mA
	High Level Output Current ($Q_{A'}$, $Q_{H'}$)				6	
f_{CLK}	Clock Frequency (Note 2)		0	70	50	MHz
f_{CLK}	Clock Frequency (Note 3)		0	60	40	MHz
t_W	Pulse Width (Note 5)	Clock High	10			ns
		Clock Low	10			
		Clear Low	10			
t_{SU}	Setup Time (Notes 4 & 5)	Select	15↑			ns
		Data High	7↑			
		Data Low	5↑			
t_H	Hold Time (Notes 4 & 5)		5↑			ns
t_{REL}	Clear Release Time (Note 5)		10↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: Data includes the two serial inputs and the eight input/output data lines.

Note 5: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	Q_A thru Q_H	2.4	3.2		V
			$Q_{A'}$, $Q_{H'}$	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A thru H, S0, S1			100	μA
			Any Other			50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Clock, Clear			−2	mA
			S0, S1			−0.5	
			Other			−0.25	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied (Q_A thru Q_H)	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				100	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied (Q_A thru Q_H)	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−250	μA
I_{OS}	Short Circuit Output Current (Q_A thru Q_H)	V_{CC} = Max (Note 2)		−40		−100	mA
	Short Circuit Output Current ($Q_{A'}$, $Q_{H'}$)	V_{CC} = Max (Note 2)		−20		−100	
I_{CC}	Supply Current	V_{CC} = Max			140	225	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω (Note 2)				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	(Note 3)	50		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 2)	Clock to $Q_{A'}$ or $Q_{H'}$		20		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 2)	Clock to $Q_{A'}$ or $Q_{H'}$		20		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q_A thru Q_H				21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q_A thru Q_H				21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 2)	Clear to $Q_{A'}$ or $Q_{H'}$		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q_A thru Q_H				24	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H				18	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H				18	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	$\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H		12			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	$\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H		12			ns

Note 1: C_L = 5 pF.

Note 2: R_L = 1KΩ for delays measured to $Q_{A'}$ and $Q_{H'}$.

Note 3: For testing f_{MAX} all outputs are loaded simultaneously.

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G}1$†	$\overline{G}2$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

$Q_{A0}...Q_{H0}$ = The output logic level of Q_X before the indicated input conditions were established.

H = high level, L = low logic level, X = either low or high logic level

$Q_{An}...Q_{Hn}$ = The output logic level before the active transition (↑) of the clock input.

Logic Diagram