National Semiconductor

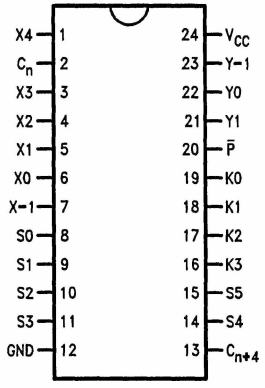
DM93S43
4-Bit by 2-Bit Twos Complement Multiplier

General Description

The DM93S43 is a high-speed twos complement multiplier. The device is a 4-bit by 2-bit building block that can be connected in an iterative array to perform multiplication of two binary numbers of variable lengths. The device can generate the twos complement product, without correction, of two binary numbers presented in twos complement notation.

Connection Diagram

Dual-In-Line Package



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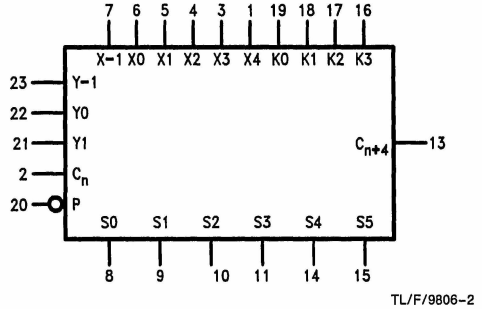
Order Number DM93S43N
See NS Package Number N24A

Logic Symbol



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V_{CC} = Pin 24
GND = Pin 12

Pin Name	Description
X-1, X3, X4, X0, X1, X2	Multiplicand Inputs
Y0, Y-1, Y1	Multiplier Inputs
C_n	Carry Input
K0–K3	Constant Inputs
$\overline{P}$	Polarity Control Input (Active Low for High Operands)
S0–S5	Product Outputs
C_{n+4}	Carry Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S43			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			149	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $S_0 - S_3$		13 11	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to S_4, S_5		16 15	ns

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations) (Continued)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay kn to C_{n+4}		12 13	ns
t_{PLH} t_{PHL}	Propagation Delay kn to S0 − S3		14 12	ns
t_{PLH} t_{PHL}	Propagation Delay kn to S4, S5		19 17	ns
t_{PLH} t_{PHL}	Propagation Delay xn to C_{n+4}		15 24	ns
t_{PLH} t_{PHL}	Propagation Delay xn to S0 − S3		25 25	ns
t_{PLH} t_{PHL}	Propagation Delay xn to S4, S5		30 21	ns
t_{PLH} t_{PHL}	Propagation Delay yn to C_{n+4}		25 27	ns
t_{PLH} t_{PHL}	Propagation Delay yn to S0 − S3		28 27	ns
t_{PLH} t_{PHL}	Propagation Delay yn to S4, S5		32 30	ns

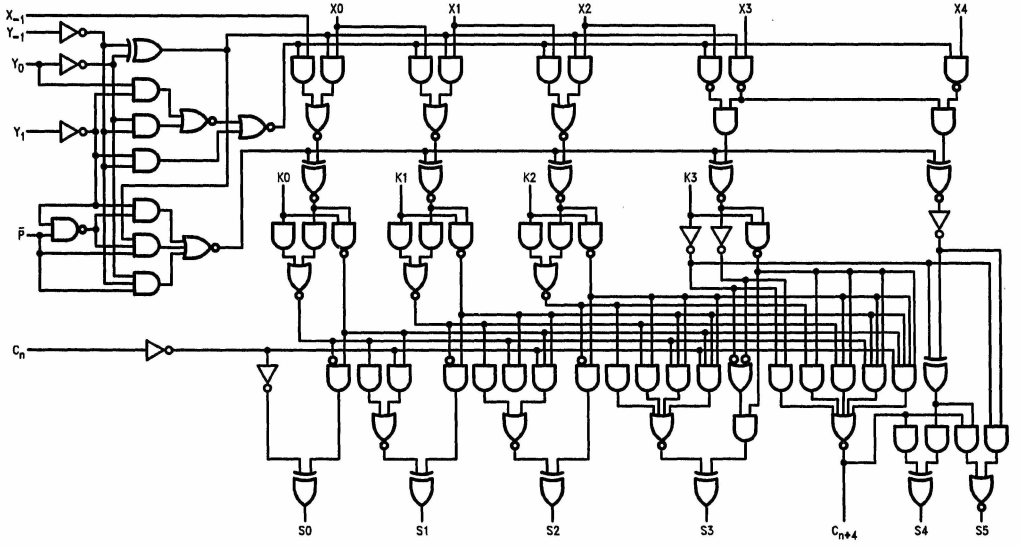
Functional Description

The DM93S43 is a super fast hardware multiplier employing Schottky technology and twos complement arithmetic. It multiplies a multiplicand of four bits by a multiplier of two bits and forms a basic iterative logic cell. It can also multiply in active HIGH (positive logic) or active LOW (negative logic) representations by reinterpreting the active levels of the inputs, outputs and the Polarity Control ($\overline{P}$). The binary number with 1 as the most significant bit is treated as a negative number represented in twos complement form. These DM93S43 iterative logic cells can be connected to implement multiplication of an X-bit number by a Y-bit number. This application requires X • Y ÷ 4 • 2 packages and the resulting product has X + Y bits. At the beginning of the array, a constant can be presented at the K inputs that will be added to the least significant part of the product. The packages can be connected in parallel, triangular or split-array scheme depending on the speed requirement. The '41 ALU can be used with these multipliers in the split-array scheme to obtain high speed multiplication.

TABLE I. Switching Test Conditions

Input	Outputs	Inputs at 0V (Remaining Inputs at 4.5 V)
C_n	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, y−1, y1 All x
k0	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, y−1, y1 All x
k1	C_{n+4}, S1 − S3, S4, S5	$\overline{P}$, y−1, y1 All x
k2	C_{n+4}, S2, S3, S4, S5	$\overline{P}$, y−1, y1 All x
k3	S3	$\overline{P}$, y−1, y1 All x
k3	S4, S5	$\overline{P}$, y−1, y1 All x, C_n
x−1	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, y−1, All k
x0	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, y−1, y1, All k
x1	C_{n+4}, S1 − S3, S4, S5	$\overline{P}$, y−1, y1, All k
x2	C_{n+4}, S2, S3, S4, S5	$\overline{P}$, y−1, y1, All k
x3, x4	S3	$\overline{P}$, y−1, y1, All k
x3, x4	S4, S5	$\overline{P}$, y−1, y1, All k, C_n
x3, x4	S4, S5	$\overline{P}$, y−1, All k, C_n
y−1	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, x1, x2, x3, x4, All k
y0	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, x1, x2, x3, x4, All k
y1	C_{n+4}, S0 − S3, S4, S5	x0, x1, x2, x3, x4, All k

Logic Diagram



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