National Semiconductor

DP117-X/DP117-XR/μA117-X/μA117-XR Series Winchester Disk Read/Write Preamplifiers

General Description

The DP117-X/DP117-XR, μA117-X/μA117-XR Series High Performance Read/Write Preamplifiers are intended for use in Winchester disk drives which employ center tapped ferrite or manganese-zinc read/write heads. The circuit can interface with up to eight read/write heads which makes it ideal for multi-platter disk drive designs. Designed to reside in the Head/Disk Assembly (HDA) of Winchester disk drives, the Read/Write Preamplifiers provide termination, gain, and output buffering for the disk heads as well as switched write current. Certain write fault conditions are detected and reported to protect recording integrity. The parts are available with internal damping resistor (DP117-R) and without internal damping resistor (DP117).

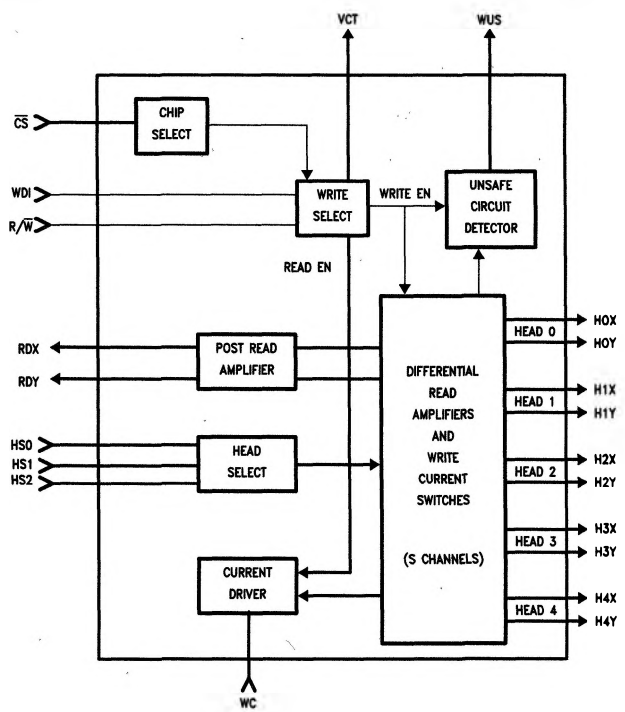
Features

- Wide bandwidth, high gain, low noise
- Up to eight read/write channels
- Internal write fault condition detection
- 5.0V and 12V power supply voltages
- Independent read and write data lines
- TTL control and data logic levels
- Externally programmable write current
- Available with internal damping resistor
- Compatible with SSI 117 family

Part Selection

Device Code	Channels
μA117-2	2
μA117-4	4
μA117-6	6

Block Diagram (Typical, DP117-X)



TL/F/9406–7

Absolute Maximum Ratings All voltages referenced to GND

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic: −65°C to +175°C
- Plastic: −65°C to +150°C

Operating Junction Temperature Range: +25°C to +135°C

Lead Temperature
- Ceramic (Soldering, 60 seconds): 300°C
- Plastic (Soldering, 10 seconds): 265°C

Internal Power Dissipation (Notes 1 & 2)
- 28L-Ceramic DIP: 2.50W
- 24L-Ceramic DIP: 1.95W
- 18L-Ceramic DIP: 1.58W
- 24L-Brazed Flatpak: 0.97W
- 24L-Ceramic Flatpak: 0.90W
- 28L-PLCC: 1.39W

Supply Voltage (V_{CC1}): 6.0V

Supply Voltage (V_{CC2}): 15V

Write Current (IWC): 70 mA

Input Voltage Range

Head Select (HS0, HS1, HS2): −0.4V to V_{CC1} + 0.3V

Write Current (WC)
Voltage in read and idle modes. (Write mode must be current limited to −70 mA): −0.3V to V_{CC1} + 0.3V

Chip Select (CS): −0.4V to V_{CC1} + 0.3V

Read/Write (R/W): −0.4V to V_{CC1} + 0.3V

DC Supply Voltage
- (V_{DD1}): −0.3V to +14V
- (V_{DD2}): −0.3V to +14V
- (V_{CC}): −0.3V to +6.0V

Digital Input Voltage Range
(V_{IN}): −0.3V to V_{CC} + 0.3V

Head Port Voltage Range
(V_H): −0.3V to V_{DD} + 0.3V

WUS Port Voltage Range
(V_{WUS}): −0.3V to +14V

Write Current (I_W): 60 mA

Output Current (I_O)
- RDX, RDY: −10 mA
- VCT: −60 mA
- WUS: +12 mA

Recommended Operating Conditions

DC Supply Voltage
- (V_{DD1}): 12V ±10%
- (V_{DD2}): 6.5V to V_{DD1}
- (V_{CC}): 5.0V ±10%

Head Inductance (Lh): 5.0 μH to 15 μH

Damping Resistor (External) (RD): 500Ω to 2000Ω

RCT Resistor (RCT): 90Ω ±5.05 (½W)

Write Current (I_W): 25 mA to 50 mA

RDX, RDY Output Current (I_O): 0 μA to 100 μA

Note 1: $T_{J\ MAX}$ = 150°C for the Plastic, and 175°C for the Ceramic.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 28L-Ceramic DIP at 16.7 mW/°C, the 24L-Ceramic DIP at 13 mW/°C, the 18L-Ceramic DIP at 10.5 mW/°C, the 24L-Brazed Flatpak at 6.5 mW/°C, the 24L-Ceramic Flatpak at 6.0 mW/°C, and the 28L-PLCC at 11.2 mW/°C.

DC Characteristics 25°C ≤ T_J < 125°C, V_{DD1} = 12V, V_{CC} = 5.0V, unless otherwise specified

Symbol	Parameter		Conditions		Min	Max	Units
I_{CC}	Supply Current		Read/Idle Mode			25	mA
			Write Mode			30	
I_{DD}	Supply Current		Idle Mode			25	mA
			Read Mode			50	
			Write Mode			30 + I_W	
P_C	Power Consumption		T_J = 125°C	Idle Mode		400	mW
				Read Mode		600	
				Write Mode, I_W = 50 mA, RCT = 90Ω		850	
				Write Mode, I_W = 50 mA, RCT = 0Ω		1050	
V_{IL}	Digital Inputs	Input Voltage LOW			−0.3	0.8	V
V_{IH}		Input Voltage HIGH			2.0	V_{CC} + 0.3	V
I_{IL}		Input Current LOW	V_{IL} = 0.8V		−0.4		mA
I_{IH}		Input Current HIGH	V_{IH} = 2.0V			100	μA
V_{OL}	WUS Output		I_{OL} = 8.0 mA			0.5	V
I_{OH}			V_{OH} = 5.0V			100	μA
V_{CT}	Center Tap Voltage		Read Mode		4.0 (typ)		V
			Write Mode		6.0 (typ)		V

Write Characteristics

V_{DD1} = 12V, V_{CC} = 5.0V, I_W = 45 mA, Lh = 10 μH, f (Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, $R_{D\ EXT}$ = 750Ω or $R_{D\ INT}$, unless otherwise specified

Parameter	Conditions	Min	Max	Units
Write Current Range		10	50	mA
Write Current Constant "K"		133	147	V
Differential Head Voltage Swing		5.7		V (pk)
Unselected Differential Head Current			2.0	mA (pk)
Differential Output Capacitance			15	pF
Differential Output Resistance	Without Internal Resistors	10k		Ω
	With Internal Resistors	538	1.0k	
WDI Transition Frequency	WUS = LOW	400 (typ)		kHz
I_{WC} to Head Current Gain		18 (typ)		mA/mA

Read Characteristics

V_{DD1} = 12V, V_{CC} = 5.0V, Lh = 10 μH, f (Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, (V_{in} is referenced to V_{CT}), $R_{D\ EXT}$ = 750Ω or $R_{D\ INT}$, unless otherwise specified

Parameter	Conditions		Min	Max	Unit
Differential Voltage Gain	V_{IN} = 1.0 mV_{p-p} at 300 kHz RL (RDX), RL (RDY) = 1.0 kΩ		80	120	V/V
Dynamic Range	Input Voltage, V_I, where gain falls by 10%. V_{IN} = V_I + 0.5 mV_{p-p} at 300 kHz		−2.0	2.0	mV
Bandwidth (−3 dB)	I Zs I < 5.0Ω, V_{IN} = 1.0 mV_{p-p}		30		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			2.1	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5.0 MHz			23	pF
Differential Input Resistance	f = 5.0 MHz	Without Internal Resistors	2k		Ω
		With Internal Resistors	440	850	
Input Bias Current				45	μA
Common Mode Rejection Ratio	V_{CM} = V_{CT} + 100 mV_{p-p} at 5.0 MHz		50		dB
Power Supply Rejection Ratio	100 mV_{p-p} at 5.0 MHz on V_{DD1}, V_{DD2} or V_{CC}		45		dB
Channel Separation	Unselected Channels: V_{IN} = 100 mV_{p-p} at 5.0 MHz and Selected Channel: V_{IN} = 0 mV_{p-p}		45		dB
Output Offset Voltage			−480	480	mV
Common Mode Output Voltage			5.0	7.0	V
Single Ended Output Resistance	f = 5.0 MHz			35	Ω
Internal Damping Resistor			560	1070	Ω

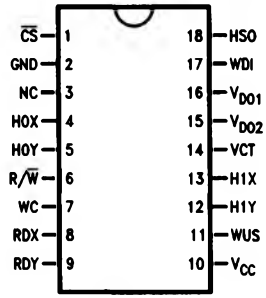
Switching Characteristics

V_{DD1} = 12V, V_{CC} = 5.0V, T_J = 25°C, I_W = 45 mA, Lh = 10 μH, f (Data) = 5.0 MHz, $R_{D\ EXT}$ = 750Ω or $R_{D\ INT}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
R/$\overline{W}$	R/$\overline{W}$ to Write	Delay to 90% of Write Current		1.0	μs
	R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% Decay of Write Current		1.0	μs
$\overline{CS}$	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope		1.0	μs
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current		1.0	
HS0 HS1 HS2	to Any Head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope		1.0	μs
WUS	Safe to Unsafe—TD1	I_W = 50 mA	1.6	8.0	μs
	Unsafe to Safe—TD2	I_W = 20 mA		1.0	
Head Current	Propagation Delay—TD3, TD4	Lh = 0 μH, Rh = 0Ω from 50% Points		25	ns
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time		2	
	Rise/Fall Time	10%–90% Points		20	

Connection Diagrams

18-Lead Molded DIP

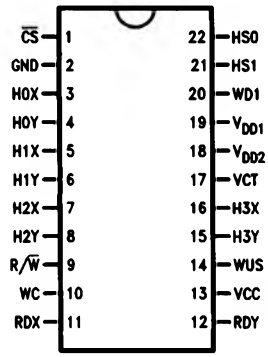


TL/F/9406–1

Top View

†Order Number μA1172DC or μA1172RDC
††See NS Package Number N18A

22-Lead Molded DIP



TL/F/9406–2

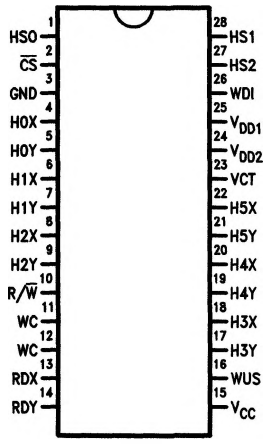
Top View

†Order Number μA1174PC or μA1174RPC
††See NS Package Number N22A

†For most current order information, contact your local sales office.
††For most current package information, contact product marketing.

Connection Diagrams (Continued)

28-Lead DIP

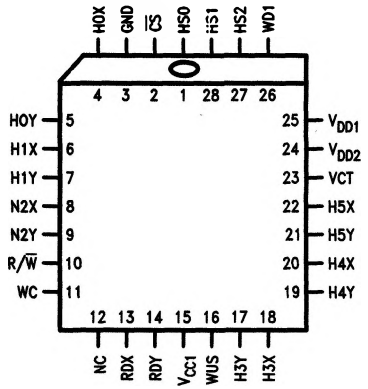


TL/F/9406–6

Top View

†Order Number μA1176PC or μA1176RPC
††See NS Package Number N28B

28-Lead PLCC



TL/F/9406–5

Top View

†Order Number μA1176QC or μA1176RQC
††See NS Package Number V28A

†For most current order information, contact your local sales office.
††For most current package information, contact product marketing.

Functional Description

In the Write mode, the DP117-X/DP117-XR, μA117-X/μA117-XR Series accepts TTL compatible write data pulses on the WDI lead. On the falling edge of each write data pulse, a current transition is made in the selected head. Head selection is accomplished via TTL input signals: HS0, HS1, HS2 (see Table II). Internal circuitry senses the following conditions:

1. Absence of data transitions.
2. Open circuit head connection.
3. Absence of write current.
4. Short circuit head connection.
5. Idle or read mode.

Any or all of the above conditions would result in a high level on the write unsafe (WUS) output signal.

During read operations, the DP117-X amplifies the differential voltages appearing across the selected R/W head lead and applies the amplified signal differentially to data lines RDX and RDY.

Pin Descriptions

Lead	Name	Function
$\overline{CS}$	Chip Select	Chip Select High disables the read/write function of the device and forces idle mode. (TTL)
R/$\overline{W}$	Read/Write Select	A Logic High places the devices in read mode and a Logic Low forces write mode. Refer to Table I. (TTL)
H0X, Y through H5X, Y	Read/Write Head Connections	The DP117 has five pairs of read/write connections. The X and Y phases are made consistent with the read output, RDX and RDY, phases. (Differential)
RDX, Y	Read Data Outputs	The chip has one pair of read data outputs which is multiplexed to the appropriate head connections. (Differential)
HS0 through HS2	Head Select Inputs	The eight read/write heads are addressed with the head select inputs. Refer to Table II. (TTL)
WC	Write Current Input	This lead sets the current level for the write mode. An external resistor is connected from this lead to ground, and write current is determined by the value of this resistor divided into the write current constant K, which is typically 140V.
WDI	Write Data Input	The write data input toggles the write current between the X and Y selected head connections. Write current is switched on the negative edge of WDI. The initial direction for write current is the X side of the switch and is set upon entering read or idle mode. (TTL)
V_{DD2}	Resistor Center Tap	In some versions (determined by lead availability) of the DP117-X series, a resistor may be connected between RCT and V_{DD1} to reduce internal power dissipation. If this resistor is not used, RCT must be connected externally to V_{DD1}.
VCT	Center Tap Voltage	The center tap output provides bias voltage for the head inputs in read and write mode. It should be connected to the center tap of the read/write heads.
WUS	Write Unsafe	A high logic level at the write unsafe output indicates a fault condition during write. Write unsafe will also be high during read and idle mode. (Open collector)

TABLE I. Read/Write Select

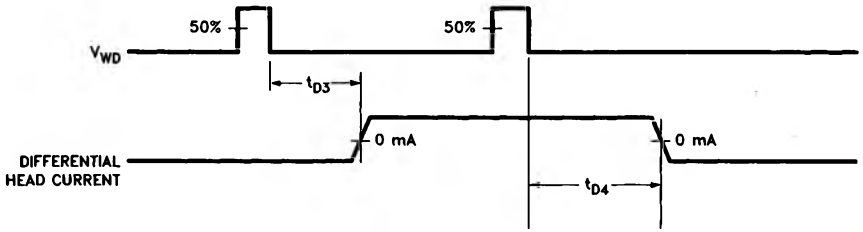
Operating Modes		
Chip Select $\overline{CS}$	**Read/Write R/$\overline{W}$**	**Mode**
1	X	idle
0	1	Read
0	0	Write

TABLE II. Head Select Inputs

Head Selection			
HS0	**HS1**	**HS2**	**Head Selected (Note 1)**
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5

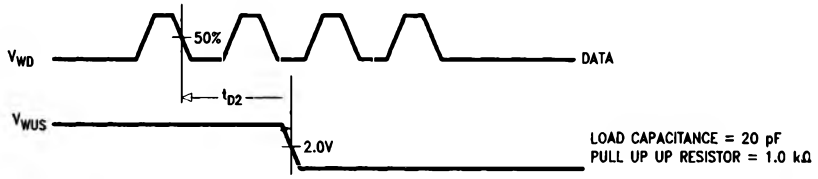
Note 1: If selected head is beyond the capacity of the DP117-X model, the open input condition on the selected input will be reported as an unsafe level at the WUS output.

Timing Diagrams



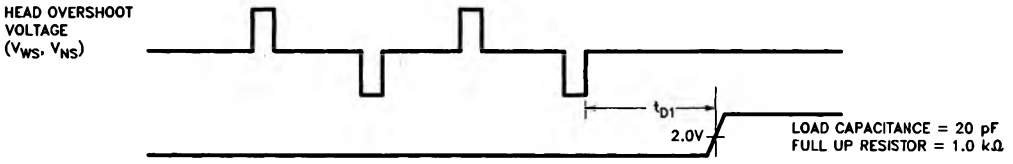
TL/F/9406–8

FIGURE 1. Head Current Timing



TL/F/9406–9

FIGURE 2a. Unsafe to Safe Timing



TL/F/9406–10

FIGURE 2b. Safe to Unsafe Timing