

DP7310/DP8310/DP7311/DP8311 Octal Latched **Peripheral Drivers**

General Description

The DP7310/8310, DP7311/8311 Octal Latched Peripheral Drivers provide the function of latching eight bits of data with open collector outputs, each driving up to 100 mA DC with an operating voltage range of 30V. Both devices are designed for low input currents, high input/output voltages, and feature a power up clear (outputs off) function.

The DP7310/8310 are positive edge latching. Two active low write/enable inputs are available for convenient data bussing without external gating.

The DP7311/8311 are positive edge latches. The active low strobe input latches data or allows fall through operation when held at logic "0". The latches are cleared (outputs off) with a logic "0" on the clear pin.

Features

- High current, high voltage open collector outputs
- Low current, high voltage inputs
- **Connection Diagrams**



Top View

All outputs simultaneously sink rated current "DC" with no thermal derating at maximum rated temperature

- Parallel latching or buffering
- Separate active low enables for easy data bussing
- Internal "glitch free" power up clear
- 10% V_{CC} tolerance

Applications

- High current high voltage drivers
- Relav drivers
- Lamp drivers
- LED drivers
- TRIAC drivers
- Solenoid drivers
- Stepper motor drivers
- Level translators
- Fiber-optic LED drivers



Top View

TI /F/5246-2

Order Number DP7310J, DP7311J, **DP8310N or DP8311N** See NS Package Number J20A or N20A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	35V
Output Voltage	35V
Maximum Power Dissipation* at 25°C	
Cavity Package	1821 mW
DP8310/DP8311	2005 mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Derate cavity package 12.1 mW/°C above 25°C	; derate molded package

Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	4.5	5.5	v
Temperature			
DP7310/DP7311	-55	+ 125	•C
DP8310/DP8311	0	+ 70	۰C
Input Voltage		30	v
Output Voltage		30	v

DC Electrical Characteristics DP7310/DP8310, DP7311/DP8311 (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
VIH	Logical "1" Input Voltage		2.0			V
V _{IL}	Logical "0" Input Voltage				0.8	V
V _{OL}	Logical "0" Output Voltage	Data outputs latched to logical "0", V _{CC} = Min.				
	DP7310/DP7311 DP8310/DP8311	$I_{OL} = 75 \text{ mA}$ $I_{OL} = 100 \text{ mA}$		0.35	0.4 0.5	v v
ЮН	Logical "1" Output Current	Data outputs latched to logical "1", $V_{CC} = Min$.				
	DP7310/DP7311 DP8310/DP8311	V _{OH} = 25V V _{OH} = 30V		2.5	500 250	μΑ μΑ
Ιн	Logical "1" Input Current	$V_{IH} = 2.7V, V_{CC} = Max$		0.1	25	μΑ
ų	Input Current at Maximum Input Voltage	$V_{IN} = 30V, V_{CC} = Max$		1	250	μΑ
կլ	Logical "0" Input Current	$V_{IN} = 0.4V, V_{CC} = Max$		-215	-300	μA
V _{clamp}	Input Clamp Voltage	I _{IN} = 12 mA		-0.8	-1.5	V
ICC0	Supply Current, Outputs On	Data outputs latched to a logical "0". All inputs are at logical "1", V _{CC} = Max.				
	DP7310			100	125	mA
	DP8310			100	152	mA
	DP7311 DP8311			88 88	117 125	mA mA
ICC1	Supply Current, Outputs Off	Data outputs latched to a logic "1". Other conditions same as I _{CC0} .				
	DP7310			40	47	mA
	DP8310			40	57	mA
	DP7311			25	34	mA
	DP8311			25	36	mA

16.0 mW/°C above 25°C.

AC Electrical Characteristics DP7310/DP8310: $V_{CC} = 4.5V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$						
Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{pd0}	High to Low Propagation Delay Write Enable Input to Output	(Figure 1)		40	120	ns
^t pd1	Low to High Propagation Delay Write Enable Input to Output	(Figure 1)		70	150	ns
^t SETUP	Minimum Set-Up Time Data in to Write Enable Input	t _{HOLD} = 0 ns <i>(Figure 1)</i>	45	20		ns
t _{pWH} , t _{pWL}	Minimum Write Enable Pulse Width	(Figure 1)	60	25		ns
t _{THL}	High to Low Output Transition Time	(Figure 1)		16	35	ns
t _{TLH}	Low to High Output Transition Time	(Figure 1)		38	70	ns
C _{IN}	"N" Package (Note 4)			5	15	pF

AC Electrical Characteristics DP7311/DP8311: $V_{CC} = 5V$, $T_A = 25^{\circ}C$

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{pd0}	High to Low Propagation Delay Data In to Output	(Figure 2)		30	60	ns
^t pd1	Low to High Propagation Delay Data to Output	(Figure 2)		70	100	ns
^t SETUP	Minimum Set-Up Time Data in to Strobe Input	t _{HOLD} ≈ 0 ns <i>(Figure 2)</i>	0	-25		ns
t _{pWL}	Minimum Strobe Enable Pulse Width	(Figure 2)	60	35		ns
t _{pdC}	Propagation Delay Clear to Data Output	(Figure 2)		70	135	ns
t _{pWC}	Minimum Clear Input Pulse Width	(Figure 2)	60	25		ns
t _{THL}	High to Low Output Transition Time	(Figure 2)		20	35	ns
t _{TLH}	Low to High Output Transition Time	(Figure 2)		38	60	ns
CIN	Input Capacitance—Any Input	(Note 4)		5	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the -55° C to $+125^{\circ}$ C temperature range for the DP7310/DP7311 and across the 0°C to $+70^{\circ}$ C for the DP8310/DP8311. All typical values are for T_A = 25°C, V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Input capacitance is guaranteed by periodic testing. $f_{TEST} = 10$ kHz at 300 mV, $T_A = 25^{\circ}C$.

DP7310/DP7311/DP8310/DP8311

Logic Table

	DP7310/DP8310					
Write Enable 1 WE ₁	Write Enable 2 WE ₂	Data Input DI ₁₋₈	Data Output DO ₁₋₈			
0	0	x	Q			
0	5	0	1			
0	5	1	0			
<u>_</u>	0	0	1			
<u>_</u>	0	1	0			
0	1	x	Q			
1	0	x	Q			
1	1	X	Q			

	DP7311/DP8311					
Clear CLR	Strobe STR	Data Input DI ₁₋₈	Data Output DO ₁₋₈			
1	1	×	a			
1	0	0	1			
1	0	1	0			
0	X	X	1			

X = Don't Care

1 = Outputs Off

0 =Outputs On Q =Pre-existing Output $\checkmark =$ Positive Edge Transition

Block Diagrams



TL/F/5246-3



TL/F/5246-4





