



# DP802511 TROPIC™ RAM Relocation Register Decoder

## General Description

The DP802511, DP802512 and DP802513 form the majority of the MEMCS\_16 circuitry that is responsible for notifying the ISA bus (by way of MEMCS\_16) that it can execute 16-bit bus transfers with the DP8025 TROPIC.

The areas of the architecture that will benefit most from the increased performance of 16-bit transfers are the shared memory interface and the host boot ROM (if so designed). For the boot ROM it is a relatively simple matter of matching the jumpered configuration bits SD9-SD15 (BIOS/MMIO base address) with the system address (SA) lines. The MEMCS\_16 signal's maximum propagation delay from the SA lines is about 25 ns (assuming 8 MHz IBM® PC-AT®).

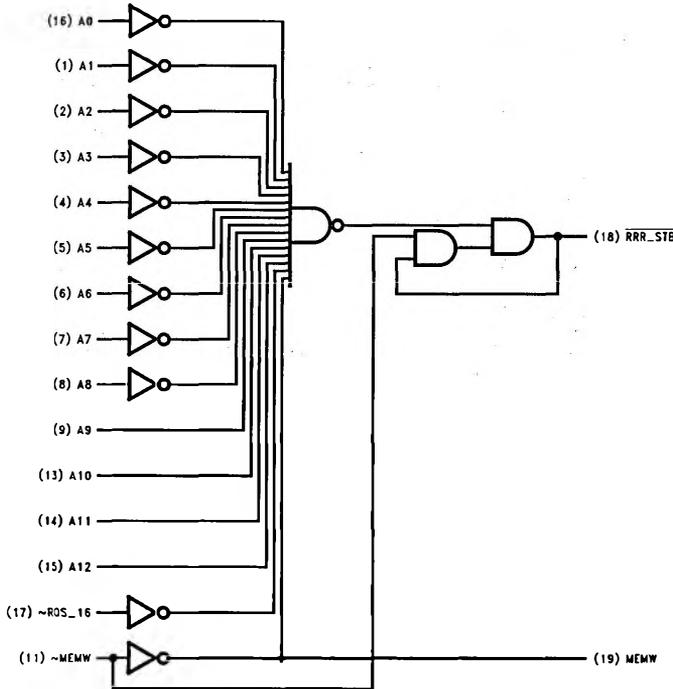
The shared memory interface RAM size is determined by jumper bits SD2 and SD3. These indicate the block size decoded to the shared memory MEMCS\_16 circuitry. The

address of this shared memory interface is software selectable. In order for the hardware to respond to the proper memory address it must shadow the RAM Relocation Register of the TROPIC's memory mapped I/O space. The data programmed into the RAM Relocation Register is latched into this shadowing register and used in conjunction with the system address lines to determine which address range contains the shared memory interface.

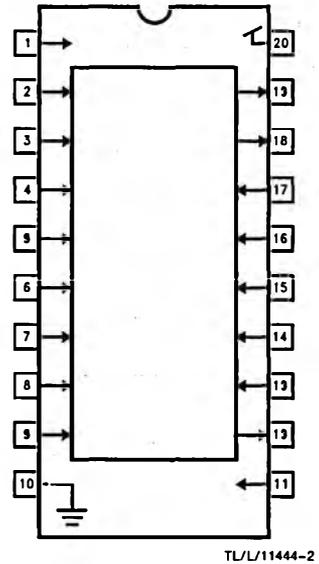
## Features

- Single chip custom logic solution
- Replaces glue logic
- Internal output latch
- t<sub>PD</sub> = 15 ns (max)

## Logic Diagram



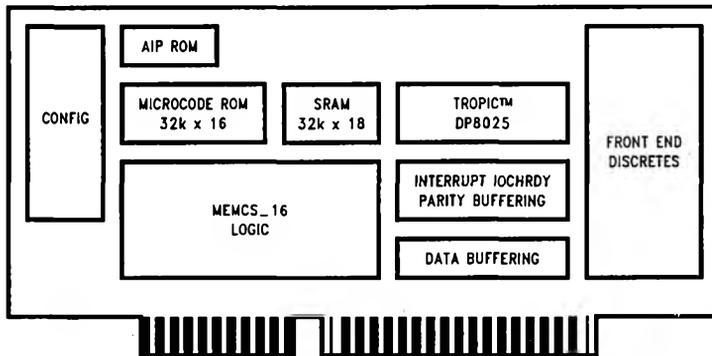
## Block Diagram



## Functional Description

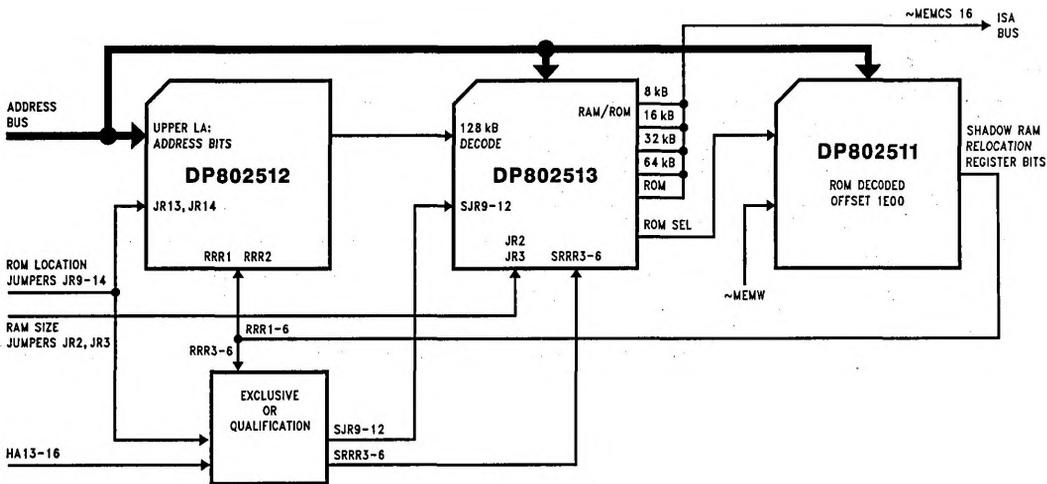
The DP802511 TROPIC RAM Relocation Register Decoder is manufactured using National's high performance 1.2  $\mu$ m CMOS process and is responsible for generating the RAM relocation register strobe signal ( $\overline{RRR\_STB}$ ) that points to the memory mapped RAM relocation register on the

DP8025 TROPIC. The device decodes the offset address 1E00 from an upper level decode, to generate the output strobe.  $\overline{RRR\_STB}$  will remain asserted for the duration of the memory write signal ( $\sim$ MEMW).



TL/L/11444-3

FIGURE 1. TROPIC™ 16-Bit ISA Token Ring Workstation Adapter



TL/L/11444-4

FIGURE 2. MEMCS\_16 Logic

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
Input Voltage	-2.5V to $V_{CC} + 1.0V$
Off-State Output Voltage	-2.5V to $V_{CC} + 1.0V$

Output Current	$\pm 100$ mA
Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +125°C
Junction Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

**Recommended Operating Conditions****SUPPLY VOLTAGE AND TEMPERATURE**

Symbol	Parameter	Commercial			Units
		Min	Nom	Max	
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$T_A$	Operating Free-Air Temperature	0	25	75	°C

**Electrical Characteristics** Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Temperature Range	Min	Typ	Max	Units
$V_{IH}$	High Level Input Voltage			2.0		$V_{CC} + 1$	V
$V_{IL}$	Low Level Input Voltage			-0.5		0.8	V
$V_{OH}$	High Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = -3.2$ mA	COM	2.4			V
$V_{OL}$	Low Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = 24$ mA	COM			0.5	V
$I_{OZH}$	High Level Off State Output Current	$V_{CC} = \text{Max}$ , $V_O = V_{CC} (\text{Max})$				10	$\mu\text{A}$
$I_{OZL}$	Low Level Off State Output Current	$V_{CC} = \text{Max}$ , $V_O = \text{GND}$				-10	$\mu\text{A}$
$I_I$	Maximum Input Current	$V_{CC} = \text{Max}$ , $V_I = V_{CC} (\text{Max})$				10	$\mu\text{A}$
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}$ , $V_I = V_{CC} (\text{Max})$				10	$\mu\text{A}$
$I_{IL}$	Low Level Input Current	$V_{CC} = 5.0V$ , $V_O = \text{GND}$				-10	$\mu\text{A}$
$I_{OS}^*$	Output Short Circuit Current	$V_{CC} = 5.0V$ , $V_O = \text{GND}$	COM	-30		-150	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$				90	mA
$C_I$	Input Capacitance	$V_{CC} = 5.0V$ , $V_I = 2.0V$				8	pF

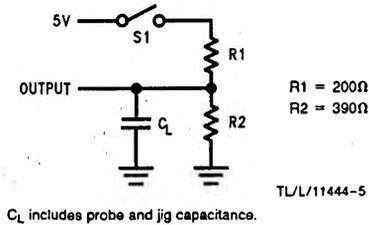
\*One output at a time for a maximum duration of one second.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

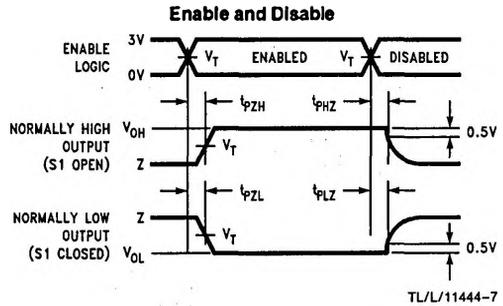
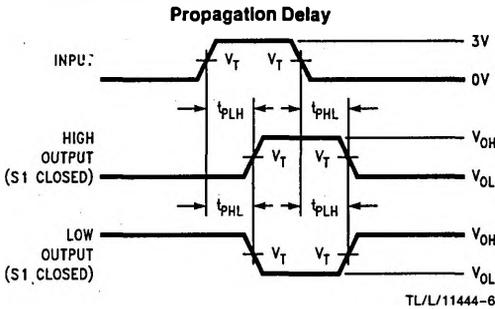
## Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions	DP802511		
			Commercial		
			Min	Max	Units
$t_{PD}$	Input to Output	S1 Closed, $C_L = 50 \text{ pF}$		15	ns
$t_{PZXI}$	Input to Output Enabled via Control Logic	Active High: S1 Open, $C_L = 50 \text{ pF}$ Active Low: S1 Closed, $C_L = 50 \text{ pF}$		15	ns
$t_{PXZI}$	Input to Output Disabled via Control Logic	Active High: S1 Open, $C_L = 5 \text{ pF}$ Active Low: S1 Closed, $C_L = 5 \text{ pF}$		15	ns

### AC Test Load



### Test Waveforms



### Input Schematic

